

# 74LV393

## Dual 4-bit binary ripple counter

Rev. 5 — 8 December 2015

Product data sheet

### 1. General description

The 74LV393 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC393 and 74HCT393.

The 74LV393 is a dual 4-stage binary ripple counter. Each counter features a clock input ( $\overline{nCP}$ ), an overriding asynchronous master reset input ( $\overline{nMR}$ ) and 4 buffered parallel outputs ( $nQ0$  to  $nQ3$ ). The counter advances on the HIGH-to-LOW transition of  $\overline{nCP}$ . A HIGH on  $\overline{nMR}$  clears the counter stages and forces the outputs LOW, independent of the state of  $\overline{nCP}$ .

### 2. Features and benefits

- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce) 0.8 V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  °C
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot) 2 V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  °C
- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V

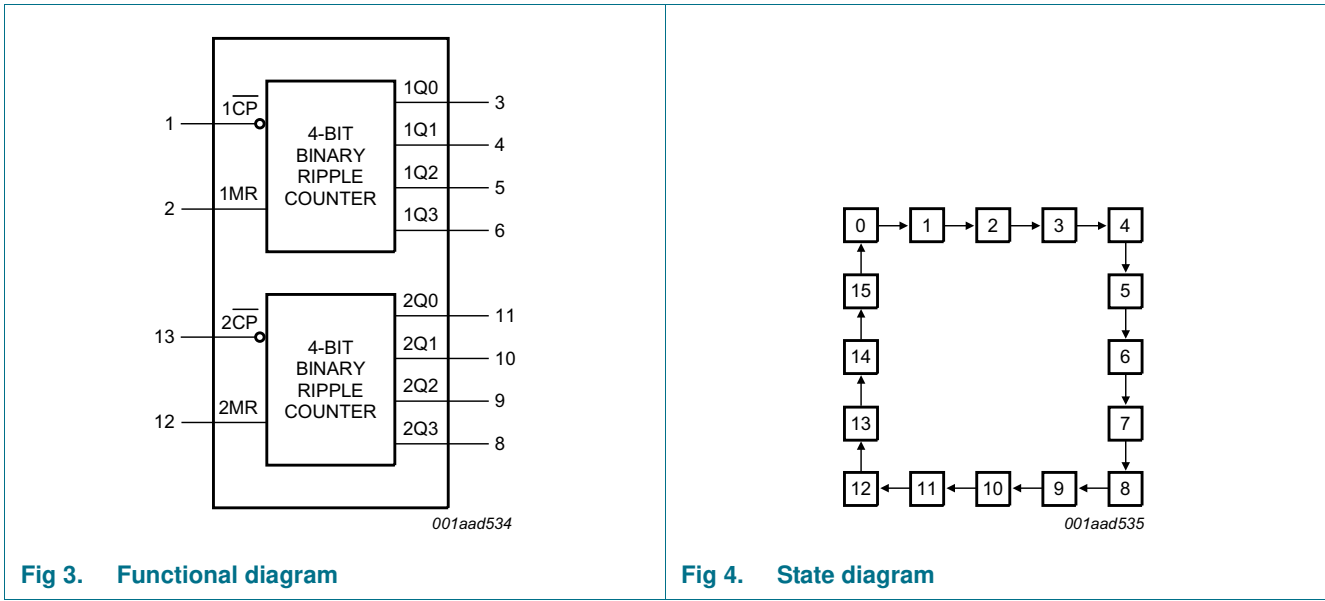
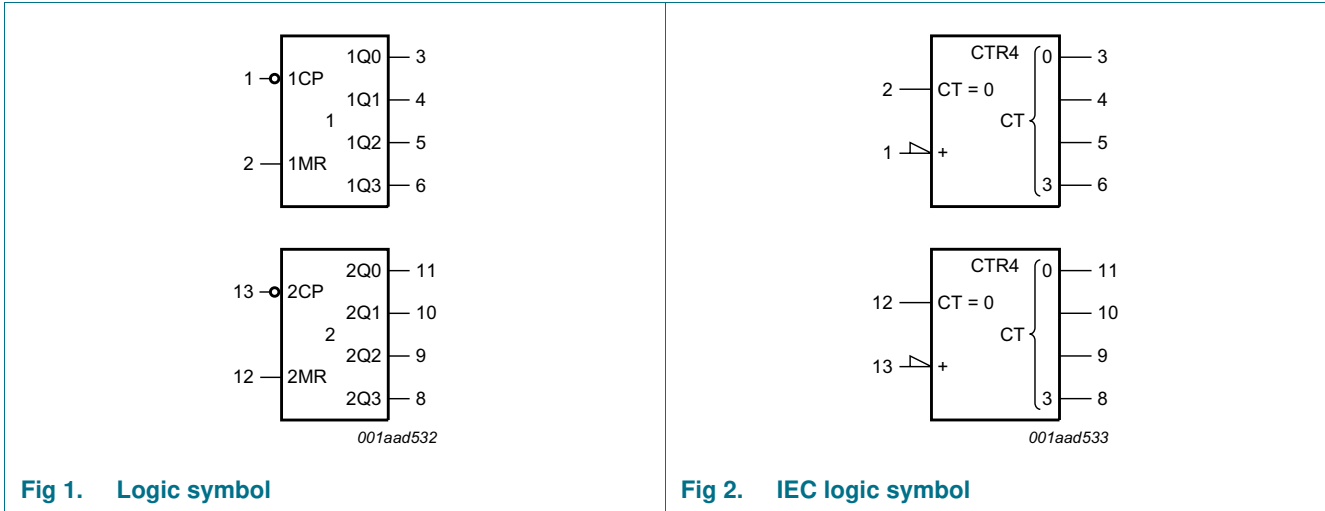
### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV393D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV393DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LV393PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1



### 4. Functional diagram



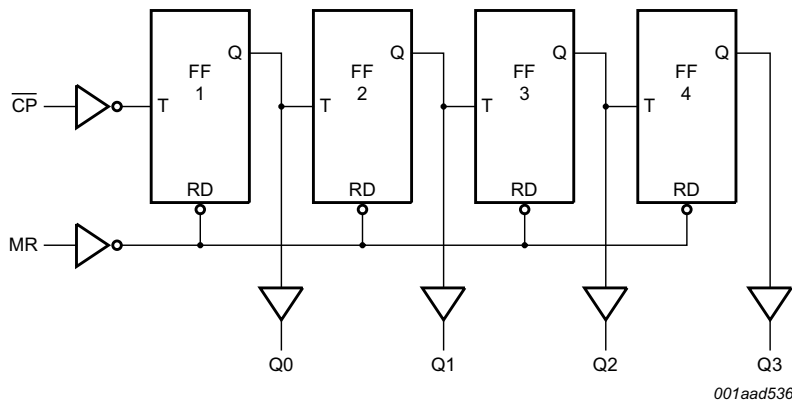


Fig 5. Logic diagram (one counter)

## 5. Pinning information

### 5.1 Pinning

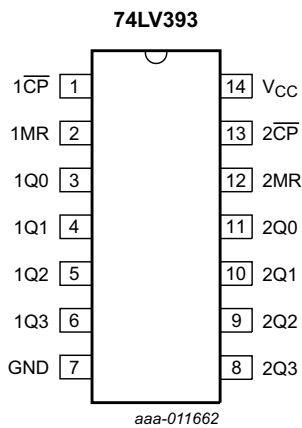


Fig 6. Pin configuration SO14

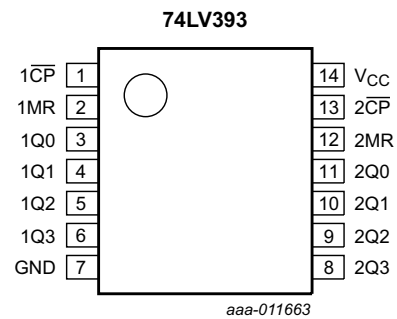


Fig 7. Pin configuration SSOP14 and TSSOP14

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP, 2CP	1, 13	clock input (HIGH-to-LOW, edge-triggered)
1MR, 2MR	2, 12	asynchronous master reset input (active HIGH)
1Q0, 1Q1, 1Q2, 1Q3	3, 4, 5, 6	flip-flop output
GND	7	ground (0 V)
2Q0, 2Q1, 2Q2, 2Q3	11, 10, 9, 8	flip-flop output
VCC	14	supply voltage

## 6. Functional description

Table 3. Count sequence for one counter [1]

Count	Output			
	nQ0	nQ1	nQ2	nQ3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

[1] H = HIGH voltage level; L = LOW voltage level.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 50$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	+50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		SO14 package [1]	-	500	mW
		(T)SSOP14 package [2]	-	400	mW

[1] For SO14 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

[2] For (T)SSOP14 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.0	3.3	3.6	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V to }2.0\text{ V}$	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V to }2.7\text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	100	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	0.9	-	-	0.9	-	V
		$V_{CC} = 2.0\text{ V}$	1.4	-	-	1.4	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	0.3	-	0.3	V
		$V_{CC} = 2.0\text{ V}$	-	-	0.6	-	0.6	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$						
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.2\text{ V}$	-	1.2	-	-	-	V
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.8	2.0	-	1.8	-	V
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 2.7\text{ V}$	2.5	2.7	-	2.5	-	V
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 3.0\text{ V}$	2.80	3.0	-	2.8	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$						
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.2\text{ V}$	-	0	-	-	-	V
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.2	-	0.2	V
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 2.7\text{ V}$	-	0	0.2	-	0.2	V
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 3.0\text{ V}$	-	0	0.2	-	0.2	V
$I_I$	input leakage current	$V_I = V_{CC}\text{ or GND}; V_{CC} = 3.6\text{ V}$	-	-	1.0	-	1.0	$\mu\text{A}$
		$V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A}; V_{CC} = 3.6\text{ V}$	-	-	20.0	-	160	$\mu\text{A}$
$\Delta I_{CC}$	additional quiescent supply current per input	$V_I = V_{CC} - 0.6\text{ V}; V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	500	-	850	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at  $T_{amb} = 25\text{ }^\circ\text{C}$ .

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nCP to nQ0; see <a href="#">Figure 8</a> <sup>[3]</sup>						
		V <sub>CC</sub> = 1.2 V	-	75	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	26	49	-	60	ns
		V <sub>CC</sub> = 2.7 V	-	19	36	-	44	ns
		V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 15 pF	-	12	-	-	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	14	29	-	35	ns
		nQ to nQn+1; see <a href="#">Figure 8</a> <sup>[3]</sup>						
		V <sub>CC</sub> = 1.2 V	-	25	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	9	17	-	20	ns
		V <sub>CC</sub> = 2.7 V	-	6	13	-	15	ns
		V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 15 pF	-	4	-	-	-	ns
V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[2]</sup>	-	5	10	-	12	ns		
t <sub>PHL</sub>	HIGH to LOW propagation delay	nMR to nQx; see <a href="#">Figure 9</a>						
		V <sub>CC</sub> = 1.2 V	-	70	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	-	24	44	-	54	ns
		V <sub>CC</sub> = 2.7 V	-	18	33	-	40	ns
		V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 15 pF	-	11	-	-	-	ns
V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[2]</sup>	-	13	26	-	32	ns		
t <sub>t</sub>	transition time	nQx; see <a href="#">Figure 8</a> <sup>[4]</sup>						
		V <sub>CC</sub> = 2.0 V	-	-	-	-	-	ns
		V <sub>CC</sub> = 2.7 V	-	-	-	-	-	ns
V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	-	-	-	ns		
t <sub>w</sub>	pulse width	nCP HIGH or LOW; see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 2.0 V	34	10	-	41	-	ns
		V <sub>CC</sub> = 2.7 V	25	8	-	30	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[2]</sup>	20	6	-	24	-	ns
		nMR HIGH; see <a href="#">Figure 9</a>						
		V <sub>CC</sub> = 2.0 V	34	12	-	41	-	ns
		V <sub>CC</sub> = 2.7 V	25	9	-	30	-	ns
V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[2]</sup>	20	7	-	24	-	ns		
t <sub>rec</sub>	recovery time	nMR to nCP; see <a href="#">Figure 9</a>						
		V <sub>CC</sub> = 1.2 V	-	5	-	-	-	ns
		V <sub>CC</sub> = 2.0 V	5	2	-	5	-	ns
		V <sub>CC</sub> = 2.7 V	5	2	-	5	-	ns
V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[2]</sup>	5	1	-	5	-	ns		

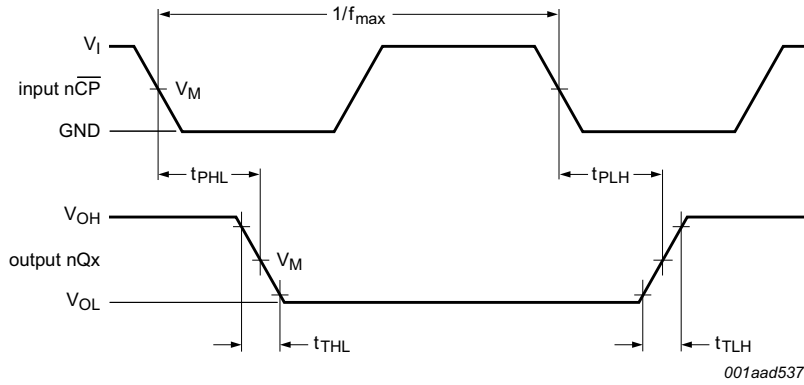
**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 10](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
f <sub>max</sub>	maximum frequency	see <a href="#">Figure 8</a>						
		V <sub>CC</sub> = 2.0 V	14	53	-	12	-	MHz
		V <sub>CC</sub> = 2.7 V	19	72	-	16	-	MHz
		V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 15 pF	-	99	-	-	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[2]</sup>	24	90	-	20	-	MHz
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[2]</sup> <sup>[5]</sup>	-	23	-	-	-	pF

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] Typical values are measured at V<sub>CC</sub> = 3.3 V.
- [3] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [4] t<sub>i</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

10.1 Waveforms

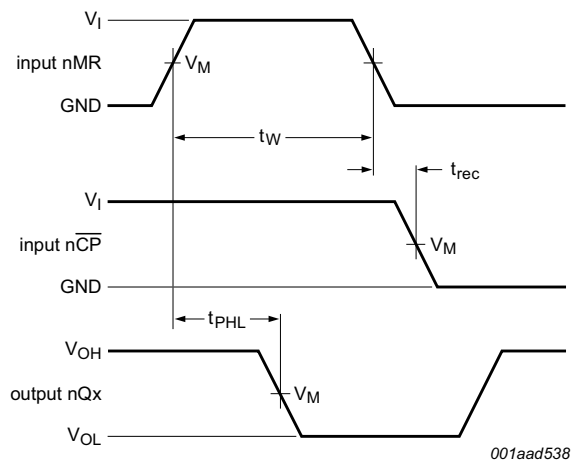


$t_{TLH} = 10\%$  and  $t_{TTL} = 90\%$ ,  
 Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 8. Propagation delays clock (nCP) to output (nQx), output transition times and maximum clock frequency**

**Table 8. Measurement points**

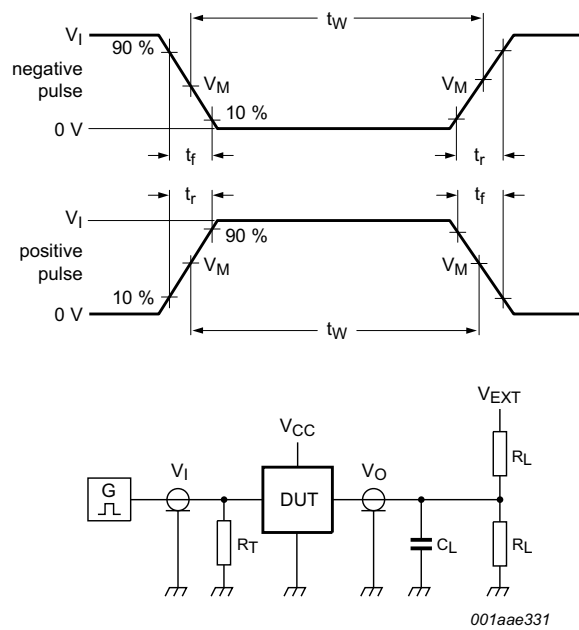
Supply voltage $V_{CC}$	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	$1.5V_{CC}$	$1.5V_{CC}$	$V_{OL} + 0.3V_{CC}$	$V_{OH} - 0.3V_{CC}$



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 9. Propagation delays clock (nCP) to output (nQx), pulse width master reset (nMR), and recovery time master reset (nMR) to clock (nCP)**





Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch.

**Fig 10. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
< 2.7 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns	15 pF, 50 pF	1 k $\Omega$	open

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

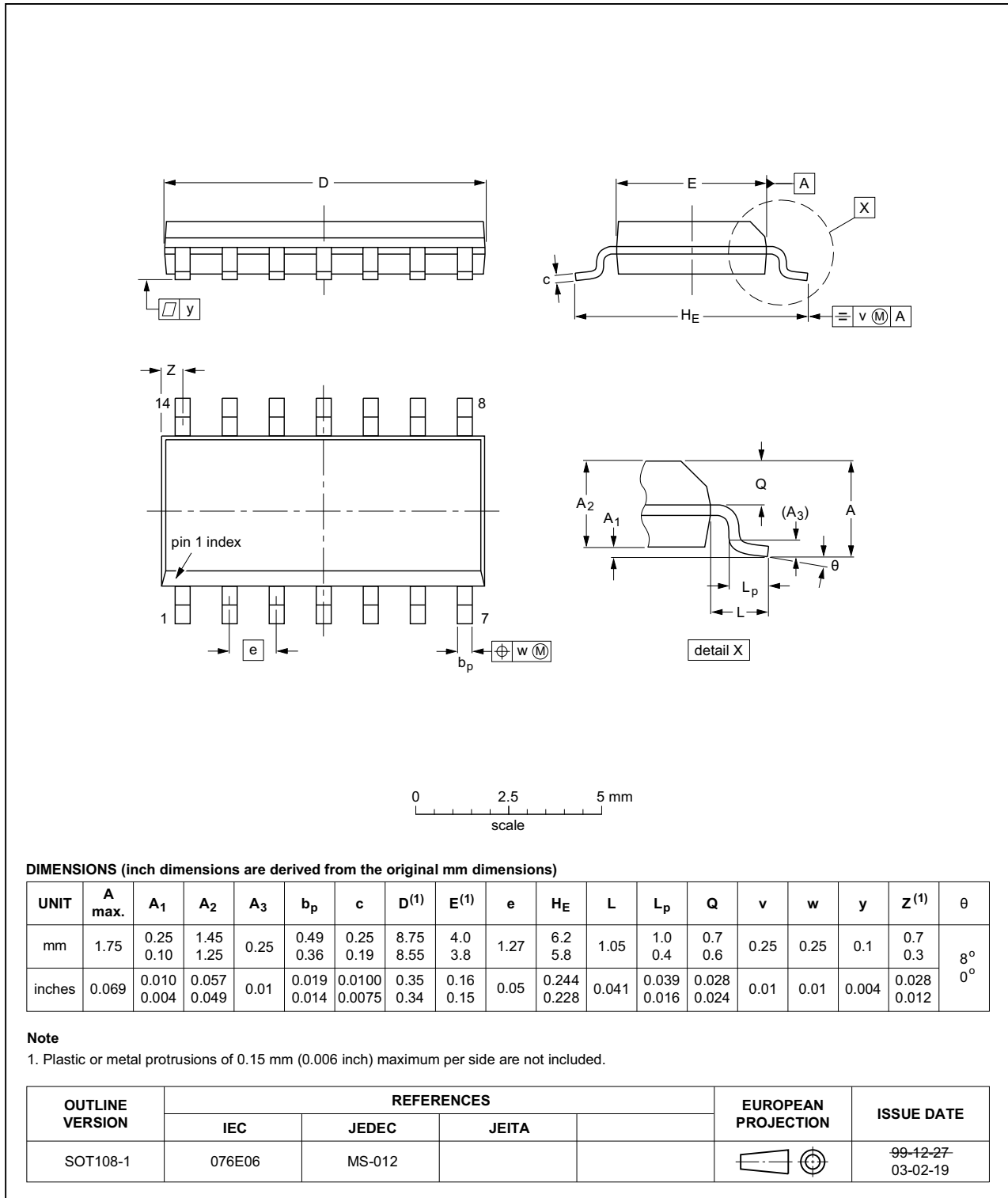


Fig 11. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

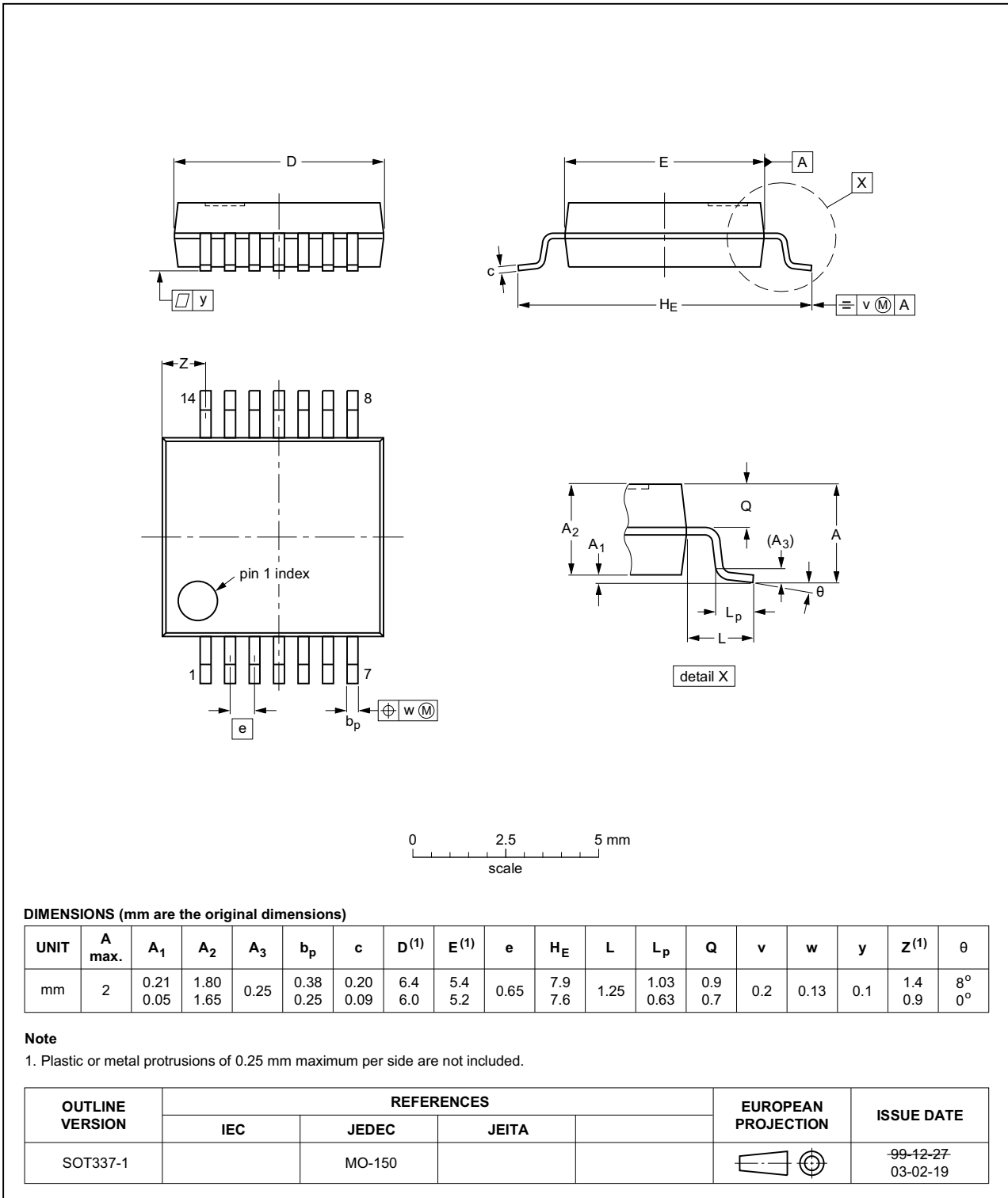


Fig 12. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

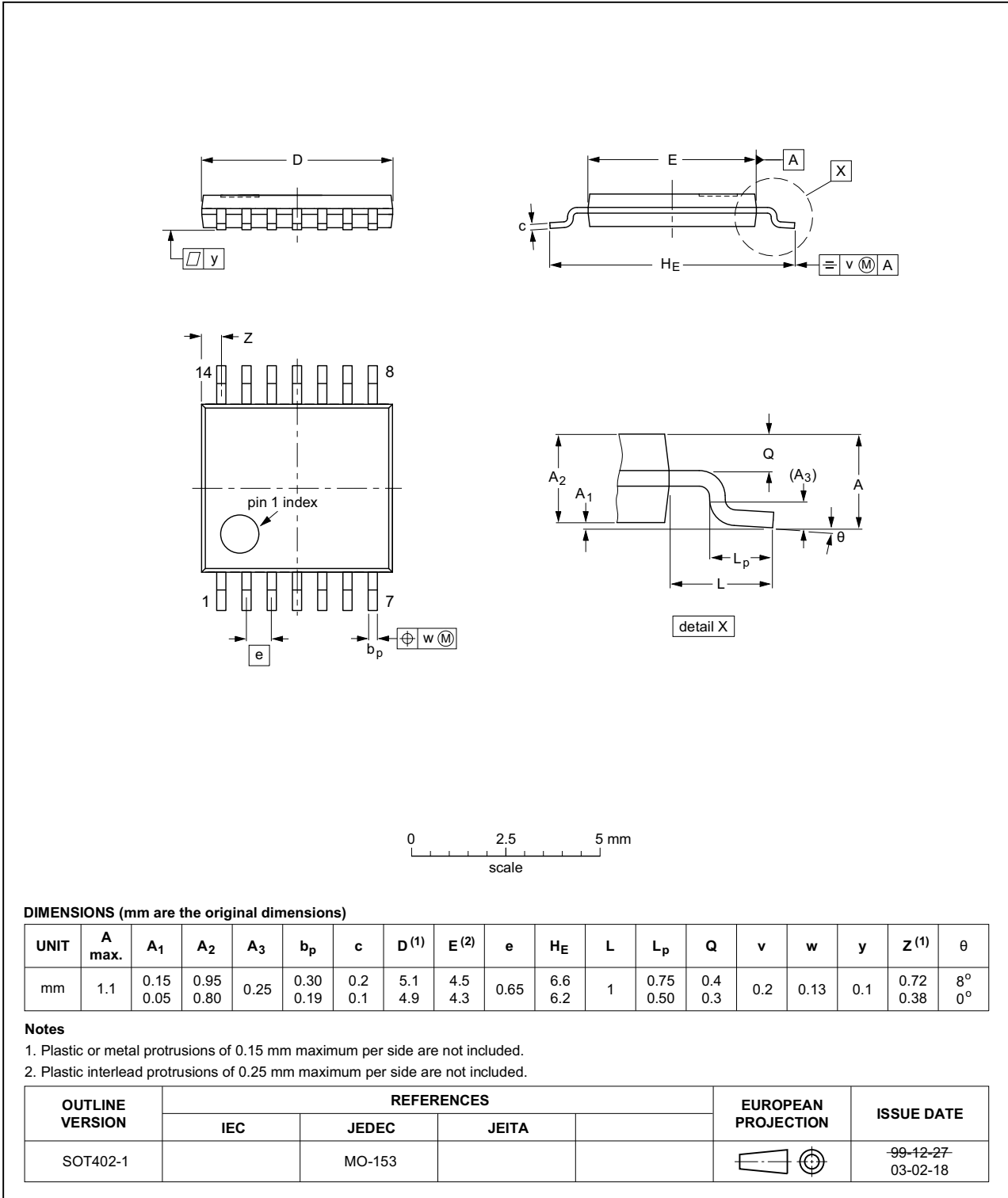


Fig 13. Package outline SOT402-1 (TSSOP14)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV393 v.5	20151208	Product data sheet	-	74LV393 v.4
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LV393N (SOT27-1) removed.</li> </ul>			
74LV393 v.4	20140918	Product data sheet	-	74LV393 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 4</a> minus sign added to the minimum ground current.</li> <li><a href="#">Figure 10</a> and <a href="#">Table 9</a> updated because of a missing load resistance in the test circuit.</li> </ul>			
74LV393 v.3	20140428	Product data sheet	-	74LV393 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74LV393 v.2	19970610	Product specification	-	74LV393 v.1
74LV393 v.1	19970304	Product specification	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 14.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 14.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 15. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 16. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>1</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>3</b>
5.1	Pinning .....	3
5.2	Pin description .....	3
<b>6</b>	<b>Functional description</b> .....	<b>4</b>
<b>7</b>	<b>Limiting values</b> .....	<b>4</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>5</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>5</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>6</b>
10.1	Waveforms .....	8
<b>11</b>	<b>Package outline</b> .....	<b>10</b>
<b>12</b>	<b>Abbreviations</b> .....	<b>13</b>
<b>13</b>	<b>Revision history</b> .....	<b>13</b>
<b>14</b>	<b>Legal information</b> .....	<b>14</b>
14.1	Data sheet status .....	14
14.2	Definitions .....	14
14.3	Disclaimers .....	14
14.4	Trademarks .....	15
<b>15</b>	<b>Contact information</b> .....	<b>15</b>
<b>16</b>	<b>Contents</b> .....	<b>16</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2015.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 8 December 2015

Document identifier: 74LV393