

# 74VHC03FT

## 1. Functional Description

- Quad 2-Input NAND Gate (Open Drain)

## 2. General

The 74VHC03FT is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the 74VHC00FT. But the 74VHC03FT has, as its outputs, high performance MOS N-channel transistors. (OPEN-DRAIN outputs) This device can, therefore, with a suitable pull-up resistors, be used in wired-AND, LED driver and other application.

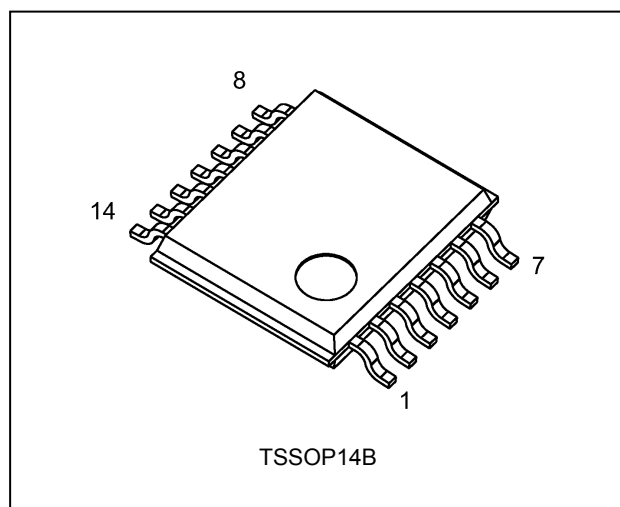
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## 3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature:  $T_{opr} = -40$  to  $125$  °C
- (3) High speed:  $t_{pd} = 3.7$  ns (typ.) at  $V_{CC} = 5.0$  V
- (4) Low power dissipation:  $I_{CC} = 2.0$   $\mu$ A (max) at  $T_a = 25$  °C
- (5) High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- (6) Power-down protection is provided on all inputs.
- (7) Wide operating voltage range:  $V_{CC(opr)} = 2.0$  to  $5.5$  V
- (8) Low noise:  $V_{OLP} = 0.8$  V (max)
- (9) Pin and function compatible with 74HC03

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

## 4. Packaging

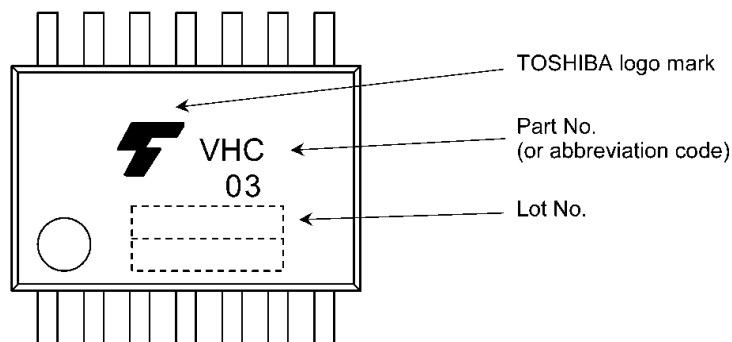


Start of commercial production  
2013-01

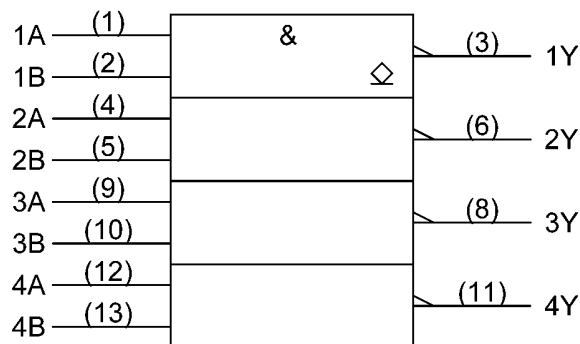
**5. Pin Assignment**



**6. Marking**



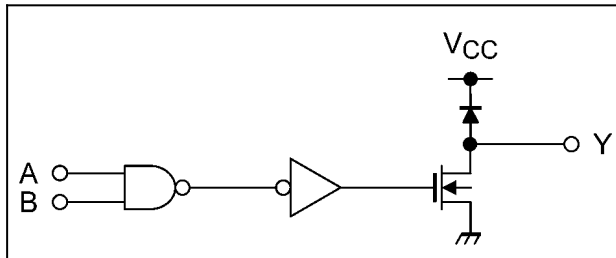
**7. IEC Logic Symbol**



**8. Truth Table**

A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

**9. System Diagram (per gate)**



**10. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to 7.0	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		-20	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		25	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 50$	mA
Power dissipation	$P_D$	(Note 1)	180	mW
Storage temperature	$T_{stg}$		-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: 180 mW in the range of  $T_a = -40$  to  $85^{\circ}C$ . From  $T_a = 85$  to  $125^{\circ}C$  a derating factor of  $-3.25$  mW/ $^{\circ}C$  shall be applied until 50 mW.

**11. Operating Ranges (Note)**

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$		2.0 to 5.5	V
Input voltage	$V_{IN}$		0 to 5.5	V
Output voltage	$V_{OUT}$		0 to $V_{CC}$	V
Operating temperature	$T_{opr}$		-40 to 125	$^{\circ}C$
Input rise and fall times	dt/dv	$V_{CC} = 3.3 \pm 0.3$ V	0 to 100	ns/V
		$V_{CC} = 5 \pm 0.5$ V	0 to 20	

Note: The operating ranges are required to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

**12. Electrical Characteristics**

**12.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	V	
			3.0 to 5.5	—	—	$V_{CC} \times 0.3$		
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36	
$I_{OL} = 8\text{ mA}$	4.5	—		—	0.36			
	Output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5	—	—	$\pm 0.25$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	$\pm 0.1$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	$\mu\text{A}$	

**12.2. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	0.50	V	
			3.0 to 5.5	—	$V_{CC} \times 0.3$		
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
$I_{OL} = 8\text{ mA}$	4.5	—		0.44			
	Output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5	—	—	$\pm 2.50$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	20.0	$\mu\text{A}$

**12.3. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $125\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	0.50	V	
			3.0 to 5.5	—	$V_{CC} \times 0.3$		
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.55	
$I_{OL} = 8\text{ mA}$	4.5	—		0.55			
	Output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5	—	—	$\pm 10.0$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	$\pm 2.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	40.0	$\mu\text{A}$

**12.4. AC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Typ.	Max	Unit
Propagation delay time	$t_{PZL}$		$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	15	—	5.5	7.9	ns
					50	—	8.0	11.4	
				$5.0 \pm 0.5$	15	—	3.7	5.5	
					50	—	5.2	7.5	
Propagation delay time	$t_{PLZ}$		$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	50	—	8.0	11.4	ns
				$5.0 \pm 0.5$	50	—	5.2	7.5	
Input capacitance	$C_{IN}$		—			—	4	10	pF
Output capacitance	$C_{OUT}$		—			—	5	—	pF
Power dissipation capacitance	$C_{PD}$	(Note 1)	—			—	6	—	pF

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4 \text{ (per gate)}$$

**12.5. AC Characteristics (Unless otherwise specified,  $T_a = -40\text{ to }85\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time	$t_{PZL}$	$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	15	1.0	9.5	ns
				50	1.0	13.0	
			$5.0 \pm 0.5$	15	1.0	6.5	
				50	1.0	8.5	
Propagation delay time	$t_{PLZ}$	$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	50	1.0	13.0	ns
			$5.0 \pm 0.5$	50	1.0	8.5	
Input capacitance	$C_{IN}$	—			—	10	pF

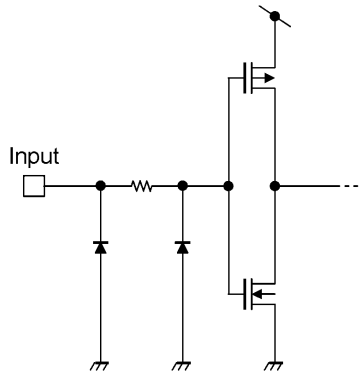
**12.6. AC Characteristics (Unless otherwise specified,  $T_a = -40\text{ to }125\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time	$t_{PZL}$	$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	15	1.0	11.0	ns
				50	1.0	14.5	
			$5.0 \pm 0.5$	15	1.0	7.5	
				50	1.0	9.5	
Propagation delay time	$t_{PLZ}$	$R_L = 1\text{ k}\Omega$	$3.3 \pm 0.3$	50	1.0	14.5	ns
			$5.0 \pm 0.5$	50	1.0	9.5	
Input capacitance	$C_{IN}$	—			—	10	pF

**12.7. Noise Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

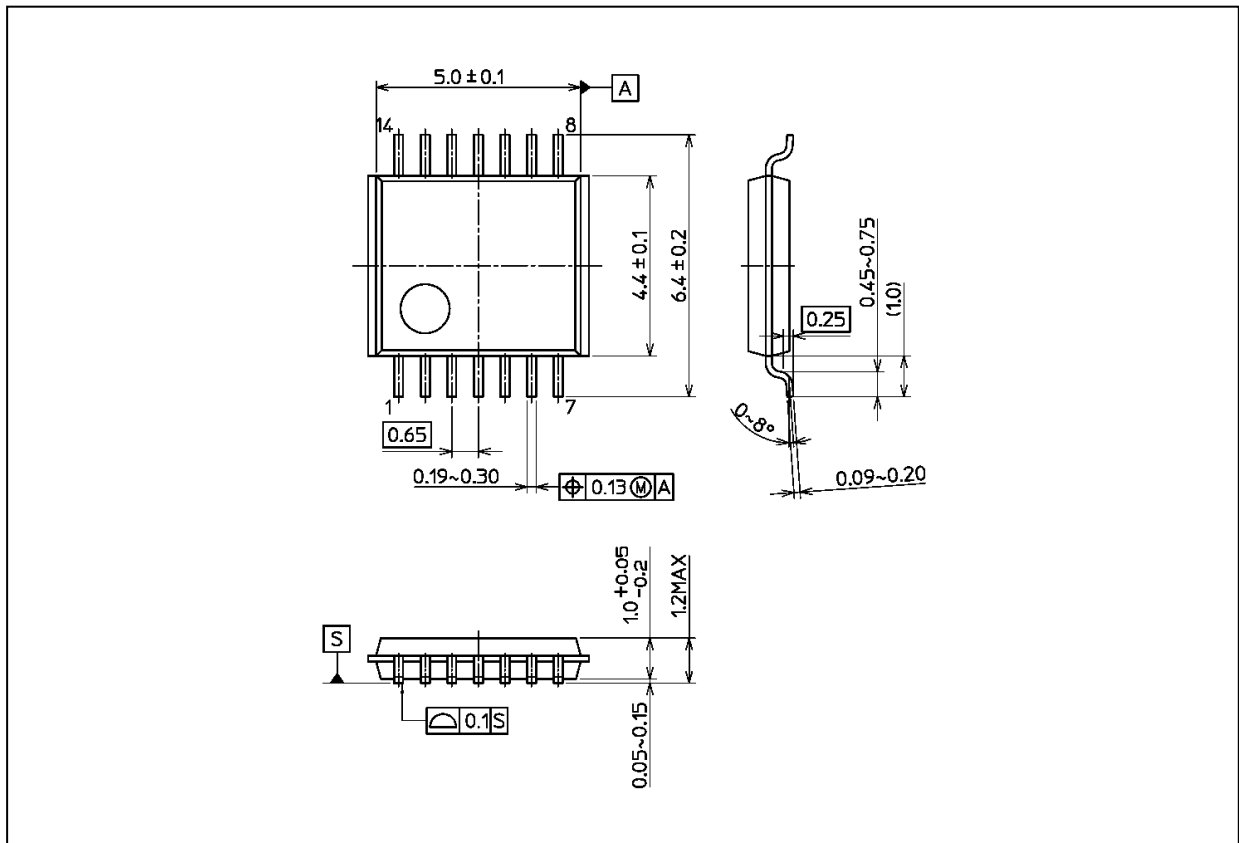
Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Limit	Unit
Quiet output maximum dynamic $V_{OL}$	$V_{OLP}$	$C_L = 50\text{ pF}$	5.0	0.3	0.8	V
Quiet output minimum dynamic $V_{OL}$	$V_{OLV}$	$C_L = 50\text{ pF}$	5.0	-0.3	-0.8	V
Minimum high-level dynamic input voltage	$V_{IHD}$	$C_L = 50\text{ pF}$	5.0	—	3.5	V
Maximum low-level dynamic input voltage	$V_{ILD}$	$C_L = 50\text{ pF}$	5.0	—	1.5	V

12.8. Input Equivalent Circuit



Package Dimensions

Unit: mm



Weight: 0.054 g (typ.)

Package Name(s)
Nickname: TSSOP14B

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