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ON Semiconductor®

FDB9503L-F085

P-Channel PowerTrench® MOSFET

- 40 V, - 110 A, 2.6 m Ω

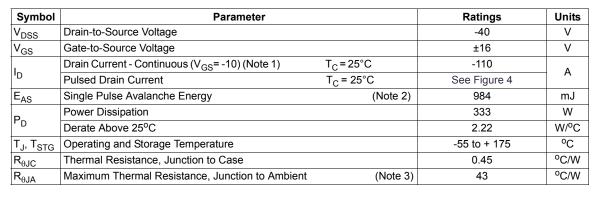
Features

- Typical $R_{DS(on)}$ = 2.0 m Ω at V_{GS} = 10V, I_D = 80 A
- Typical $Q_{q(tot)}$ = 196 nC at V_{GS} = -10V, I_D = -80 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems

MOSFET Maximum Ratings $T_J = 25$ °C unless otherwise noted.

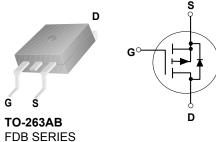


Notes:

- 1: Current is limited by wirebond configuration.
- 2: Starting T_J = 25°C, L = 0.3mH, I_{AS} = -81A, V_{DD} = -40V during inductor charging and V_{DD} = 0V during time in avalanche.
- 3: R_{0,JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,JC} is guaranteed by design, while R_{0,JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB9503L	FDB9503L-F085	TO-263AB	330mm	24mm	800 units





Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Cha	racteristics					

B _{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$		-40	-	-	V
1	Drain-to-Source Leakage Current	V _{DS} =-40V,	$T_{\rm J} = 25^{\rm o}{\rm C}$	-	-	-1	μΑ
DSS		$V_{GS} = 0V$	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	-	-1	mA
I _{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 16V, V_{DS} = 0V$		-	-	±100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$		-1.0	-1.8	-3.0	V
		$I_D = -80A$, $V_{GS} = -4.5V$, $T_J = 25^{\circ}C$		-	2.7	3.5	mΩ
R _{DS(on)}	Drain to Source On Resistance	I _D = -80A,	$T_{\rm J} = 25^{\rm o}{\rm C}$	-	2.0	2.6	mΩ
, ,		V _{GS} = -10V	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	2.9	3.7	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	\/ - 20\/ \/ -	0)/	-	8320	-	pF
C _{oss}	Output Capacitance	V_{DS} = -20V, V_{GS} = 0V, f = 1MHz		-	5620	-	pF
C _{rss}	Reverse Transfer Capacitance			-	102	-	pF
R_g	Gate Resistance	f = 1MHz		-	20	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0 \text{ to } -10V$	V _{DD} = -32V	-	196	255	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } -2V$	I _D = -80A	-	26	-	nC
Q_{gs}	Gate-to-Source Gate Charge		_	-	44	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge			Ī	22	ı	nC

Switching Characteristics

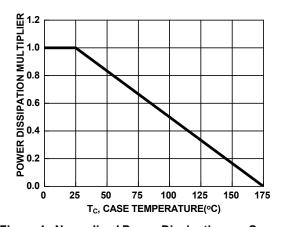
t _{on}	Turn-On Time		-	-	146	ns
t _{d(on)}	Turn-On Delay	V_{DD} = -20V, I_{D} = -80A, V_{GS} = -10V, R_{GEN} = 6 Ω	-	12	-	ns
t _r	Rise Time		-	86	-	ns
t _{d(off)}	Turn-Off Delay		-	700	-	ns
t _f	Fall Time		-	310	-	ns
t _{off}	Turn-Off Time		ı	ı	1538	ns

Drain-Source Diode Characteristics

TVos ISOUICE-IO-DISID DIONE VOITAGE	Occurs to Davis Diada Vallana	I _{SD} = -80A, V _{GS} = 0V	-	-	-1.25	V
	I _{SD} = -40A, V _{GS} = 0V	-	-	-1.2	V	
t _{rr}	Reverse-Recovery Time	$I_{SD} = -80A$, $dI_{SD}/dt = 100A/\mu s$,	-	124	186	ns
Q _{rr}	Reverse-Recovery Charge	V _{DD} = -32V	-	214	321	nC

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.



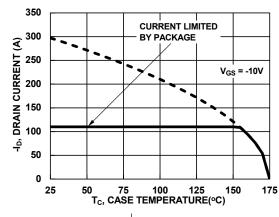
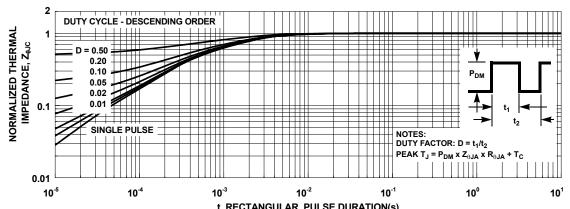


Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs. Case Temperature



t, RECTANGULAR PULSE DURATION(s)
Figure 3. Normalized Maximum Transient Thermal Impedance

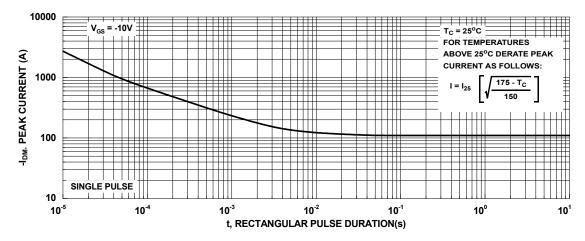


Figure 4. Peak Current Capability

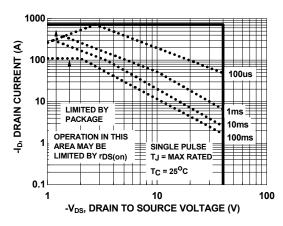
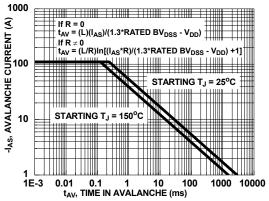


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

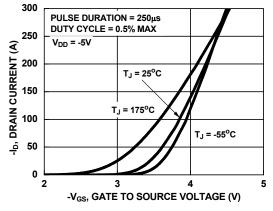


Figure 7. Transfer Characteristics

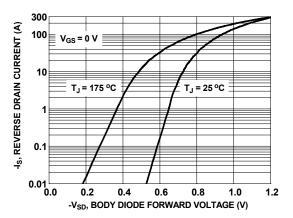


Figure 8. Forward Diode Characteristics

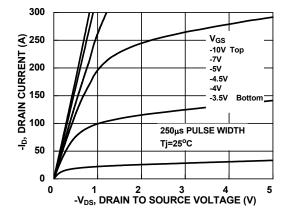


Figure 9. Saturation Characteristics

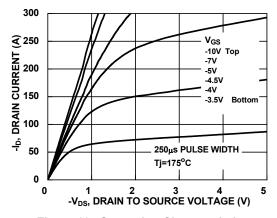


Figure 10. Saturation Characteristics

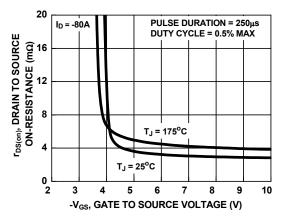


Figure 11. R_{DSON} vs. Gate Voltage

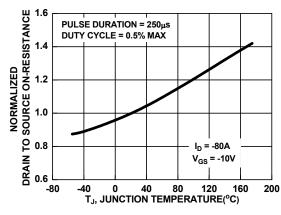


Figure 12. Normalized R_{DSON} vs. Junction Temperature

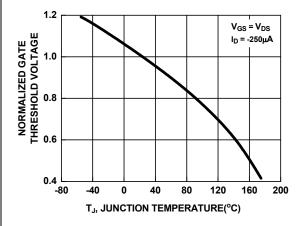


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

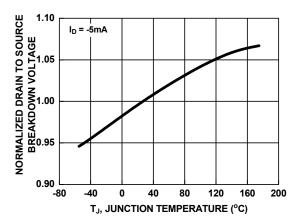


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

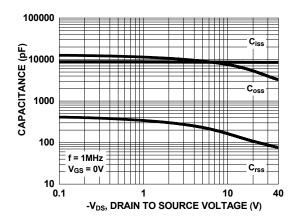


Figure 15. Capacitance vs. Drain to Source Voltage

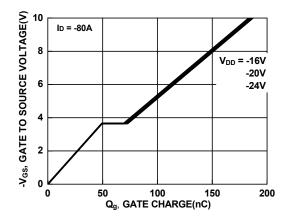


Figure 16. Gate Charge vs. Gate to Source Voltage

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