MP4569

75V, 0.3A Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP4569 is a step-down switching regulator with integrated high-side/low-side, high-voltage power MOSFETs. It provides a highly efficient output of up to 0.3A.

The wide 4.5V to 75V input range accommodates a variety of step-down applications in automotive environment. A 3.5μA shutdown mode quiescent current is good for battery-powered applications.

It allows for high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load condition to reduce the switching and gate driver losses.

The switching frequency during start-up and short circuit also can be scaled down to prevent inductor current runaway. Thermal shutdown provides reliable, fault-tolerant operation.

The MP4569 is available in QFN-10 (3mmx3mm) and SOIC-8 EP packages.

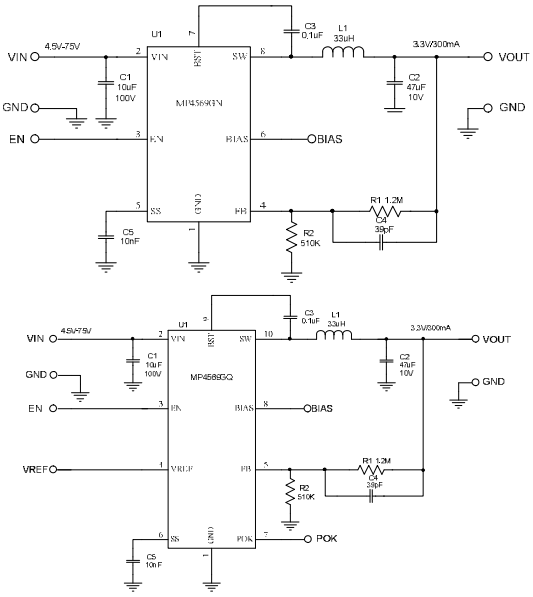
FEATURES

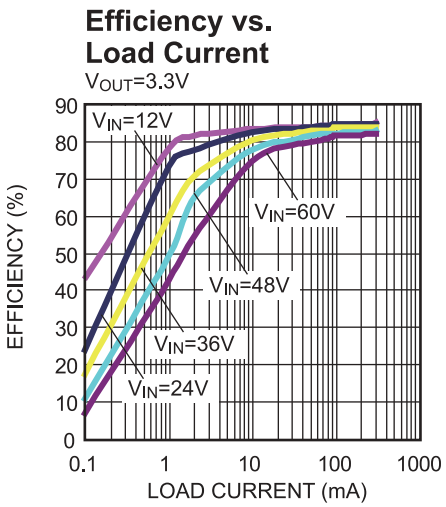
- 20μA Quiescent Current (Active mode)
- Wide 4.5V to 75V Operating Input Range
- 1.2Ω/0.45Ω Internal Power MOSFETs
- Programmable Soft-Start
- FB-Tolerance: 1% at Room Temperature; 2% at Full Temperature.
- Adjustable Output
- 1V Reference Voltage Output for QFN Package
- Low Shutdown Mode Current: 3.5μA
- Available in QFN-10 (3mmx3mm) and SOIC-8 EP Packages

APPLICATIONS

- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4569GQ	QFN-10 (3mmx3mm)	*See Below*
MP4569GN	SOIC-8 EP	*See Below*

*For Tape & Reel, add suffix –Z (e.g. MP4569GQ–Z)

TOP MARKING (QFN-10 (3mmx3mm))

AEXY
LLL

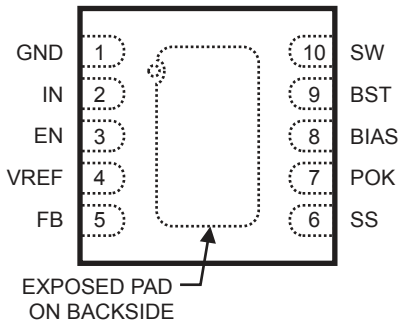
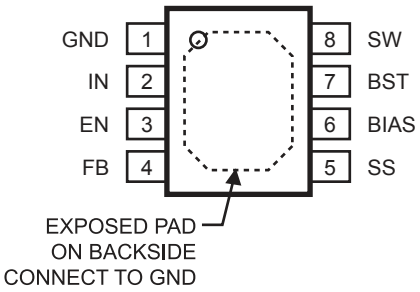
AEX: product code of MP4569GQ;
Y: year code;
LLL: lot number;

TOP MARKING (SOIC-8 EP)

MP4569
LLLLLLLL
MPSYWW

MP4569: part number;
MPS: MPS prefix:
Y: year code;
WW: week code:
LLLLLLLL: lot number;

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
QFN-10 (3mmx3mm)	**SOIC-8 EP**

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN}) …… ..... -0.3V to +80V
Switch Voltage (V_{SW}) …… …….-0.3V to V_{IN} + 1V
BST to SW…… ……-0.3 to +6.0V
All Other Pins…… …….-0.3V to +6.0V
EN Sink Current ……..……150μA
Continuous Power Dissipation (T_A = +25°C) (2)
QFN-10 (3mmx3mm)…….....2.5W
SOIC-8 EP ……..……..……2.6W
Junction Temperature…….……150°C
Lead Temperature …… .....……260°C
Storage Temperature……-65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} …… ..... 4.5V to 75V
Output Voltage V_{OUT} .. ……1V to 0.9xV_{IN}
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-10 (3mmx3mm) ……	50……	12…°C/W
SOIC-8 EP ……..……	48……	12…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 2V, T_J = 25°C, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
Supply Quiescent Current	No load, V_{FB}=1.2V		20	25	μA
Shutdown Supply Current	V_{EN} < 0.3V		2.2	3.5	μA
VIN UVLO Rising Threshold		3.9	4.2	4.4	V
VIN UVLO Falling Threshold		3.45	3.75	3.95	V
VIN UVLO Hysteresis			0.45		V
Feedback Voltage	V_{IN}=4V to 75V, -40°C<T_J<125°C	0.98	1	1.02	V
	V_{IN}=4V to 75V, T_J =25 °C	0.99	1	1.01	V
Feedback Current	V_{FB}=1.2V	-50	2	50	nA
VREF Pin Voltage(5)	V_{IN}=4V to 75V, I_{REF}=100μA	0.965	1	1.035	V
Upper Switch On Resistance	V_{BST}-V_{SW}=5V,	0.9	1.2	1.5	Ω
Lower Switch On Resistance	V_{BIAS}=5V,	0.275	0.45	0.625	Ω
Lower Switch Leakage	V_{EN} = 0V, V_{SW} = 75V			1	μA
Peak Current Limit		670	730	790	mA
Minimum Switch On Time(6)			120		ns
Enable Rising Threshold		1.4	1.55	1.7	V
Enable Falling Threshold		1.152	1.2	1.248	V
Enable Threshold Hysteresis			0.35		V
Enable Current	V_{EN}=2.4V		0.8		μA
Soft Start Current		4	5.5	7	μA
POK Upper Trip Threshold(5)	FB respect to the nominal value	86	90	94	%
POK Lower Trip Threshold(5)	FB respect to the nominal value	81	85	89	%
POK Threshold Hysteresis(5)	FB respect to the nominal value		5		%
POK Deglitch Timer(5)			40		μs
POK Output Voltage Low (5)	I_{SINK} = 1mA			0.4	V
FB OVP Rising Threshold			1.05	1.1	V
FB OVP Hysteresis			50		mV
Thermal Shutdown(6)			175		°C
Thermal Shutdown Hysteresis(6)			20		°C

Notes:

5) QFN package only.
6) Derived from bench characterization. Not tested in production.

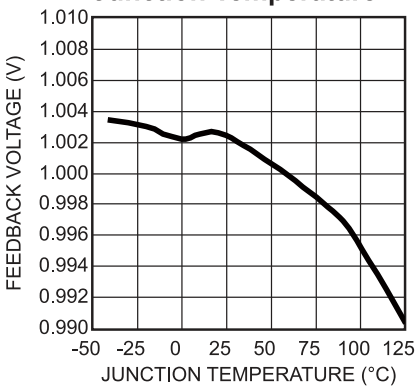
PIN FUNCTIONS

Pin # QFN-10 (3mmx3mm)	Pin # SOIC-8 EP	Name	Description
1	1	GND	Ground. Connected the output capacitor as close as possible to avoid high-current switch paths.
2	2	IN	Input Supply. Requires a decoupling capacitor to ground to reduce switching spikes.
3	3	EN	Enable Input. Pull this pin below the low threshold to shut the chip down. Pull it above the high threshold enables the chip. Float this pin to shut the chip down.
4	No Bonding	VREF	Reference Voltage Output, for QFN-10 (3mmx3mm) package only.
5	4	FB	Feedback Connected to the tap of an external resistive divider between the output and GND. Sets the regulation voltage when compared to the internal 1V reference.
6	5	SS	Soft-Start Control Input. Connect a capacitor from SS to GND to set the soft-start period.
7	No Bonding	POK	Open Drain Power Good Output. “HIGH” output indicates VOUT is higher than 90% of reference. POK is pulled down in shutdown, for QFN-10 (3mmx3mm) package only
8	6	BIAS	Controller Bias Input. Supplies current to the internal circuit when V_{BIAS}>2.9V.
9	7	BST	Bootstrap. Positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.
10	8	SW	Switch Node.

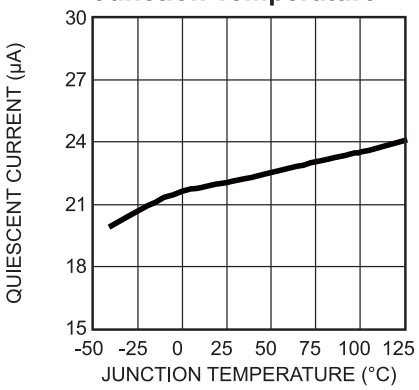
TYPICAL CHARACTERISTICS

V_{IN}=12V, unless otherwise noted.

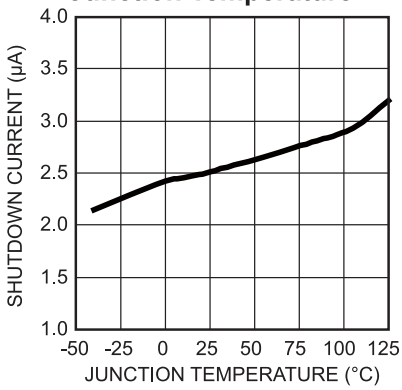
Feedback Voltage vs. Junction Temperature



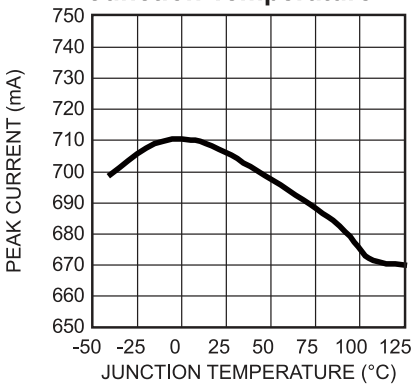
Quiescent Current vs. Junction Temperature



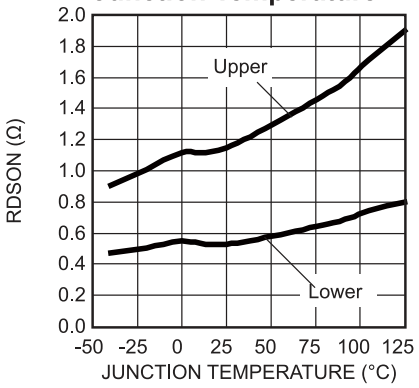
Shutdown Current vs. Junction Temperature



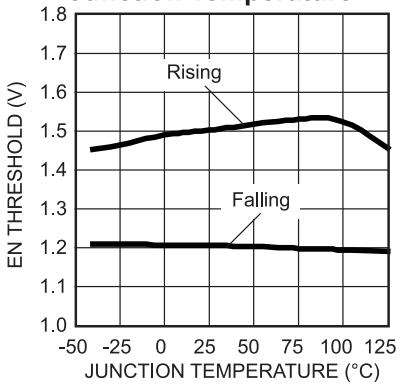
Current Limit vs. Junction Temperature



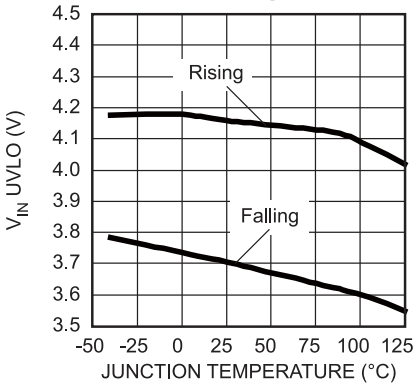
Switch ON Resistance vs. Junction Temperature



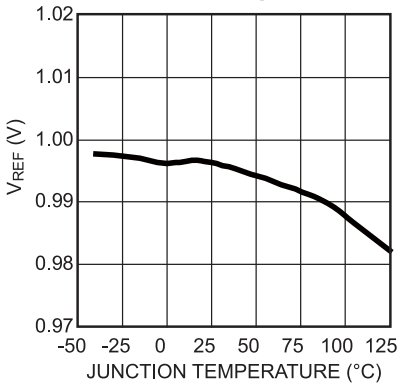
EN Threshold vs. Junction Temperature



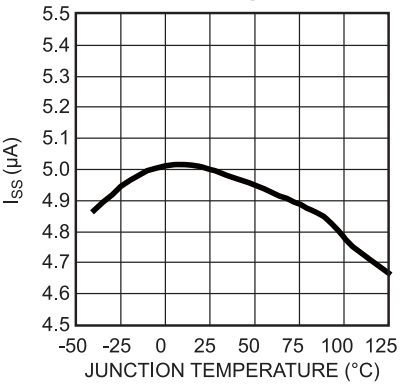
V_{IN} UVLO vs. Junction Temperature



V_{REF} vs. Junction Temperature



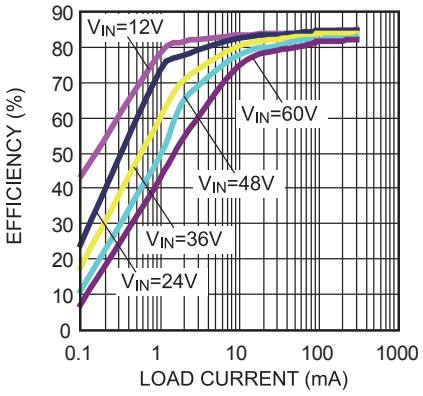
I_{SS} vs. Junction Temperature



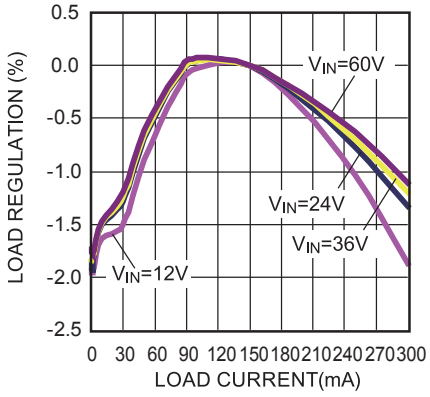
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 33µH, C_{OUT}=2x22µF, T_A = +25°C, unless otherwise noted.

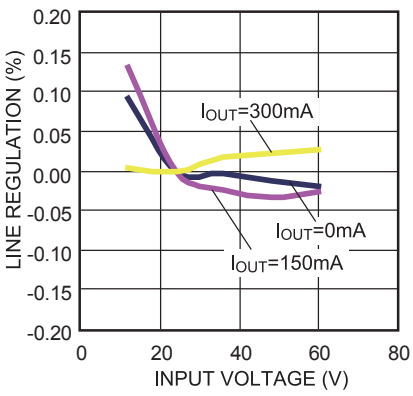
Efficiency vs. Load Current



Load Regulation

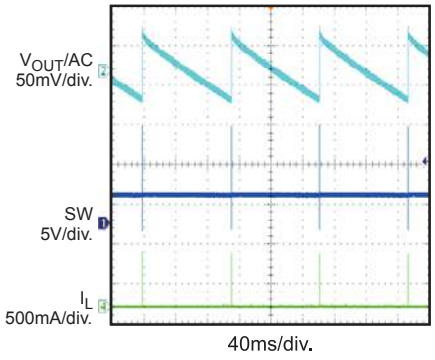


Line Regulation



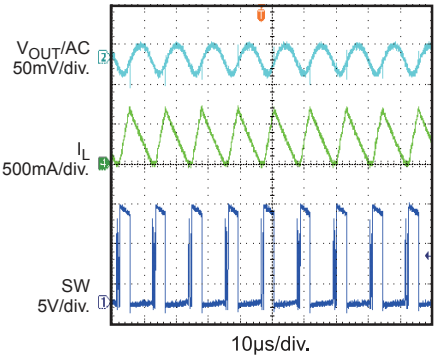
Steady State

I_{OUT}=0A



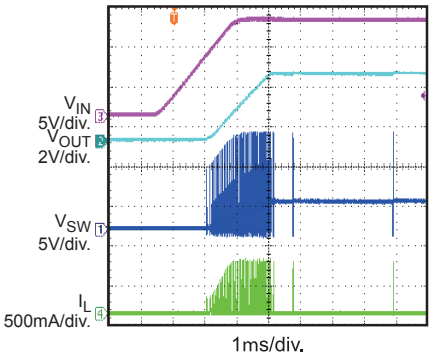
Steady State

I_{OUT}=0.3A



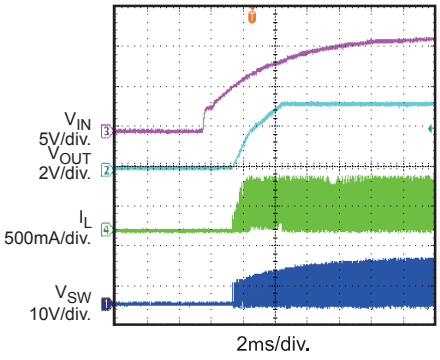
Startup Through V_{IN}

I_{OUT} = 0A



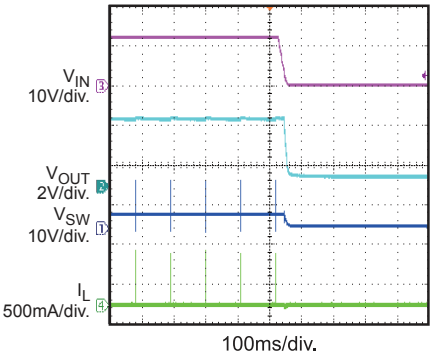
Startup Through V_{IN}

I_{OUT} = 0.3A



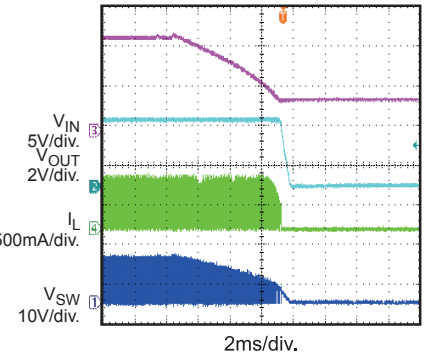
Shutdown Through V_{IN}

I_{OUT} = 0A



Shutdown Through V_{IN}

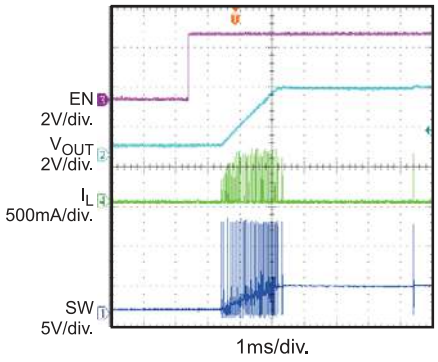
I_{OUT} = 0.3A



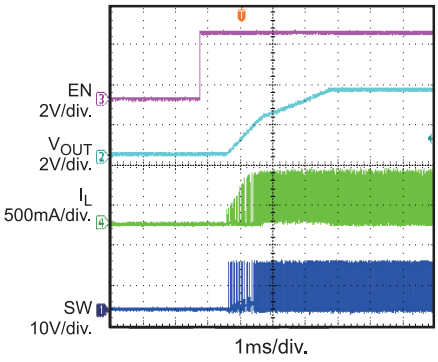
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 33µH, C_{OUT}=2x22µF, T_A = +25°C, unless otherwise noted.

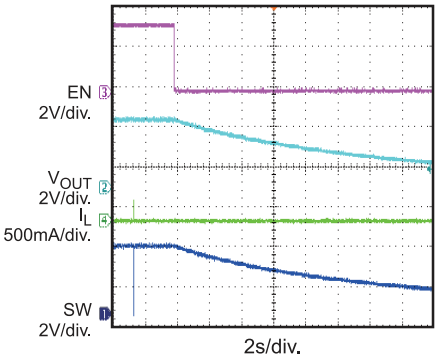
Startup Through EN
I_{OUT} = 0A



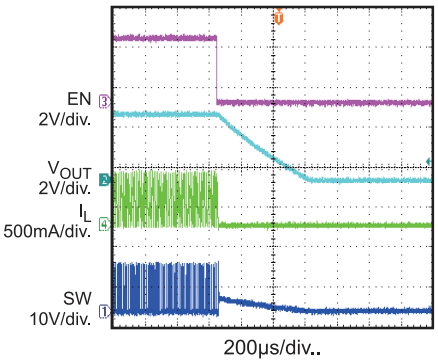
Startup Through EN
I_{OUT} = 0.3A



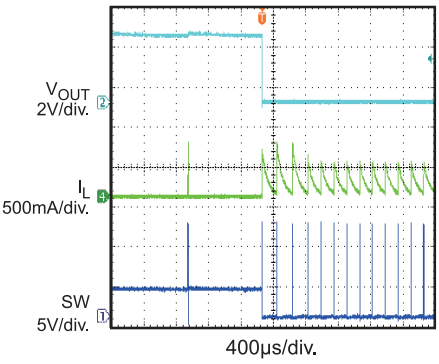
Shutdown Through EN
I_{OUT}=0A



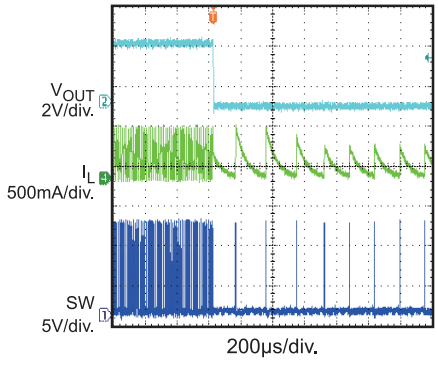
Shutdown Through EN
I_{OUT}=0.3A



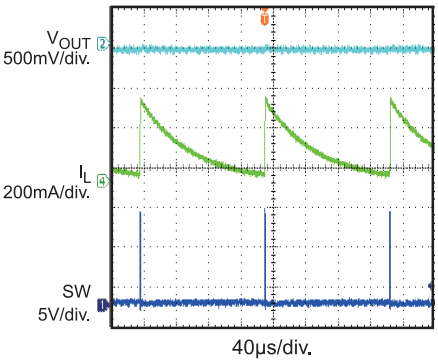
SCP Entry
I_{OUT}=0A to Short Circuit



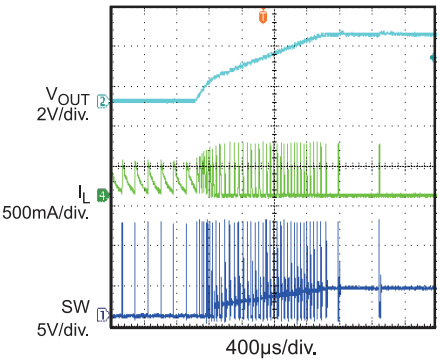
SCP Entry
I_{OUT}=0.3A to Short Circuit



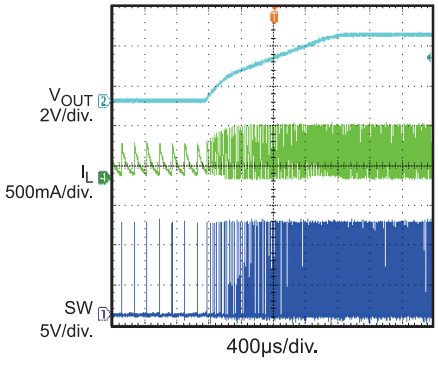
SCP Steady State



SCP Recovery
Short Circuit to I_{OUT}=0A



SCP Recovery
Short Circuit to I_{OUT}=0.3A



FUNCTIONAL BLOCK DIAGRAM

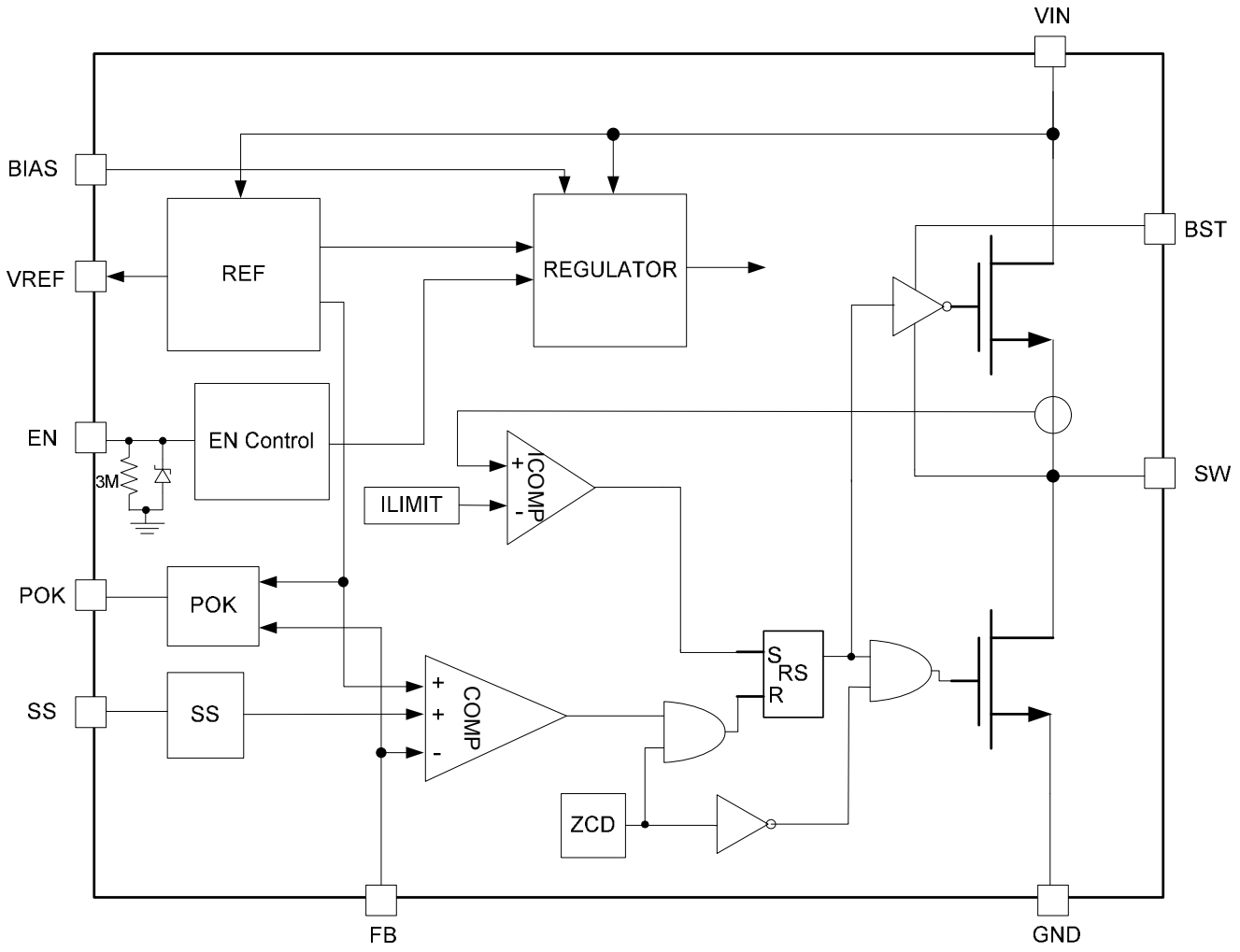


Figure 1 - Functional Block Diagram

OPERATION

The MP4569 is a 75V, 0.3A, synchronous, step-down switching regulator with integrated high-side and low-side high-voltage power MOSFETs (HS_FET and LS_FET, respectively). It provides a highly-efficient, 0.3A output. It features a wide input voltage range, external soft-start control, and precision current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

Control Scheme

The ILIM comparator, FB comparator and zero current detector (ZCD) block control the PWM. If V_{FB} is below the 1V reference and the inductor current drops to zero, HS_FET turns on and the ILIM comparator starts to sense the HS_FET current: When the HS_FET current reaches the limit, the HS_FET turns off and LS_FET turns on together with the ZCD block. Meanwhile, the ILIM comparator is turned off to reduce the quiescent current. The LS_FET turns off together with ZCD block after the inductor current drops to zero. If V_{FB} is less than the 1V reference at this time, the HS_FET turns on at once and commences another cycle. If V_{FB} is still higher than 1V reference, HS_FET would not turn on till V_{FB} drops below 1V.

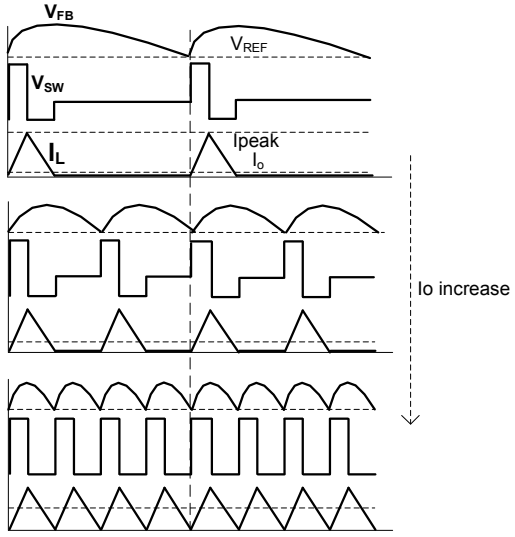


Figure2 - Control Scheme

Internal Regulator and BIAS

The 2.6V internal regulator powers most of the internal circuitry. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} is greater than 3.0V, the output of the regulator is in full regulation. Lower values of V_{IN} result in lower output voltages. When V_{BIAS}>2.9V, the bias supply overrides the input voltage and supplies power to the internal regulator. When V_{BIAS}>4.5V, it can power LS_FET driver furthermore. Using BIAS to power internal regulator can improve the efficiency. It is recommended to connect BIAS to the regulated output voltage when it is in the range of 2.9V to 5.5V. When output voltage is out of above range, an external supply that is >2.9V or even better >4.5V can be used to power BIAS.

Enable Control

The MP4569 has a dedicated enable-control pin, EN: when V_{IN} goes high, the EN pin enables and disables the chip. This is HIGH logic. Its trailing threshold is a consistent 1.2V. Its rising threshold is about 350mV higher. When floating, EN pin is internally pulled down to GND to disable the chip.

When EN = 0V, the chip goes into the lowest shutdown-current mode. When EN is higher than zero but lower than its rising threshold, the chip remains in shutdown mode with a slightly larger shutdown current.

Internally a zener diode is connected from EN pin to GND pin. The typical clamping voltage of the zener diode is 6.5V. So VIN can be connected to EN through a high ohm resistor if the system doesn't have another logic input acting as enable signal. The resistor needs to be designed to limit the EN pin sink current less than 150μA. Just note that there is an internal 3M resistor from EN to GND, so the external pull up resistor should be smaller than $\frac{[V_{IN(MIN)} - 1.55V] \times 3M}{1.55V}$ to make sure the part can EN on at the lowest operation VIN.

Under-Voltage Lockout

V_{IN} under voltage lockout (UVLO) protects the chip from operating below the operational supply voltage range. The UVLO-rising threshold is about 4.2V while its trailing threshold is about 3.75V.

Soft-start

Reference-type soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a constant current to charge external SS capacitor. The soft-start (SS) voltage slowly ramps up from 0V at a slow pace set by the soft-start time. When V_{SS} is less than the V_{REF}, V_{SS} overrides V_{REF} so the FB comparator uses V_{SS} instead of V_{REF} as the reference. When V_{SS} is higher than V_{REF}, V_{REF} resumes control.

V_{SS} is also associated with V_{FB}. Though V_{SS} can be much smaller than V_{FB}, it can only barely exceed V_{FB}. If somehow V_{FB} drops, V_{SS} tracks V_{FB}. This function prevents output voltage overshoot in short-circuit recovery -- when the short circuit is removed, the SS ramps up as if it is a fresh soft-start process.

Thermal Shutdown

Thermal shutdown prevents the chip from thermally running away. When the silicon die temperature exceeds its upper threshold, the thermal shutdown feature shuts down the whole chip. When the temperature falls below its lower threshold, the chip resumes function.

Floating Driver and Bootstrap Charging

The external bootstrap capacitor powers the floating HS_FET driver. This floating driver has its own UVLO protection, with a rising threshold of about 2.4V with a hysteresis of about 300mV. During this UVLO, the SS voltage resets to zero. When the UVLO is disabled, the regulator follows the soft-start process.

The dedicated internal bootstrap regulator charges and regulates the bootstrap capacitor to about 5V. When the voltage difference between BST and SW falls below its working parameters, a PMOS pass transistor connected from V_{IN} to BST turns on to charge the bootstrap capacitor. The current path is from V_{IN} to BST and then to SW. The external circuit must have enough voltage headroom to accommodate charging.

As long as V_{IN} is sufficiently higher than SW, the bootstrap capacitor can charge. When the HS_FET is ON, V_{IN} is about equal to SW so the bootstrap capacitor cannot charge. The best charging period occurs when the LS_FET is on so that V_{IN} - V_{SW} is at its largest. When there is no current in the inductor, V_{SW} equals V_{OUT} so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor.

If the internal circuit does not have sufficient voltage and time to charge the bootstrap capacitor, extra external circuitry can be used to ensure the bootstrap voltage in normal operation region.

Startup and Shutdown

If both V_{IN} and V_{EN} are higher than their appropriate thresholds, the chip starts operating. The reference block starts first, generating stable reference voltage and currents, and then enables the internal regulator. The regulator provides stable supply for the rest device.

While the internal supply rail is high, an internal timer holds the power MOSFET off for about 50μsec to blank startup glitches. When the soft-start block is enabled, it first holds its SS output low and then slowly ramps up.

Three events shut down the chip: V_{EN} low, V_{IN} low, and junction temperature triggers the thermal shutdown threshold. For shutdown, the signaling path is blocked first to avoid any fault triggering. Internal supply rail are pulled down then. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power OK (POK)

POK is an open drain power good output. “HIGH” output indicates VOUT is higher than 90% of its nominal value. POK is pulled down in shutdown mode.

Reference Voltage Output (VREF)

VREF pin output 1V reference voltage. It has up to 500uA source current capability.

APPLICATION INFORMATION

Selecting the Inductor

As the Ipeak is fixed, for given input voltage and output voltage, the inductor value can be determined by the following formula:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times I_{peak} \times f_s}$$

Where fs is the switching frequency at the maximal output current.

Larger inductor value results in lower switching frequency, as well as higher efficiency. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current as well as the slow load transient dynamic performance. There is also a lower limit of the inductor value, which is determined by the minimum on time. In order to keep the inductor working under control, the inductor value should be chosen higher than Lmin that is derived from below formula:

$$L_{MIN} = \frac{V_{IN(MAX)} \times t_{ON(MIN)}}{I_{peak}}$$

Where $V_{IN(MAX)}$ is the max value of input voltage. $t_{ON(MIN)}$ is the 120ns minimum switch on time.

Switching Frequency

Switching frequency can be estimated by below equation.

$$f_s = \frac{2 \times Io \times V_{OUT} \times (V_{IN} - V_{OUT})}{I_{peak}^2 \times V_{IN} \times L}$$

Larger inductor can get lower fs. And fs increases as Io increasing. When Io increases to its maximal value Ipeak/2, fs also reaches its highest value and can be derived by:

$$f_{s(max)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{peak} \times V_{IN} \times L}$$

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. As shown in figure 3.

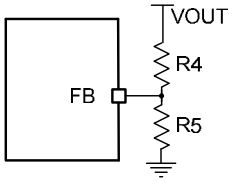


Figure 3 – Adjustable V_{OUT} by divider resistors

To get the desired output voltage, divider resistor can be chosen through below formula:

$$\frac{R4}{R5} = \frac{V_{OUT}}{V_{REF}} - 1$$

Where V_{REF} is the FB reference voltage 1V.

The current flows into divider resistor would increase the supply current, especially at no load and light load condition. The Vin supply current caused by the feedback resistors can be calculated from:

$$I_{IN\_FB} = \frac{V_{OUT}}{R4 + R5} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta}$$

Where η is the efficiency of the regulator.

To reduce this current, resistors in the megohm range are recommended. The recommended value of the feedback resistors are shown in Table 1.

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R4 (kΩ)	R5 (kΩ)
3.3	1200	523
5	1200	300

Under Voltage Lock Out Point Setting

MP4569 has internal fixed under voltage lock out (UVLO) threshold: rising threshold is about 4.2V while trailing threshold is about 3.75V. External resistor divider between EN and VIN as shown in Figure 4 can be used to get higher equivalent UVLO threshold.

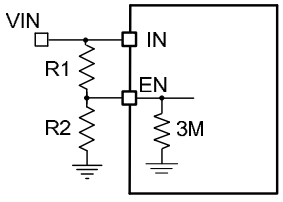


Figure 4 – Adjustable UVLO using EN pin

The UVLO threshold can be computed from below two equations.

$$UVLO_{TH\_Rising} = (1+\frac{R1}{3M//R2})\times EN_{TH\_Rising}$$

$$UVLO_{TH\_Falling} = (1+\frac{R1}{3M//R2})\times EN_{TH\_Falling}$$

Soft Start Capacitor

The soft start time is the duration when SS is charged from 0 to FB reference voltage 1V by an internal 5μA current source. So the capacitor at SS pin can be chosen according to below formula:

$$C_{SS} = 5\times t_{SS}(\mu F)$$

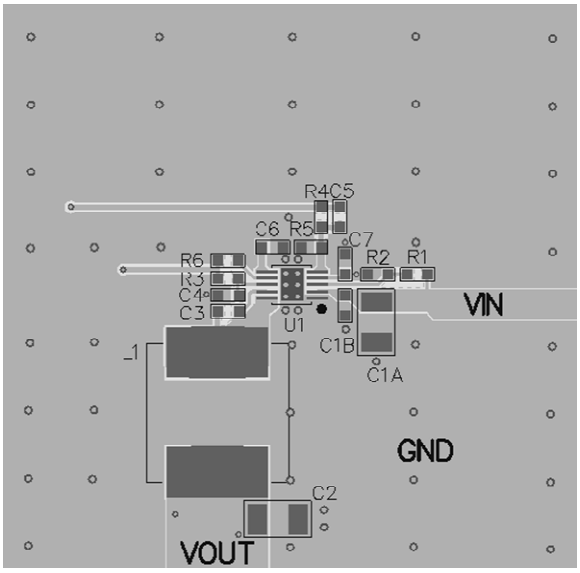
Feed-Forward Capacitor

As described above that the PWM control scheme of MP4569 is very special and the HS_FET turns on when FB drops lower than reference voltage. This brings good load transient performance. However, this also makes the HS_FET turn on moment is very sensitive to the FB voltage. Once there is noise on FB, the moment HS_FET turns on is easy to be affected, and then Fsw jitter would occur. The Fsw jitter is easy to happen especially when Vo ripple is very small. To improve the jitter performance, a small feedforward capacitor between Vo and FB can be used and typical 39pF is recommended.

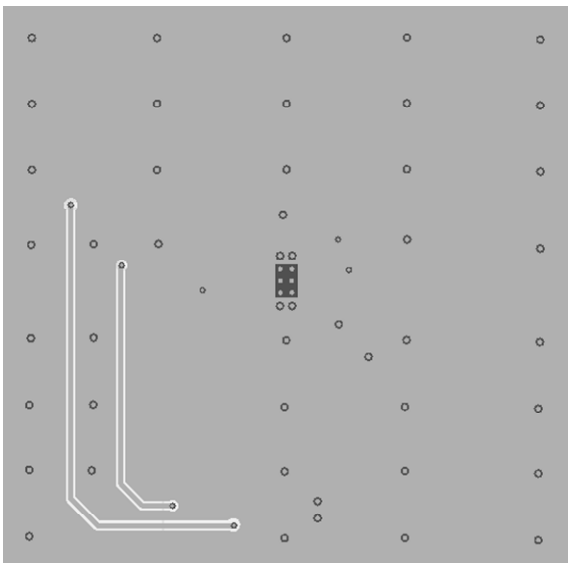
PCB Layout

PCB layout is very important to achieve stable operation. Please follow below guidelines and use Figure 5 as reference.

1) Keep the path of switching current short and minimize the loop area formed by input capacitor, high-side, low-side MOSFET and output capacitor.
2) Bypass ceramic capacitors should be as close as possible to the VIN pin.
3) Make sure that all feedback connections are short and direct. Place the feedback resistors as close to the chip as possible.
4) Keep SW away from sensitive analog areas such as FB.
5) For better thermal performance and long-term reliability consideration, VIN, SW and GND should be connected to a large copper area respectively to cool the chip.

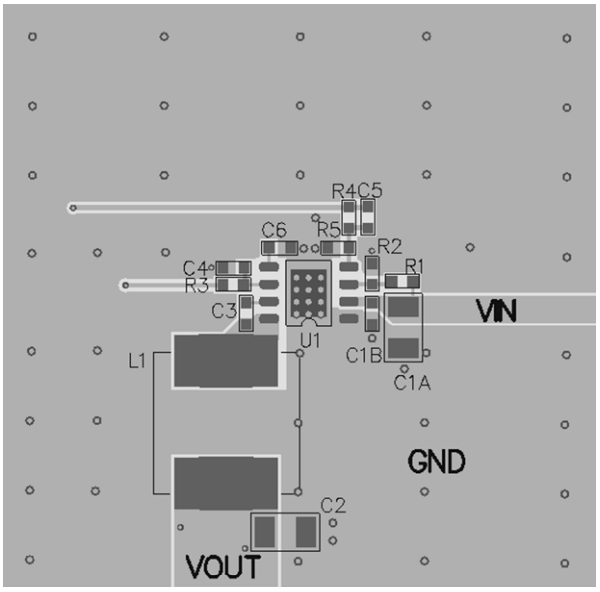


Top Layer



Bottom Layer

(a) Layout Reference of QFN-10 Package(7)



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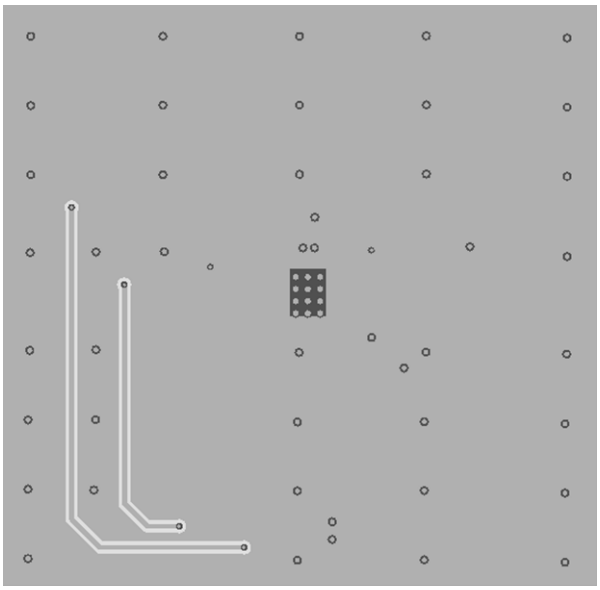

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(b) Layout Reference of SOIC-8 EP Package(8)

Figure 5 – Layout Reference

Notes:

7) Take Figure 6 as schematic
8) Take Figure 7 as schematic

TYPICAL APPLICATION CIRCUITS

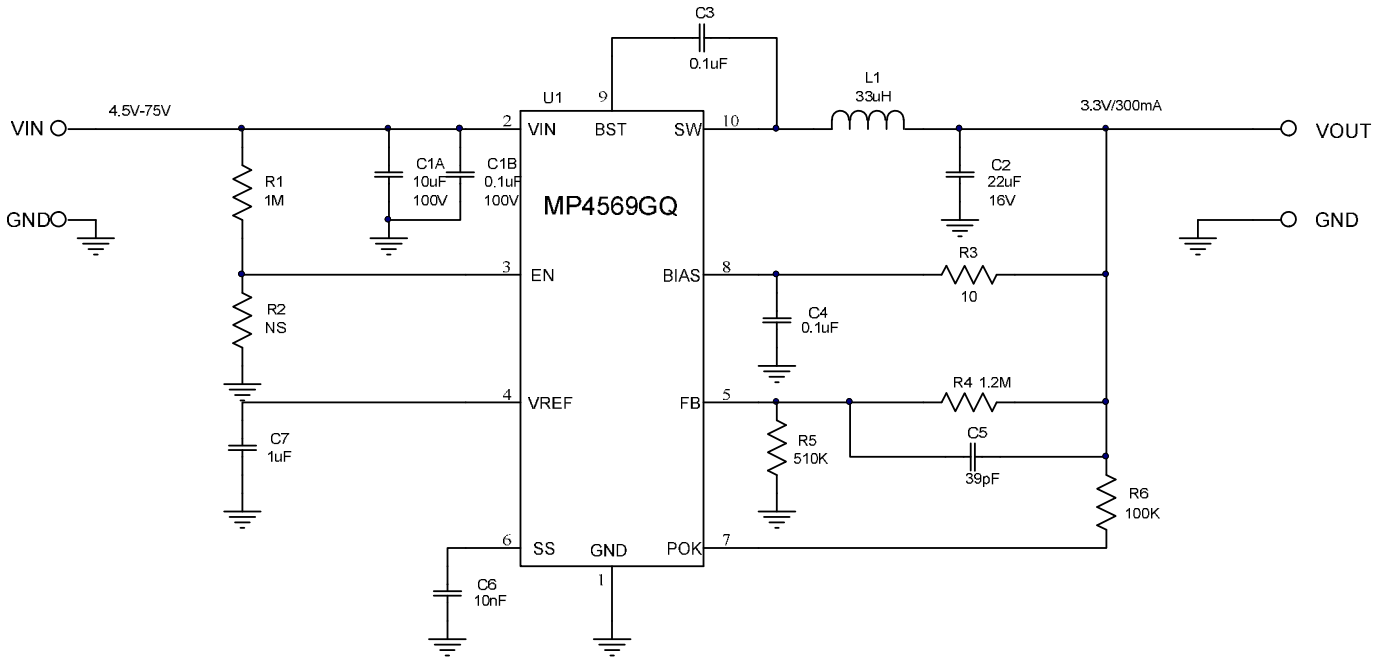


Figure 6 – 3.3V Output Typical Application Circuit of QFN-10 Package

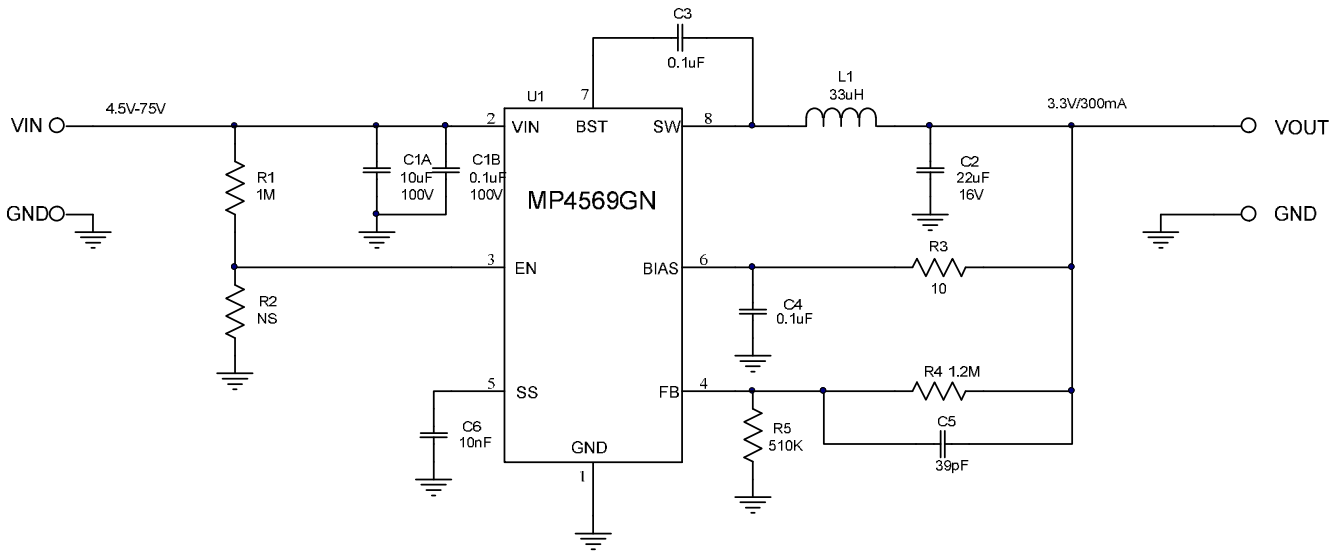
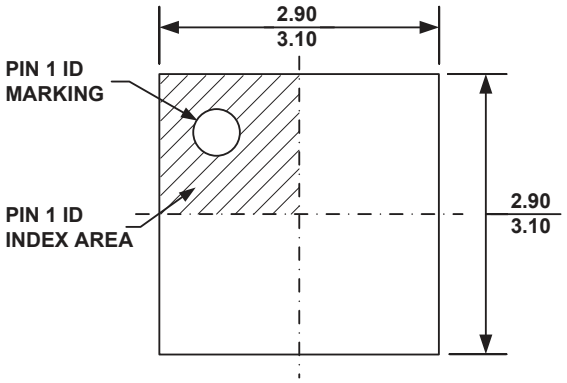


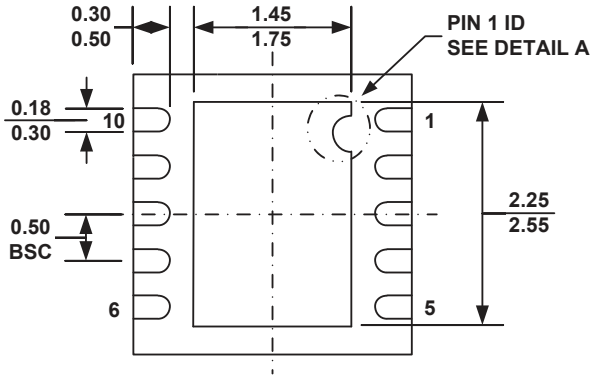
Figure 7 – 3.3V Output Typical Application Circuit of SOIC-8 EP Package

PACKAGE INFORMATION

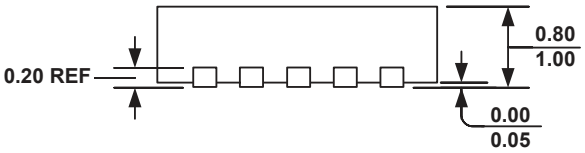
QFN-10 (3mmx3mm)



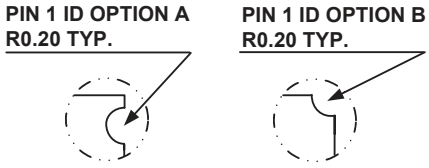
TOP VIEW



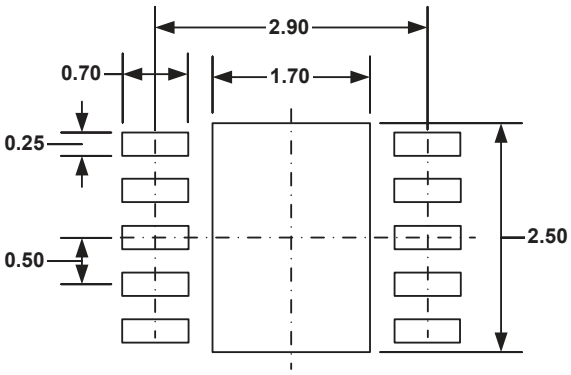
BOTTOM VIEW



SIDE VIEW



DETAIL A



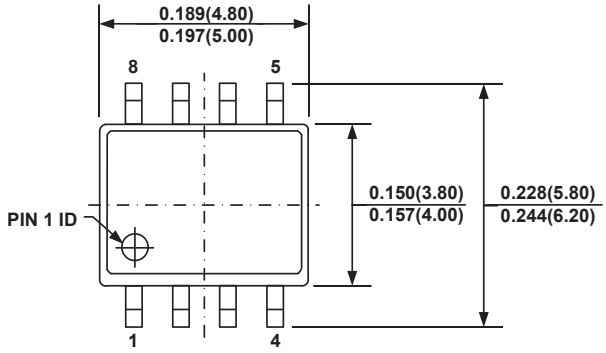
RECOMMENDED LAND PATTERN

NOTE:

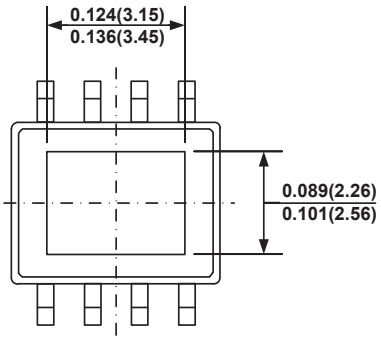
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

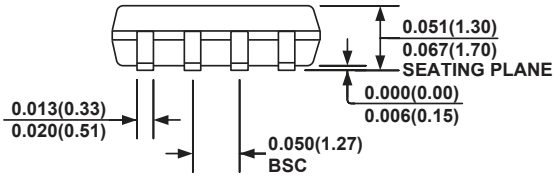
SOIC-8 EP



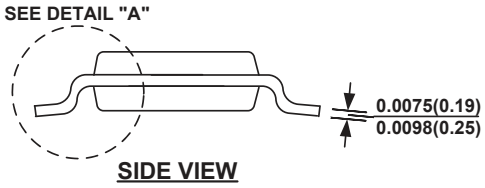
TOP VIEW



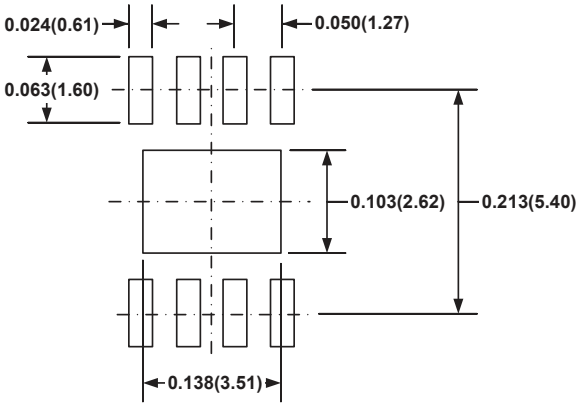
BOTTOM VIEW



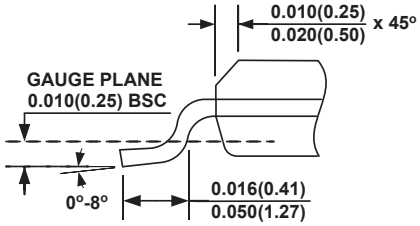
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.