Introduction

This document provides a guide on how to configure the 8V49NS0312 Rev. B evaluation board. The board can be configured through I2C, which offers complete control of the device features, or through tri-level pin selections which offers the most popular configurations. When the board is connected to a PC running IDT Timing Commander™ Software through USB, the device can be configured and programmed to generate frequencies with best-in-class performances.

Shipping Contents

The 8V49NS0312 evaluation board ships with the following:

- (1) 8V49NS0312 Evaluation Board

Requirements

1. Power supply with 3.3V and/or 5V output and 1000mA rating.
2. Two banana plug cables to connect the power supply to the board.
3. Optional for I2C programming:

   PC Requirements:
   - IDT Timing Commander Software installed
   - Windows XP SP3 or later
   - Processor: Minimum 1GHz
   - Memory: Minimum 512MB, recommended 1GB
   - Available Disk Space: Min 600MB (1.5GB 64bit), recommended 1GB (2GB 64bit)
   - Network access during installation if the .NET framework is not currently installed on the system

Contents

Quick Start: Power Up the Board

1. Configure the lab power supply to 3.3V with a 700mA limit. Turn off the output.
2. Set POWER_SEL (JP21) to select VCC_INPUT.
3. Remove all output terminations.
4. Set Dip Switch selectors to the positions shows in Figure 1.
5. Connect VEE to the GND jack (J22).
6. Connect the 3.3V source to POWER (J90).
7. Turn on the power supply. The current should measure ~503mA.

Optional (for I2C programming through Timing Commander).

8. Connect a cable from a PC to the USB port.

Once correct operation is verified, set the power supply limit for the number of outputs to be active.

The board ships with a 50MHz crystal and with the DIP Switch settings from Figure 1 it will be configured as follows:

QA1 = QA2 = 156.25MHz, LVDS levels

QB1 = QB2 = 156.25MHz, LVPECL levels

QC0 = QC1 = 125MHz, LVDS levels

QD0 = 125MHz, LVDS levels

QD1 = High Impedance

When evaluating performance with the default hardware configuration, it is recommended that all active outputs be terminated 50Ω to GND by either terminator plugs or an instrument.

Bank A: This device supports four outputs for bank A, but only QA1 and QA2 have been routed. This bank's termination is configured for LVDS operation and will not switch if set to LVPECL levels unless the terminations are modified. For LVPECL operation, consult the Output Configuration section of this document.

Bank B: This device supports four outputs for bank A, but only QB1 and QB2 have been routed. This bank's termination is configured for LVPECL operation. For LVDS operation, consult the Output Configuration section of this document.

Bank C: This bank's termination is configured for LVDS operation and will not switch if set to LVPECL levels unless the terminations are modified. For LVPECL operation, consult the Output Configuration section of this document.

Bank D: QD0 is terminated for LVDS operation and will not switch if set to LVPECL levels unless the terminations are modified. For LVPECL operation, consult the Output Configuration section of this document.

Board Overview

Use Figure 1 and Table 1 to identify: power supply jacks, USB connector, input and output SMA connectors, DIP switches, and other board elements.

Figure 1. Evaluation Board Overview

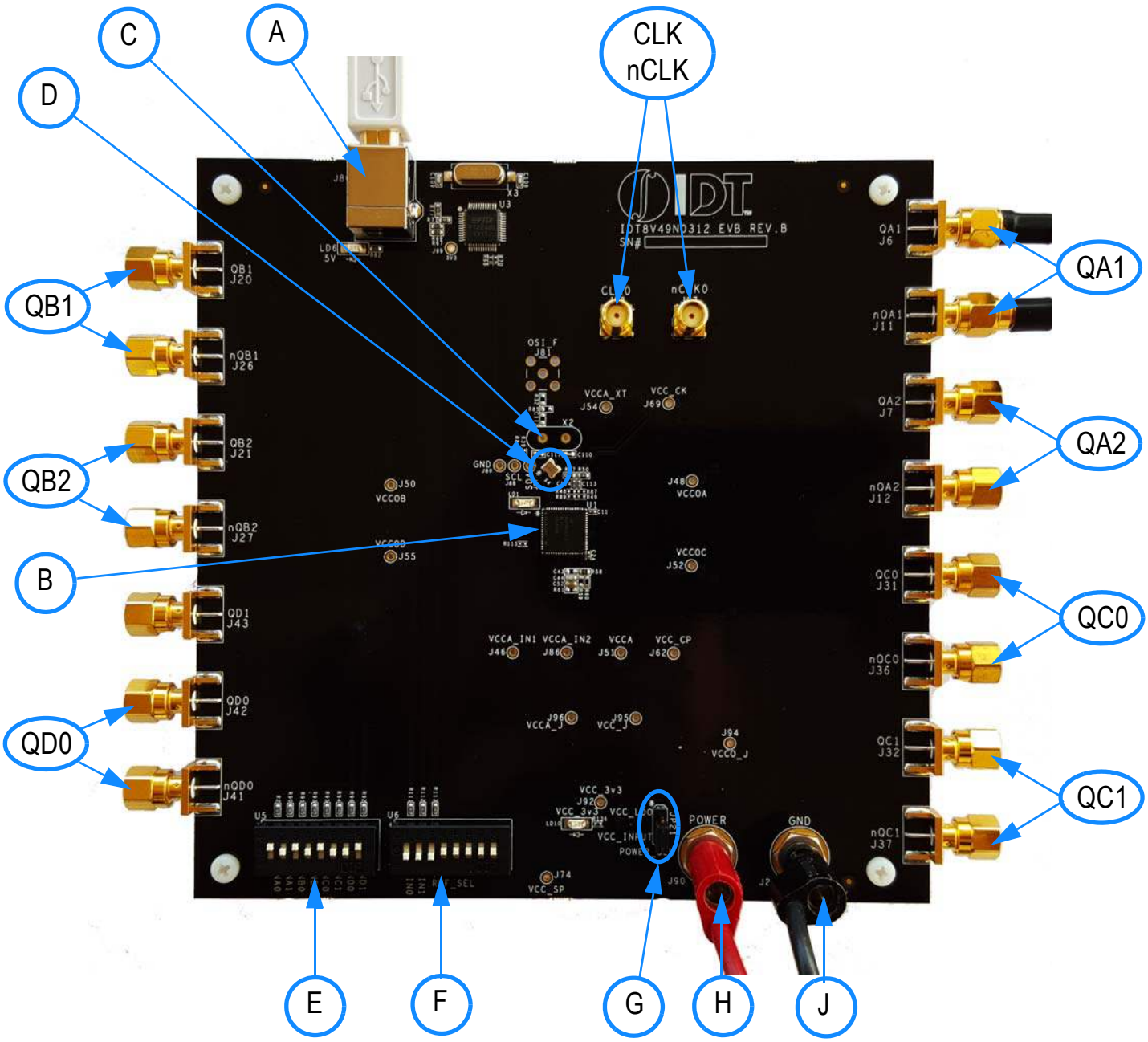
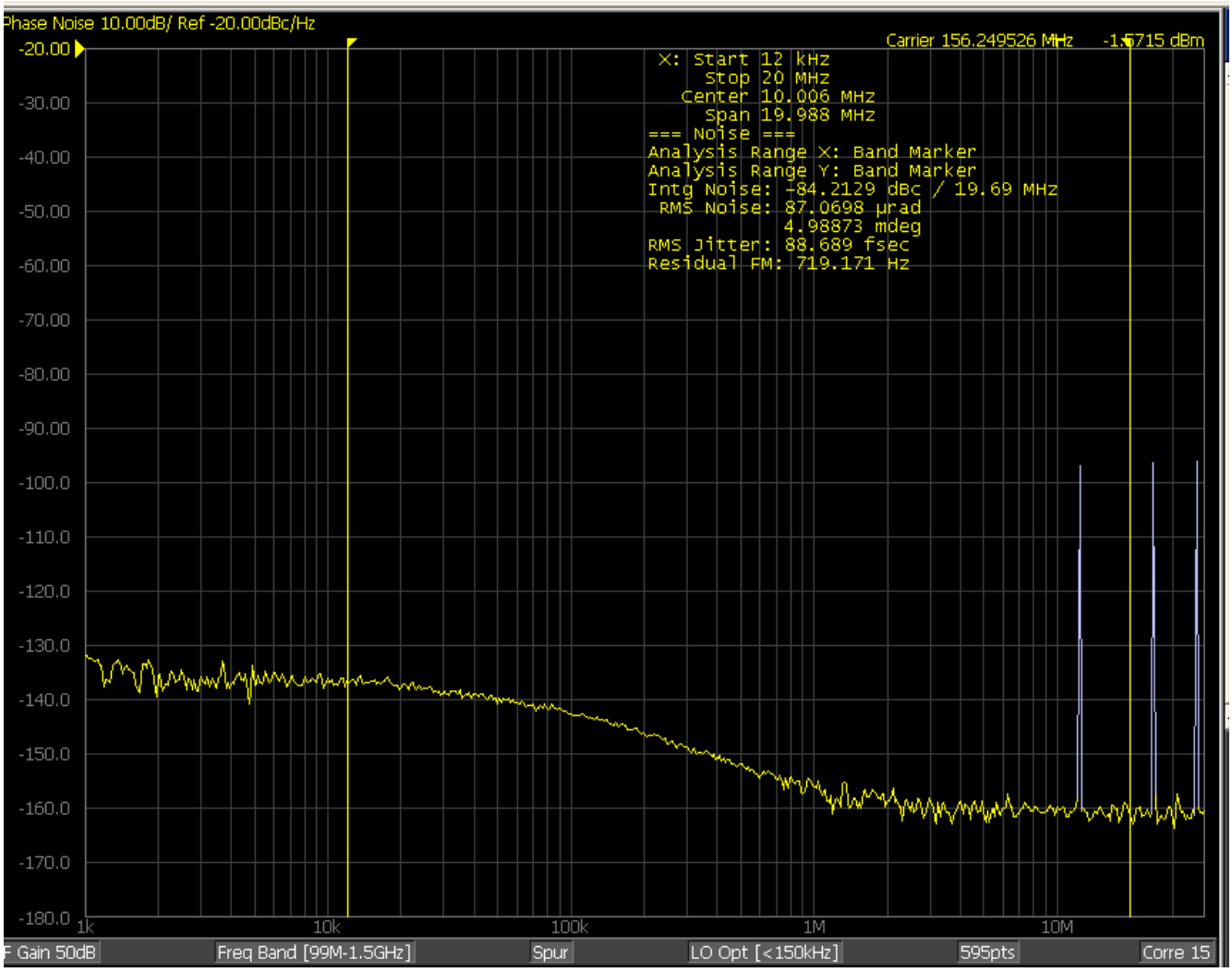


Table 1. Evaluation Board Legend

Inputs	Description
CLK	Clock input line. Can be configured for differential or single-ended input.
nCLK	nClock input line.
Outputs	**Description**
QA1	Can be configured for either LVPECL or LVDS output levels.
QA2	Can be configured for either LVPECL or LVDS output levels.
QB1	Can be configured for either LVPECL or LVDS output levels.
QB2	Can be configured for either LVPECL or LVDS output levels.
QC0	Can be configured for either LVPECL or LVDS output levels.
QC1	Can be configured for either LVPECL or LVDS output levels.
QD0	Can be configured for either LVPECL or LVDS output levels.
QD1	Single-ended LVCMOS output.
Other	**Description**
A	USB connector.
B	8V49NS0312- the device to be evaluated.
C	Through-hole HC-49 crystal socket (optional).
D	SMD 50MHz crystal.
E	Dip Switch for DC control signals (NAx, NBx, NCx, NDx).
F	Dip Switch for DC control signals (FINx, REF_SEL).
G	Power select (default is 3.3V input).
H	Power jack.
J	Ground jack.

Typical Performance

Figure 2. Default Configuration, Phase Noise on QA1



Schematics

The following figures are schematics that are applicable to specific sections of this user guide. The complete schematics are available in a separate document.

Figure 3. Input CLK Schematic

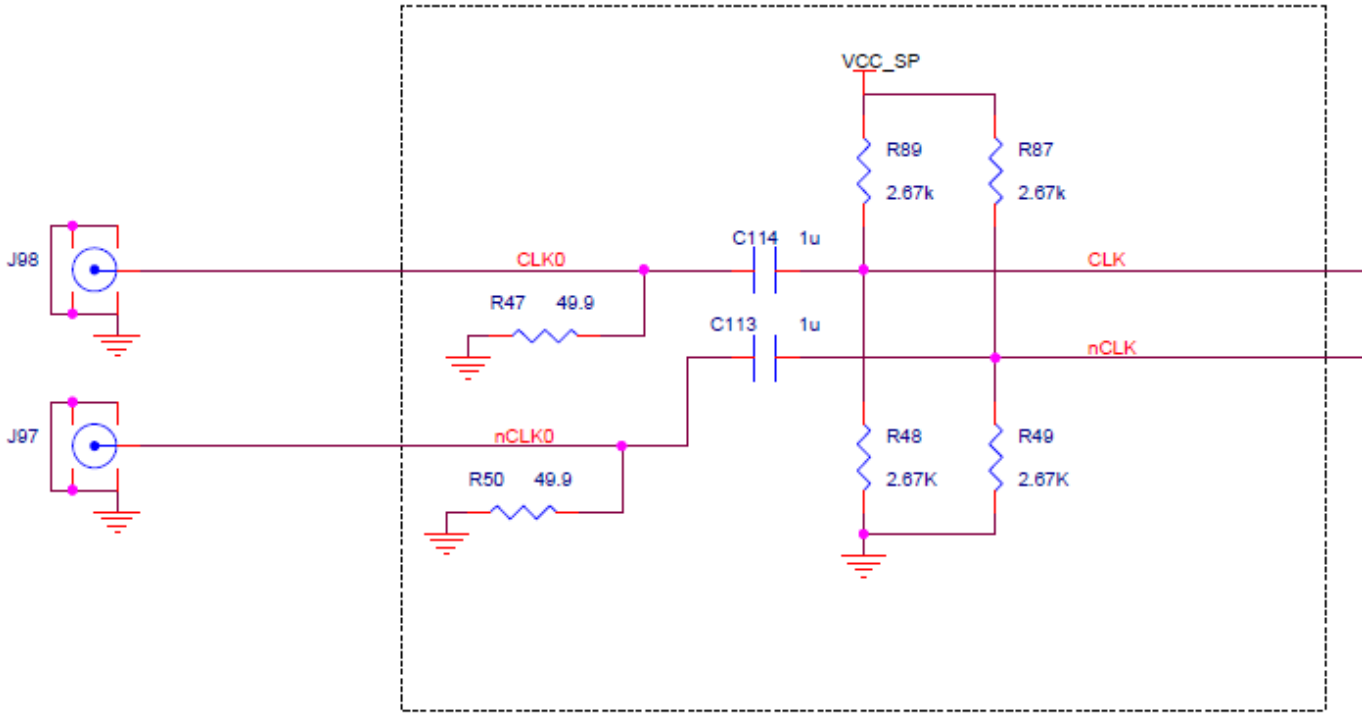


Figure 4. Output Termination Schematics

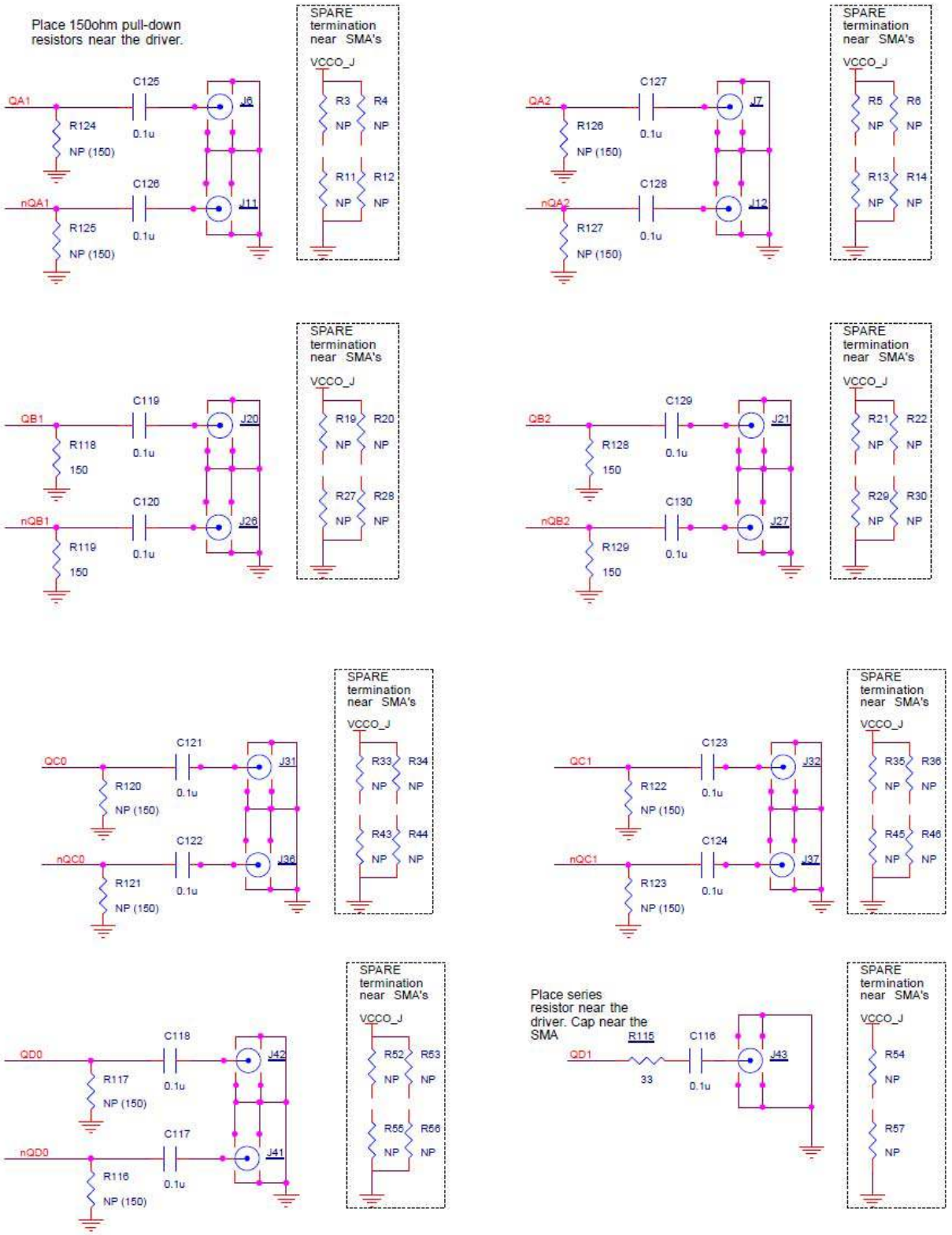
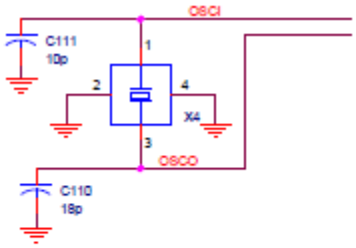


Figure 5. Crystal Interface Schematic



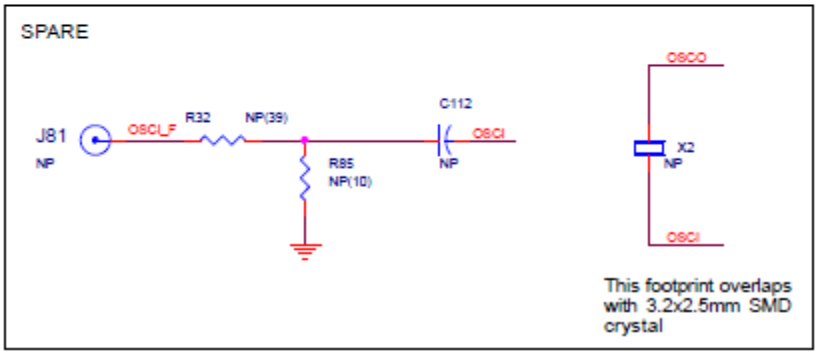


Figure 6. DC Control Schematic

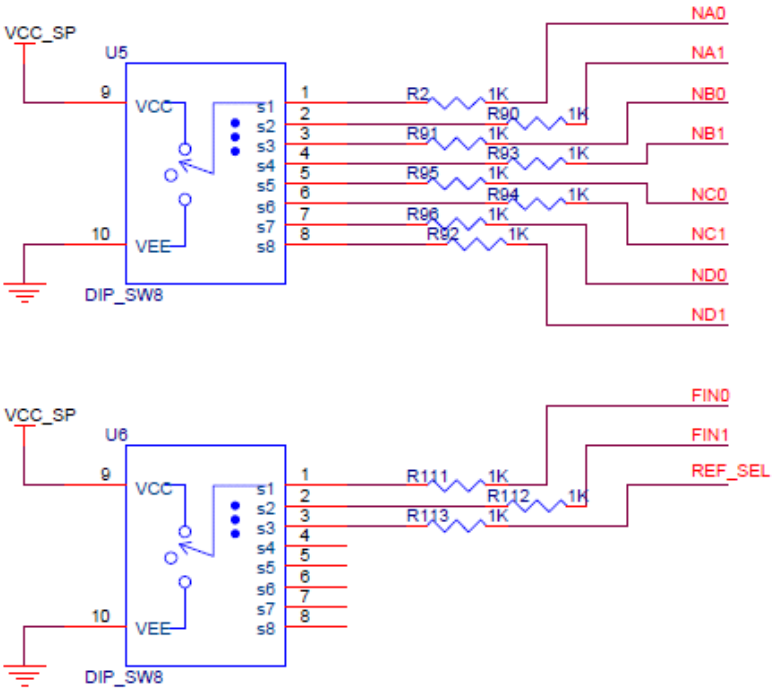


Figure 7. VCCO Power Filtering

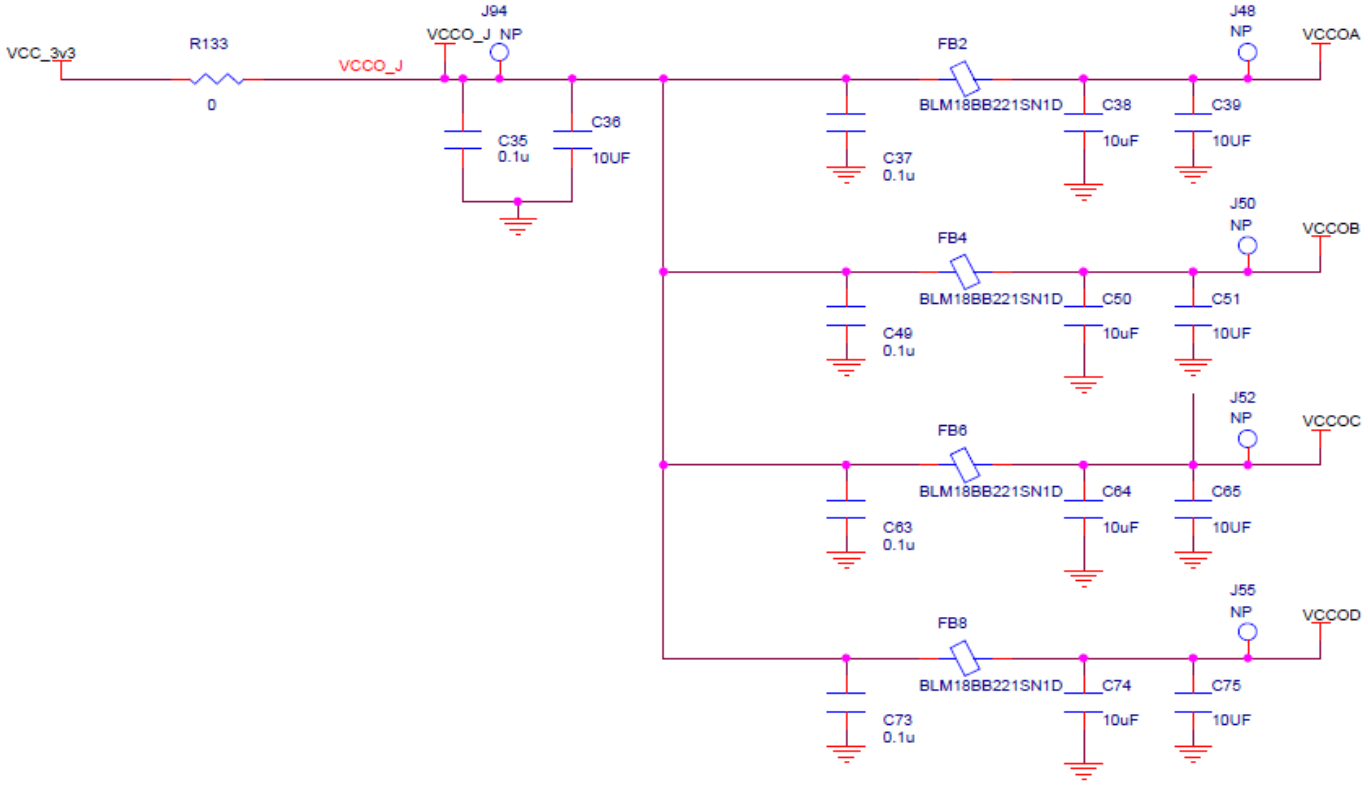


Figure 8. VCC Filtering

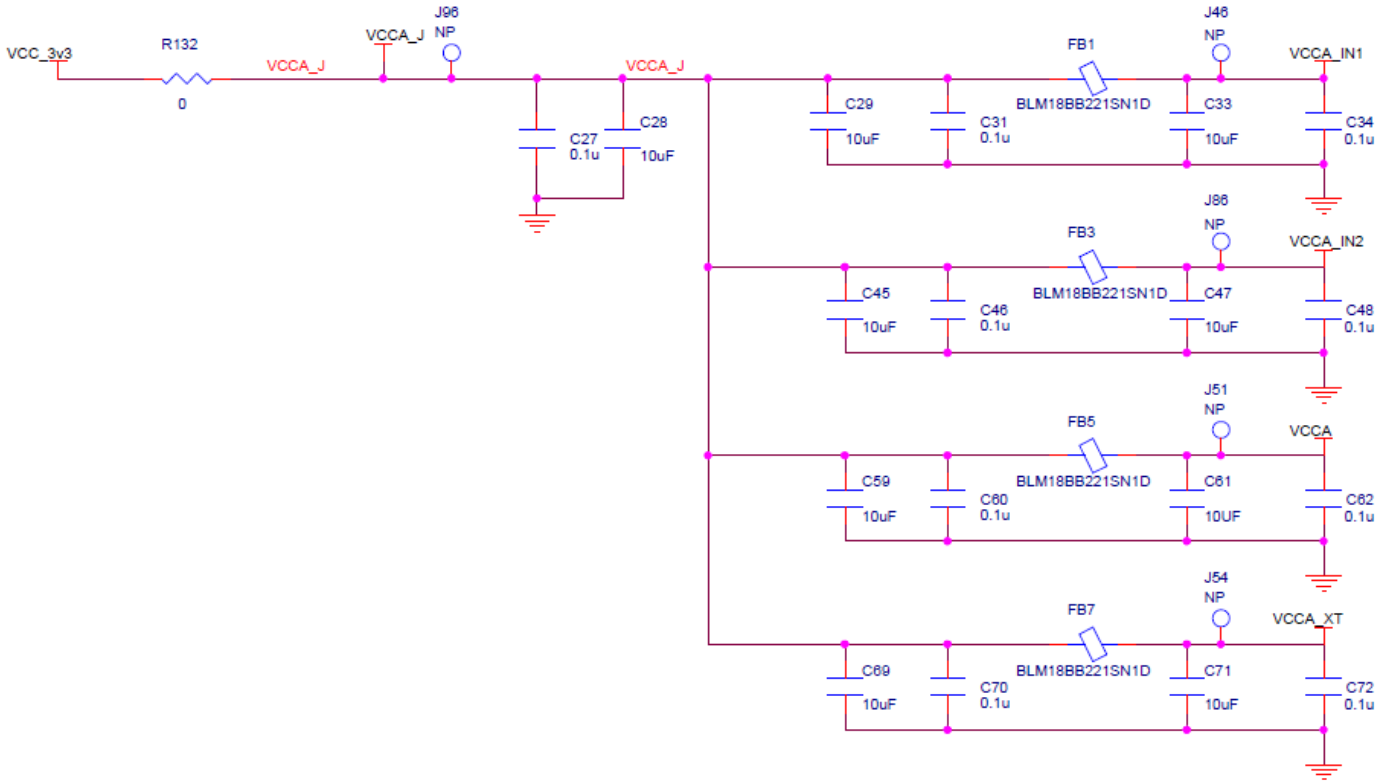


Figure 9. Digital and Core Power Filter

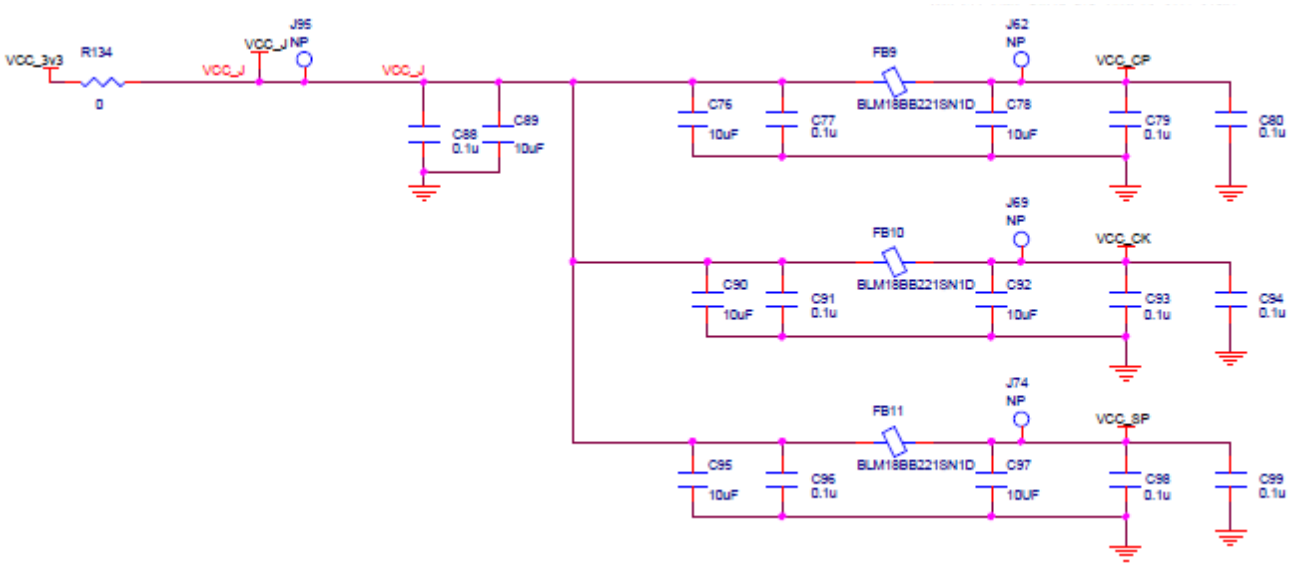
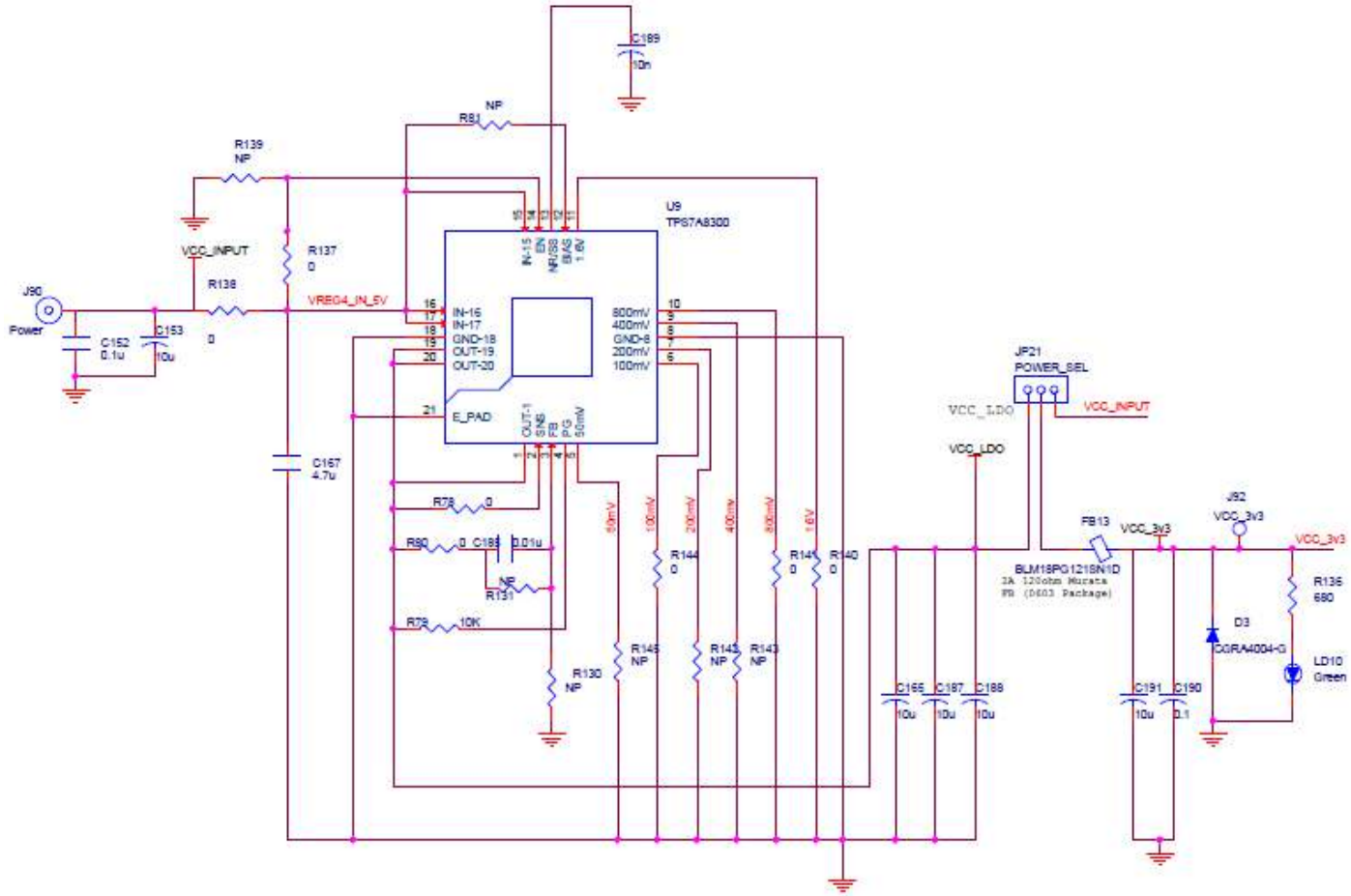


Figure 10. LDO and Power Scheme



Board Power Supply

This board offers the option to power the device from either a supply set to 5V and an LDO (U9) or the supply set to 3.3V and bypassing the LDO.

Bypass External LDO (default configuration)

Set JP21 jumper to VCC_INPUT. Provide 3.3V to the POWER jack (J90).

External LDO Configuration

Set JP21 jumper to VCC_LDO. Provide 5V to the POWER jack (J90).

Input Configuration

The inputs are configured with an ac-coupling termination scheme. This scheme allows flexibility for either differential or single-ended inputs. The default configuration is as follows:

Table 2. Default Input Configuration

Input	Default Termination
CLK0	50Ω to ground, AC-coupled into the device.

Differential Input

Connect the input signal to CLK0 and nCLK0.

Single-ended Input

Connect the input signal to CLK0 and float nCLK0.

Output Configuration

The differential outputs are ac-coupled, allowing for maximum flexibility for observation of the output whether configured for LVPECL or LVDS levels. The default termination scheme can be used to measure either of the two output level-types but is not optimal. The optimal termination circuits are tabulated below. Refer to Figure 4 to locate the components listed below.

Table 3. Termination Outputs for QA1

Signal Type	180Ω Pull-down: R124, R125	Series Capacitors: C125, C126	Resistor Network: R3, R4, R11, R12
LVPECL	Installed	0.1µF	Not Installed
LVDS (default)	Not Installed	0.1µF	Not Installed

Table 4. Termination Outputs for QA2

Signal Type	180Ω Pull-down: R126, R127	Series Capacitors: C127, C128	Resistor Network: R5, R6, R13, R14
LVPECL	Installed	0.1µF	Not Installed
LVDS (default)	Not Installed	0.1µF	Not Installed

Table 5. Termination Outputs for QB1

Signal Type	180Ω Pull-down: R118, R119	Series Capacitors: C119, C120	Resistor Network: R19, R20, R27, R28
LVPECL (default)	Installed	0.1µF	Not Installed
LVDS	Not Installed	0.1µF	Not Installed

Table 6. Termination Outputs for QB2

Signal Type	180Ω Pull-down: R128, R129	Series Capacitors: C129, C130	Resistor Network: R21, R20, R29, R30
LVPECL (default)	Installed	0.1µF	Not Installed
LVCMOS	Not Installed	33Ω	Not Installed
LVDS	Not Installed	0.1µF	Not Installed

Table 7. Termination Outputs for QD0

Signal Type	180Ω Pull-down: R116, R117	Series Capacitors: C118, C117	Resistor Network: R52, R53, R55, R56
LVPECL (default)	Installed	0.1µF	Not Installed
LVCMOS	Not Installed	33Ω	Not Installed
LVDS	Not Installed	0.1µF	Not Installed

As noted, the 4-resistor network is not installed in Tables 2–7 because an oscilloscope with internal 50Ω termination is utilized for signal termination and measurement. If a DC-coupled, stand-alone LVPECL output is needed (without oscilloscope connections), the 4-resistor network needs to be installed accordingly. This table provides the configuration for QA1:

Table 8. Resistor Network Termination for LVPECL for QA1

Signal Type	180Ω Pull-down: R39, R40	Series Capacitors: C123, C125	Resistor Network: R3, R4, R11, R12
LVPECL	Not Installed	0Ω	R3 = R4 = 125Ω R11 = R12 = 84Ω

DC Controls

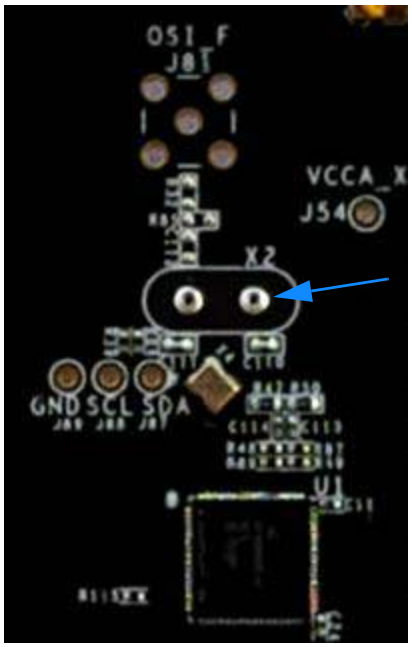
The Dip Switches have three settings: 0V, Float, and VCC. Refer to Figure 1, labels “E” and “F”, for the location of the Dip Switches and their default configuration.

Crystal Interface

By default, a 3.2 × 2.5 mm SMD 50MHz crystal is installed on the top side of the board. It provides the reference frequency for the device. This board supports other options for the XTAL_IN reference. If using one of the other options, the crystal on X4 must be removed.

1. Through-hole crystal. With this option, the device can be evaluated with different crystals without the need to solder each time the crystal is replaced:
   a. Remove the crystal from X4 on the top-side of the board (see Figure 1, “X4” for location of the component).
   b. Place a crystal into the crystal socket X2. (see Figure 11 below for location of the component).

Figure 11. Crystal Interface PCB



2. Crystal Overdrive. With this option, the device can be evaluated with different sources, such as frequency generators, XOs, or other devices. Refer to Figure 5 and Figure 11 for identification of the components mentioned below.
   a. Remove the crystal from X4 (see Figure 1, “X4” for location of the component).
   b. Populate SMA J81.
   c. Solder a 1µF capacitor onto C112. **Note**: the input must be AC-coupled.
   d. R85 may be populated with a 50Ω resistor for input sources requiring such termination.
   e. R32 must be populated. It may be a 0Ω resistor for input sources or 33Ω for CMOS inputs.

Revision History

Revision Date	Description of Change
October 23, 2018	Initial release of user guide in the latest document format.

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