

FEATURES

Latch-up proof
8 kV human body model (HBM) ESD rating
Low on resistance (13.5 Ω)
 ± 9 V to ± 22 V dual-supply operation
9 V to 40 V single-supply operation
Fully specified at ± 15 V, ± 20 V, $+12$ V, and $+36$ V
 V_{SS} to V_{DD} analog signal range

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Military temperature range: -55°C to $+125^{\circ}\text{C}$
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Relay replacement
Automatic test equipment
Data acquisition
Instrumentation
Avionics
Communication systems

GENERAL DESCRIPTION

The [ADG5408-EP/ADG5409-EP](#) are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The [ADG5408-EP](#) switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2. The [ADG5409-EP](#) switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines, A0 and A1.

An EN input on both devices enables or disables the device. When EN is disabled, all channels switch off. The on-resistance profile is very flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals. High switching speed also makes the parts suitable for video signal switching.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked.

Rev. 0

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FUNCTIONAL BLOCK DIAGRAMS

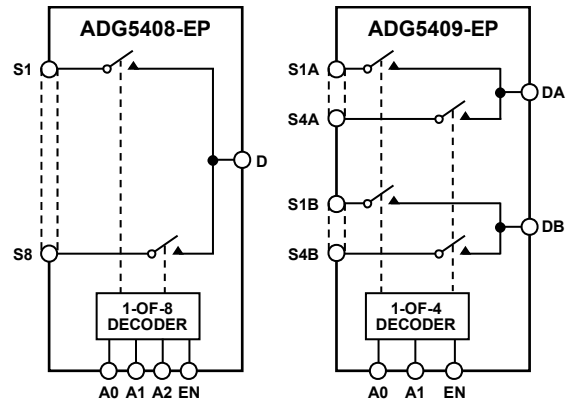


Figure 1.

The [ADG5408-EP/ADG5409-EP](#) do not have V_L pins; rather, the logic power supply is generated internally by an on-chip voltage generator.

Additional application and technical information can be found in the [ADG5408/ADG5409](#) data sheet.

PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON} .
3. Dual-supply operation. For applications where the analog signal is bipolar, the [ADG5408-EP/ADG5409-EP](#) can be operated from dual supplies up to ± 22 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the [ADG5408-EP/ADG5409-EP](#) can be operated from a single rail power supply up to 40 V.
5. 3 V logic compatible digital inputs: $V_{INH} = 2.0$ V, $V_{INL} = 0.8$ V.
6. No V_L logic power supply required.

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REVISION HISTORY

9/15—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	13.5			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 24
	15	18	22	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.8			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	2.2	2.6	3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.05			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.25	± 1	± 7	nA max	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 27
Drain Off Leakage, I_D (Off)	± 0.1			nA typ	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 27
	± 0.4	± 4	± 30	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 10\text{ V}$; see Figure 23
	± 0.4	± 4	± 30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	170			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	217	258	292	ns max	$V_S = 10\text{ V}$; see Figure 30
t_{ON} (EN)	140			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	175	213	242	ns max	$V_S = 10\text{ V}$; see Figure 32
t_{OFF} (EN)	130			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	161	183	198	ns max	$V_S = 10\text{ V}$; see Figure 32
Break-Before-Make Time Delay, t_D	50			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			13	ns min	$V_{S1} = V_{S2} = 10\text{ V}$; see Figure 31
Charge Injection, Q_{INJ}	115			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 33
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
Channel-to-Channel Crosstalk	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 25
Total Harmonic Distortion + Noise	0.01			% typ	$R_L = 1\text{ k}\Omega$, 15 V p-p , $f = 20\text{ Hz to }20\text{ kHz}$; see Figure 28
-3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 29
ADG5408-EP	50			MHz typ	
ADG5409-EP	87			MHz typ	
Insertion Loss	0.9			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; Figure 29
C_S (Off)	15			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)					
ADG5408-EP	102			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG5409-EP	50			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
C _D (On), C _S (On) ADG5408-EP ADG5409-EP	133 81			pF typ pF typ	V _S = 0 V, f = 1 MHz V _S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V _{DD} = +16.5 V, V _{SS} = -16.5 V
I _{DD}	45 55		80	μA typ μA max	Digital inputs = 0 V or V _{DD}
I _{SS}	0.001		1	μA typ μA max	Digital inputs = 0 V or V _{DD}
V _{DD} /V _{SS}			±9/±22	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = -20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analogue Signal Range			V _{DD} to V _{SS}	V	
On Resistance, R _{ON}	12.5 14	17	21	Ω typ Ω max	V _S = ±15 V, I _S = -10 mA; see Figure 24 V _{DD} = +18 V, V _{SS} = -18 V
On-Resistance Match Between Channels, ΔR _{ON}	0.3			Ω typ	V _S = ±15 V, I _S = -10 mA
On-Resistance Flatness, R _{FLAT (ON)}	0.8 2.3 2.7	1.3 3.1	1.4 3.5	Ω max Ω typ Ω max	V _S = ±15 V, I _S = -10 mA
LEAKAGE CURRENTS					V _{DD} = +22 V, V _{SS} = -22 V
Source Off Leakage, I _S (Off)	±0.1 ±0.25	±1	±7	nA typ nA max	V _S = ±15 V, V _D = ∓15 V; see Figure 27
Drain Off Leakage, I _D (Off)	±0.15 ±0.4	±4	±30	nA typ nA max	V _S = ±15 V, V _D = ∓15 V; see Figure 27
Channel On Leakage, I _D (On), I _S (On)	±0.15 ±0.4	±4	±30	nA typ nA max	V _S = V _D = ±15 V; see Figure 23
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.002		±0.1	μA typ μA max	V _{IN} = V _{GND} or V _{DD}
Digital Input Capacitance, C _{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, t _{TRANSITION}	160 207	237	262	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 10 V; see Figure 30
t _{ON} (EN)	140 165	194	218	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 10 V; see Figure 32
t _{OFF} (EN)	133 153	174	189	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 10 V; see Figure 32
Break-Before-Make Time Delay, t _D	38		8	ns typ ns min	R _L = 300 Ω, C _L = 35 pF V _{S1} = V _{S2} = 10 V; see Figure 31
Charge Injection, Q _{INJ}	155			pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 33
Off Isolation	-60			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	-60			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 25

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
Total Harmonic Distortion + Noise	0.012			% typ	$R_L = 1\text{ k}\Omega$, 20 V p-p, $f = 20\text{ Hz to }20\text{ kHz}$; see Figure 28
-3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 29
ADG5408-EP	50			MHz typ	
ADG5409-EP	88			MHz typ	
Insertion Loss	0.8			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 29
C_S (Off)	17			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)					
ADG5408-EP	98			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG5409-EP	48			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)					
ADG5408-EP	128			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
ADG5409-EP	80			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	50			$\mu\text{A typ}$	$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$
	70		120	$\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
I_{SS}	0.001			$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
			1	$\mu\text{A max}$	
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	26			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 24
	30	36	42	Ω max	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
	1	1.5	1.6	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	5.5			Ω typ	$V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$
	6.5	8	12	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.02			nA typ	$V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$
	± 0.25	± 1	± 7	nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 27
Drain Off Leakage, I_D (Off)	± 0.05			nA typ	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 27
	± 0.4	± 4	± 30	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.05			nA typ	$V_S = V_D = 1\text{ V}/10\text{ V}$; see Figure 23
	± 0.4	± 4	± 30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			$\mu\text{A typ}$	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	$\mu\text{A max}$	
Digital Input Capacitance, C_{IN}	3			pF typ	

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{\text{TRANSITION}}$	230			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	321	388	430	ns max	$V_S = 8 \text{ V}$; see Figure 30
t_{ON} (EN)	215			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	276	345	397	ns max	$V_S = 8 \text{ V}$; see Figure 32
t_{OFF} (EN)	134			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	161	187	209	ns max	$V_S = 8 \text{ V}$; see Figure 32
Break-Before-Make Time Delay, t_D	118			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
			44	ns min	$V_{S1} = V_{S2} = 8 \text{ V}$; see Figure 31
Charge Injection, Q_{INJ}	45			pC typ	$V_S = 6 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 33
Off Isolation	-60			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 26
Channel-to-Channel Crosstalk	-60			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 25
Total Harmonic Distortion + Noise	0.1			% typ	$R_L = 1 \text{ k}\Omega$, 6 V p-p , $f = 20 \text{ Hz to } 20 \text{ kHz}$; see Figure 28
-3 dB Bandwidth					$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 29
ADG5408-EP	35			MHz typ	
ADG5409-EP	74			MHz typ	
Insertion Loss	-1.8			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 29
C_S (Off)	22			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
C_D (Off)					
ADG5408-EP	119			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
ADG5409-EP	59			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
C_D (On), C_S (On)					
ADG5408-EP	146			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
ADG5409-EP	86			pF typ	$V_S = 6 \text{ V}$, $f = 1 \text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	40			$\mu\text{A typ}$	$V_{\text{DD}} = 13.2 \text{ V}$
	50		75	$\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	$\text{GND} = 0 \text{ V}$, $V_{\text{SS}} = 0 \text{ V}$

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{\text{DD}} = 36 \text{ V} \pm 10\%$, $V_{\text{SS}} = 0 \text{ V}$, $\text{GND} = 0 \text{ V}$, unless otherwise noted.

Table 4.

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$0 \text{ V to } V_{\text{DD}}$	V	
On Resistance, R_{ON}	14.5			$\Omega \text{ typ}$	$V_S = 0 \text{ V to } 30 \text{ V}$, $I_S = -10 \text{ mA}$; see Figure 24
	16	19	23	$\Omega \text{ max}$	$V_{\text{DD}} = 32.4 \text{ V}$, $V_{\text{SS}} = 0 \text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.3			$\Omega \text{ typ}$	$V_S = 0 \text{ V to } 30 \text{ V}$, $I_S = -10 \text{ mA}$
	0.8	1.3	1.4	$\Omega \text{ max}$	
On-Resistance Flatness, $R_{\text{FLAT (ON)}}$	3.5			$\Omega \text{ typ}$	$V_S = 0 \text{ V to } 30 \text{ V}$, $I_S = -10 \text{ mA}$
	4.3	5.5	6.5	$\Omega \text{ max}$	

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	±0.1			nA typ	$V_{DD} = 39.6\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/30\text{ V}$, $V_D = 30\text{ V}/1\text{ V}$; see Figure 27
Drain Off Leakage, I_D (Off)	±0.25 ±0.15	±1	±7	nA max nA typ	$V_S = 1\text{ V}/30\text{ V}$, $V_D = 30\text{ V}/1\text{ V}$; see Figure 27
Channel On Leakage, I_D (On), I_S (On)	±0.4 ±0.15 ±0.4	±4 ±4	±30 ±30	nA max nA typ nA max	$V_S = V_D = 1\text{ V}/30\text{ V}$; see Figure 23
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	$V_{IN} = V_{GND}$ or V_{DD}
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002		±0.1	µA typ µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	187 242			ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$; see Figure 30
t_{ON} (EN)	160 195	257 219	281 237	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$; see Figure 32
t_{OFF} (EN)	147 184			ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 18\text{ V}$; see Figure 32
Break-Before-Make Time Delay, t_D	53	184	190	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 18\text{ V}$; see Figure 31
Charge Injection, Q_{INJ}	150		14	pC typ	$V_S = 18\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 33
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
Channel-to-Channel Crosstalk	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 25
Total Harmonic Distortion + Noise	0.4			% typ	$R_L = 1\text{ k}\Omega$, 18 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 28
-3 dB Bandwidth					$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 29
ADG5408-EP	45			MHz typ	
ADG5409-EP	76			MHz typ	
Insertion Loss	-1			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 29
C_S (Off)	18			pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)					
ADG5408-EP	120			pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
ADG5409-EP	60			pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)					
ADG5408-EP	137			pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
ADG5409-EP	80			pF typ	$V_S = 18\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	80 100		155	µA typ µA max	$V_{DD} = 39.6\text{ V}$ Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	$GND = 0\text{ V}$, $V_{SS} = 0\text{ V}$

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR D

Table 5. ADG5408-EP

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR D ($\theta_{JA} = 30.4^{\circ}\text{C/W}$)				
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$	207	113	60	mA maximum
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$	218	117	61	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$	168	99	57	mA maximum
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$	214	116	61	mA maximum

Table 6. ADG5409-EP

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR D ($\theta_{JA} = 30.4^{\circ}\text{C/W}$)				
$V_{DD} = +15\text{ V}, V_{SS} = -15\text{ V}$	156	95	55	mA maximum
$V_{DD} = +20\text{ V}, V_{SS} = -20\text{ V}$	165	98	56	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$	126	81	50	mA maximum
$V_{DD} = 36\text{ V}, V_{SS} = 0\text{ V}$	161	97	56	mA maximum

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	-0.3 V to +48 V
V_{SS} to GND	+0.3 V to -48 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx or D Pins ADG5408-EP ADG5409-EP	435 mA (pulsed at 1 ms, 10% duty cycle maximum) 300 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or D ²	Data + 15%
Temperature Range	
Operating	-55°C to $+125^\circ\text{C}$
Storage	-65°C to $+150^\circ\text{C}$
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead LFCSP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb-Free	As per JEDEC J-STD-020

¹ Overvoltages at the Ax, EN, Sx, and D pins are clamped by internal diodes. Limit current to the maximum ratings given.

² See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

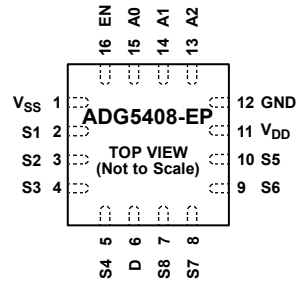
Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

13397-003

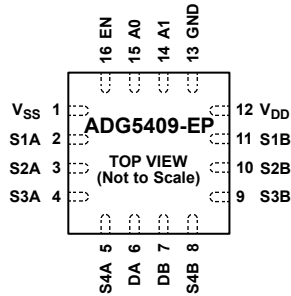
Figure 2. ADG5408-EP Pin Configuration

Table 8. ADG5408-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
15	A0	Logic Control Input.
16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
1	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
2	S1	Source Terminal 1. This pin can be an input or an output.
3	S2	Source Terminal 2. This pin can be an input or an output.
4	S3	Source Terminal 3. This pin can be an input or an output.
5	S4	Source Terminal 4. This pin can be an input or an output.
6	D	Drain Terminal. This pin can be an input or an output.
7	S8	Source Terminal 8. This pin can be an input or an output.
8	S7	Source Terminal 7. This pin can be an input or an output.
9	S6	Source Terminal 6. This pin can be an input or an output.
10	S5	Source Terminal 5. This pin can be an input or an output.
11	V _{DD}	Most Positive Power Supply Potential.
12	GND	Ground (0 V) Reference.
13	A2	Logic Control Input.
14	A1	Logic Control Input.
EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} .

Table 9. ADG5408-EP Truth Table

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

13387-005

Figure 3. ADG5409-EP Pin Configuration

Table 10. ADG5409-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
15	A0	Logic Control Input.
16	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
1	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
2	S1A	Source Terminal 1A. This pin can be an input or an output.
3	S2A	Source Terminal 2A. This pin can be an input or an output.
4	S3A	Source Terminal 3A. This pin can be an input or an output.
5	S4A	Source Terminal 4A. This pin can be an input or an output.
6	DA	Drain Terminal A. This pin can be an input or an output.
7	DB	Drain Terminal B. This pin can be an input or an output.
8	S4B	Source Terminal 4B. This pin can be an input or an output.
9	S3B	Source Terminal 3B. This pin can be an input or an output.
10	S2B	Source Terminal 2B. This pin can be an input or an output.
11	S1B	Source Terminal 1B. This pin can be an input or an output.
12	V _{DD}	Most Positive Power Supply Potential.
13	GND	Ground (0 V) Reference.
14	A1	Logic Control Input.
EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} .

Table 11. ADG5409-EP Truth Table

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TYPICAL PERFORMANCE CHARACTERISTICS

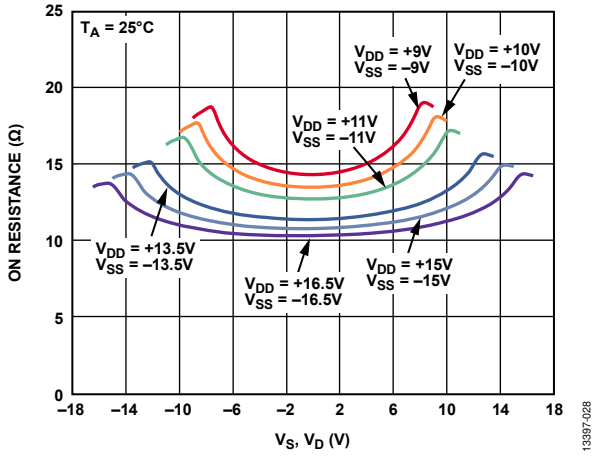


Figure 4. R_{ON} as a Function of V_S, V_D (Dual Supply)

13397-028

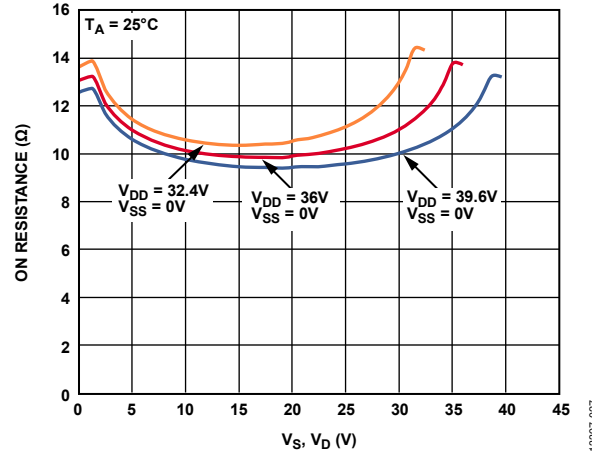


Figure 7. R_{ON} as a Function of V_S, V_D (Single Supply)

13397-027

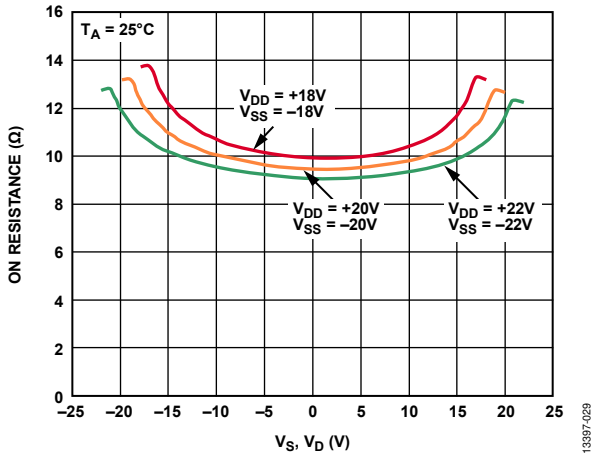


Figure 5. R_{ON} as a Function of V_S, V_D (Dual Supply)

13397-028

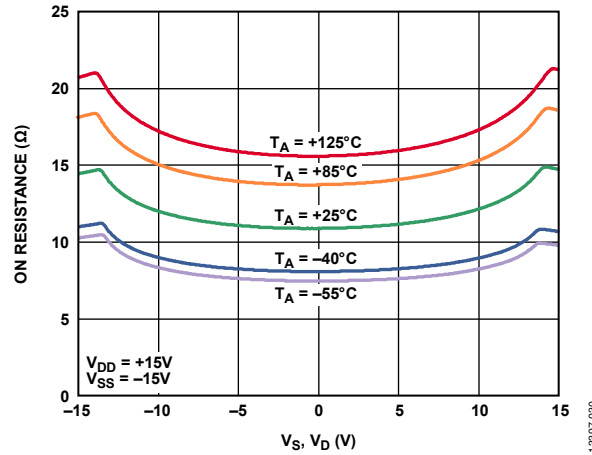


Figure 8. R_{ON} as a Function of $V_S (V_D)$ for Different Temperatures, ± 15 V Dual Supply

13397-030

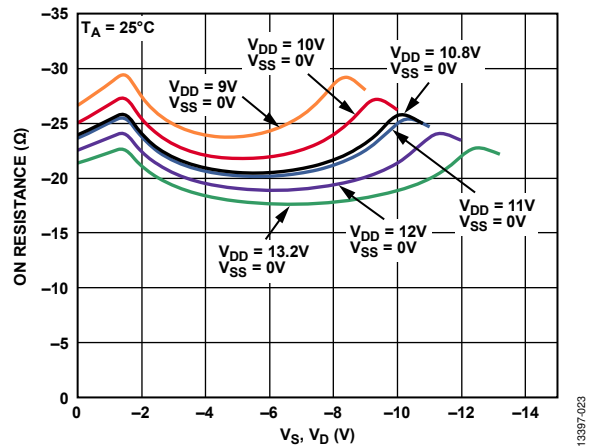


Figure 6. R_{ON} as a Function of V_S, V_D (Single Supply)

13397-028

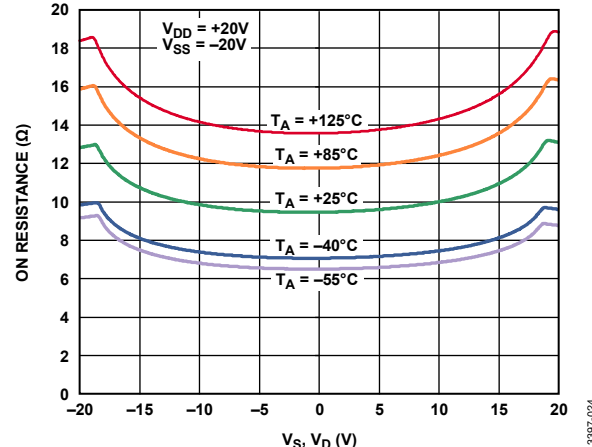


Figure 9. R_{ON} as a Function of $V_S (V_D)$ for Different Temperatures, ± 20 V Dual Supply

13397-024

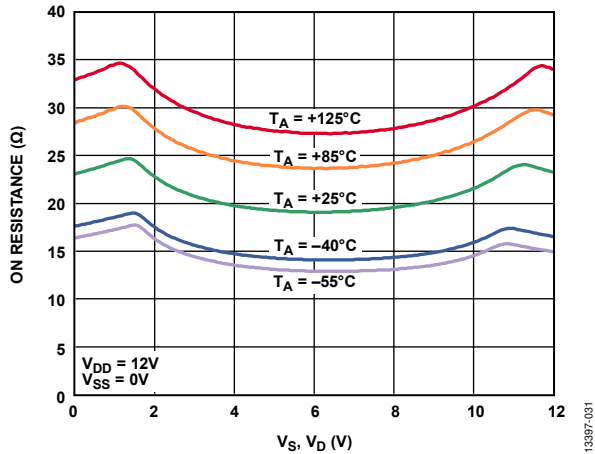


Figure 10. R_{ON} as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

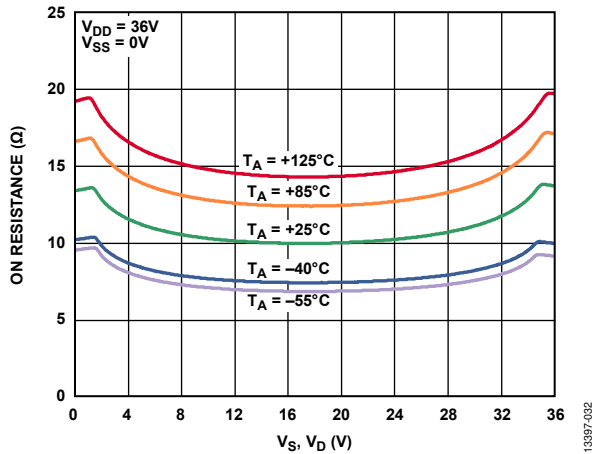


Figure 11. R_{ON} as a Function of V_D (V_S) for Different Temperatures, 36 V Single Supply

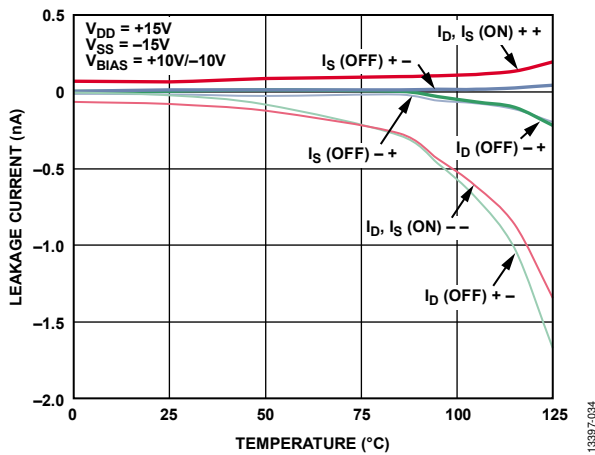


Figure 12. Leakage Currents vs. Temperature, ± 15 V Dual Supply

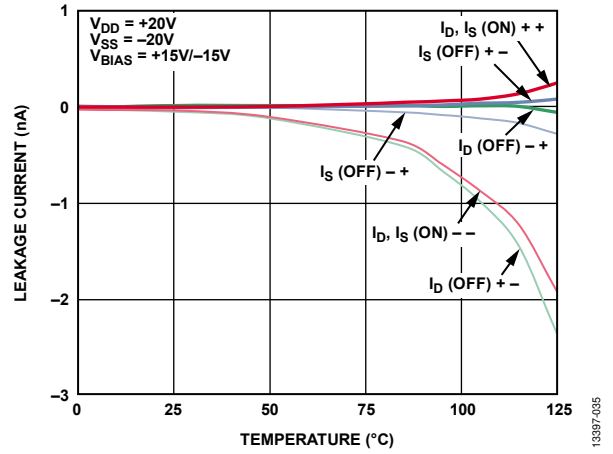


Figure 13. Leakage Currents vs. Temperature, ± 20 V Dual Supply

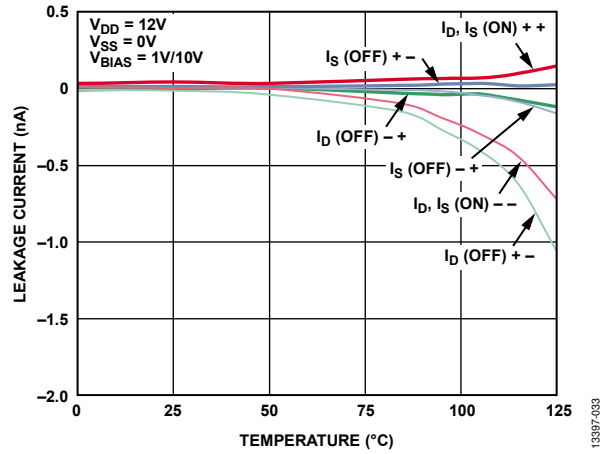


Figure 14. Leakage Currents vs. Temperature, 12 V Single Supply

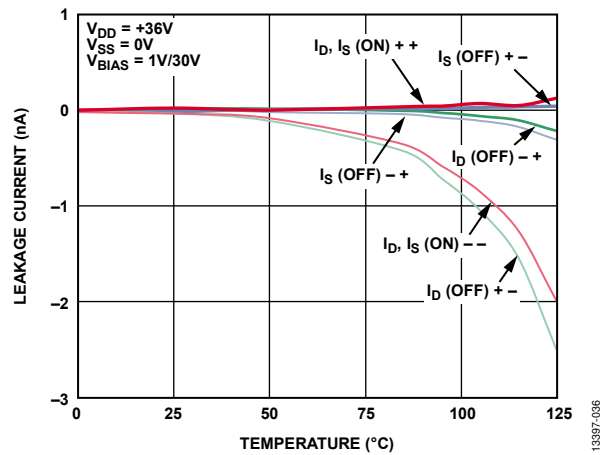


Figure 15. Leakage Currents vs. Temperature, 36 V Single Supply

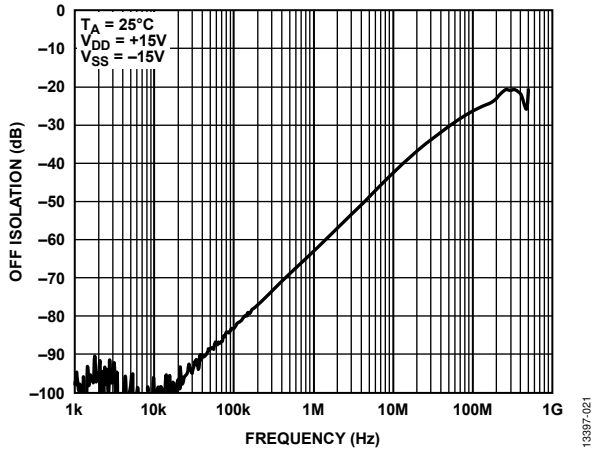


Figure 16. Off Isolation vs. Frequency, ±15 V Dual Supply

13397-021

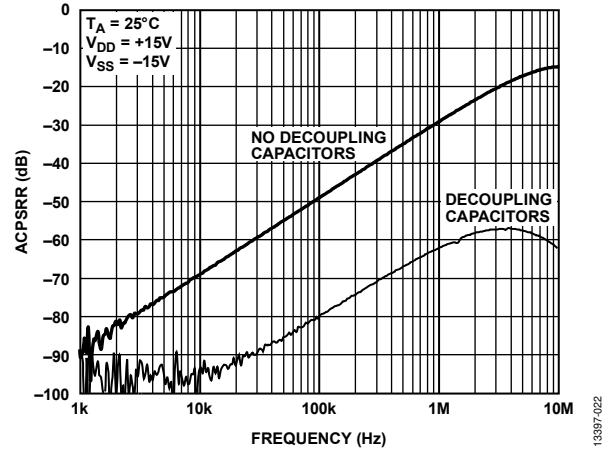


Figure 19. ACPSRR vs. Frequency, ±15 V Dual Supply

13397-022

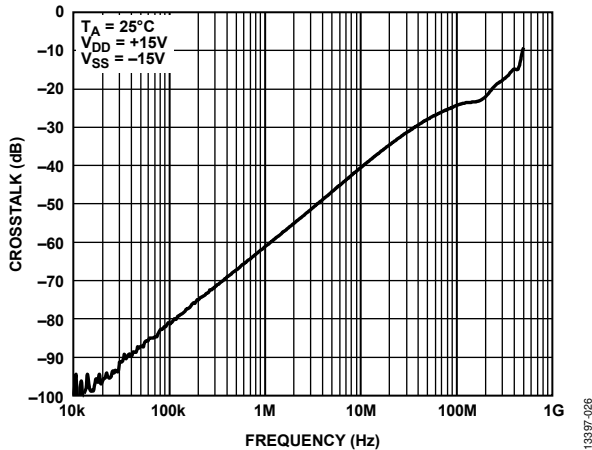


Figure 17. Crosstalk vs. Frequency, ±15 V Dual Supply

13397-026

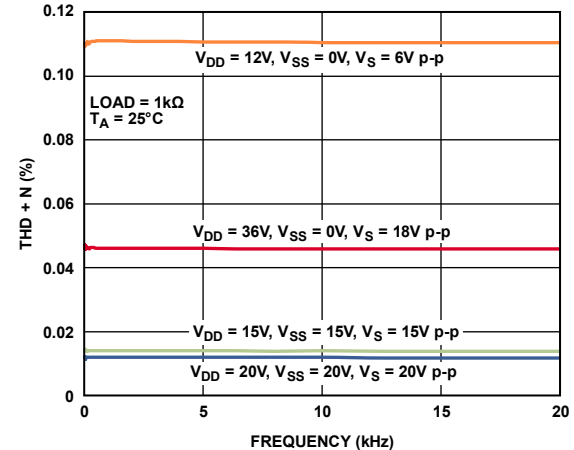


Figure 20. THD + N vs. Frequency

13397-025

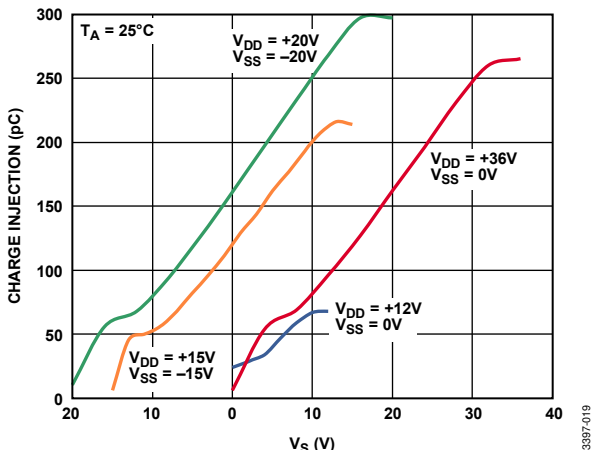


Figure 18. Charge Injection vs. Source Voltage

13397-019

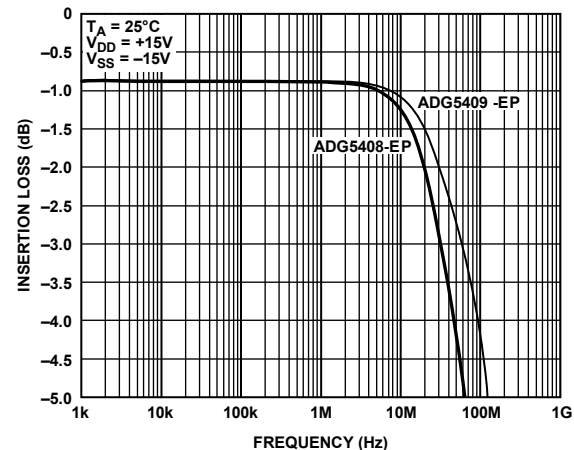


Figure 21. Bandwidth

13397-020

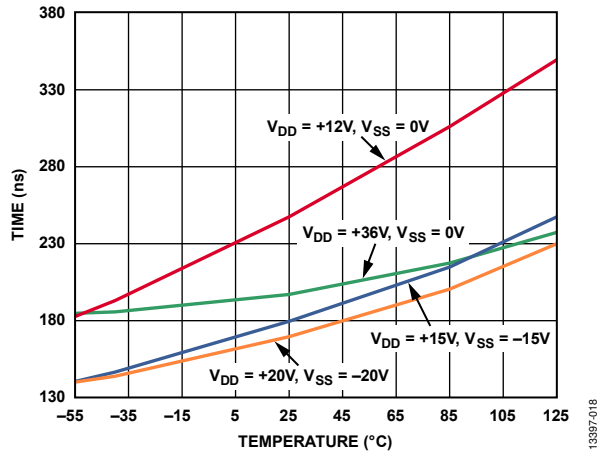


Figure 22. $t_{TRANSITION}$ Times vs. Temperature

13397-018

TEST CIRCUITS

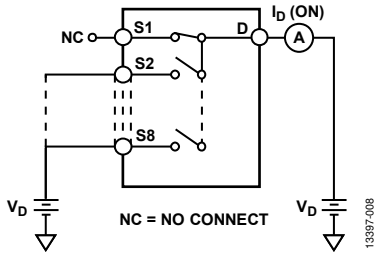


Figure 23. On Leakage

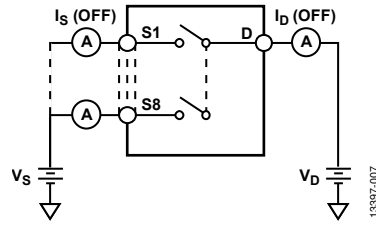


Figure 27. Off Leakage

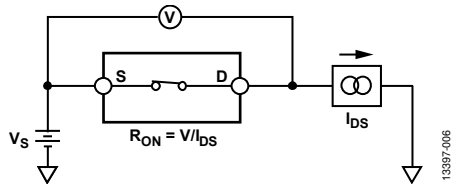


Figure 24. On Resistance

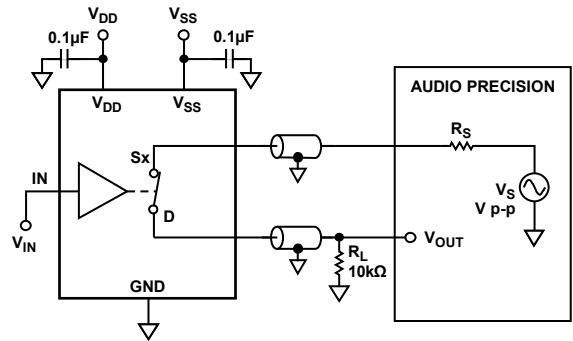
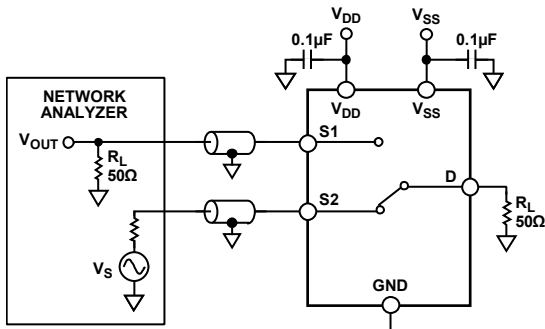
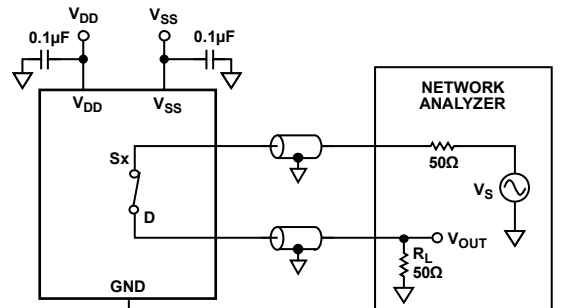


Figure 28. THD + Noise Figure



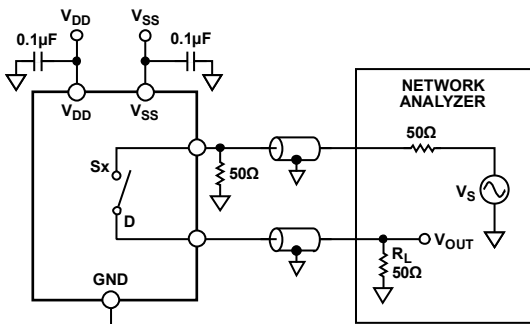
$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 25. Channel-to-Channel Crosstalk



$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_{OUT \text{ WITHOUT SWITCH}}}$$

Figure 29. Bandwidth



$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 26. Off Isolation

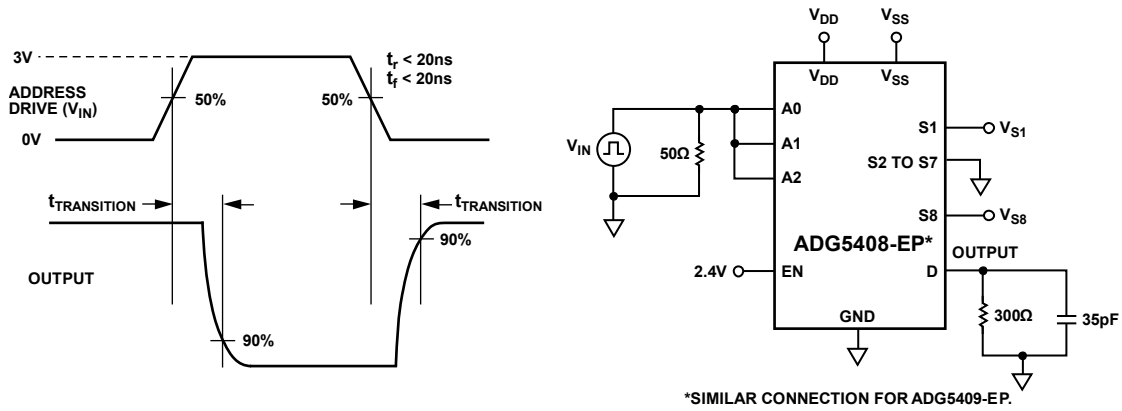


Figure 30. Address to Output Switching Times, $t_{\text{TRANSITION}}$

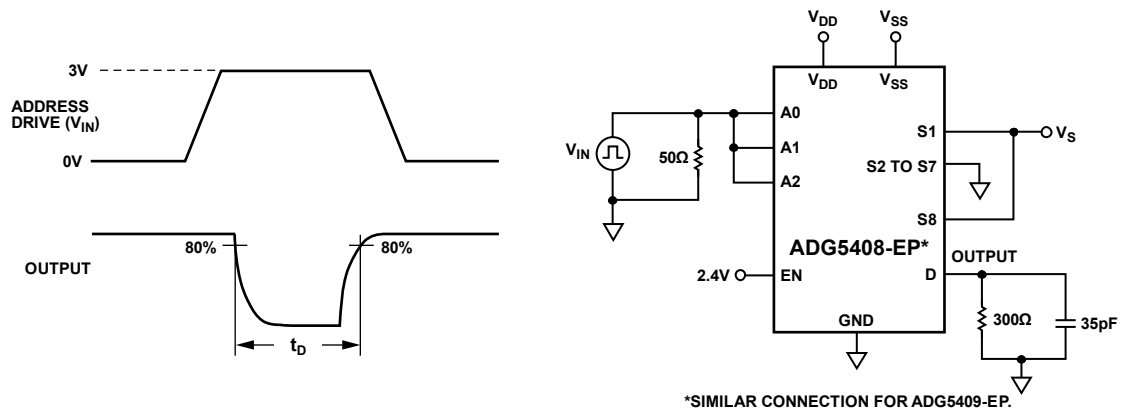


Figure 31. Break-Before-Make Delay, t_D

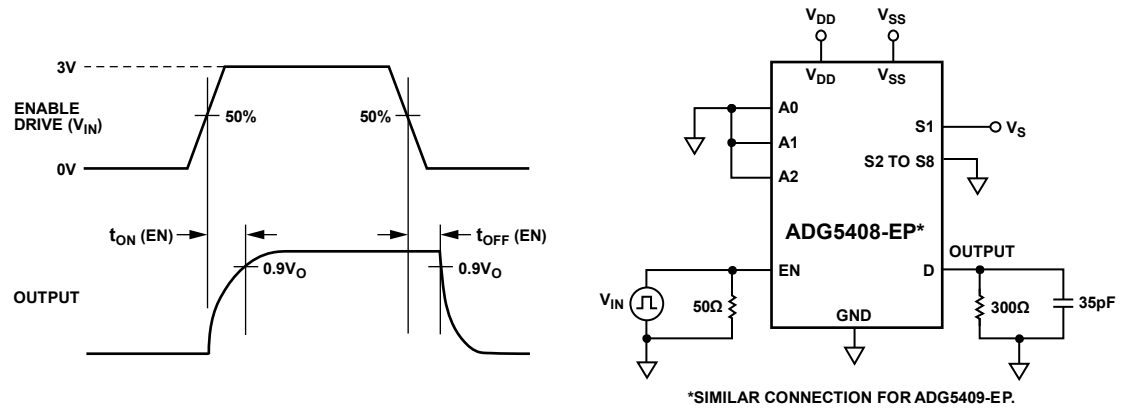


Figure 32. Enable Delay, $t_{\text{ON}}(\text{EN})$, $t_{\text{OFF}}(\text{EN})$

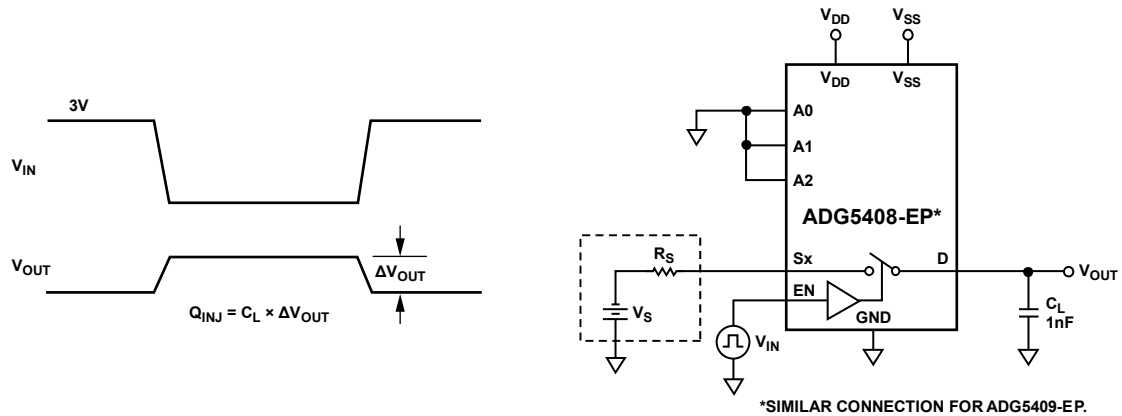


Figure 33. Charge Injection
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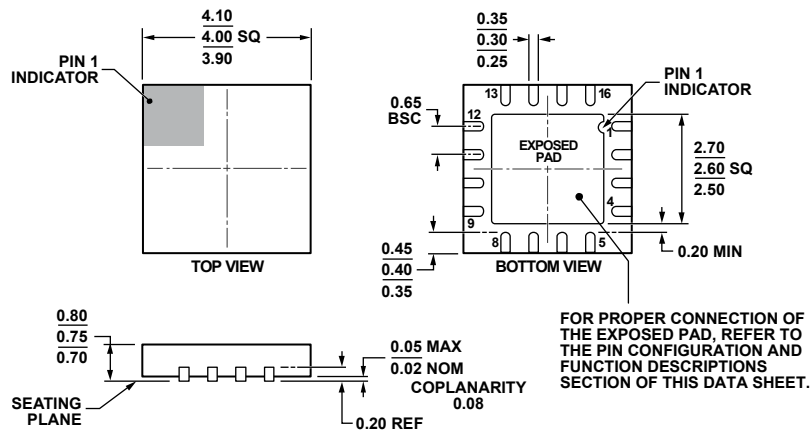
13397-009

13397-010

13397-011

13397-012

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
 4 mm × 4 mm Body, Very Very Thin Quad
 (CP-16-17)
 Dimensions shown in millimeters

08-16-2010-C

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG5408TCPZ-EP-RL7	-55°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17
ADG5408TCPZ-EP	-55°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17
ADG5409TCPZ-EP-RL7	-55°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17
ADG5409TCPZ-EP	-55°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17

¹ Z = RoHS Compliant Part.