CSD25480F3 –20-V P-Channel FemtoFET™ MOSFET

1 Features

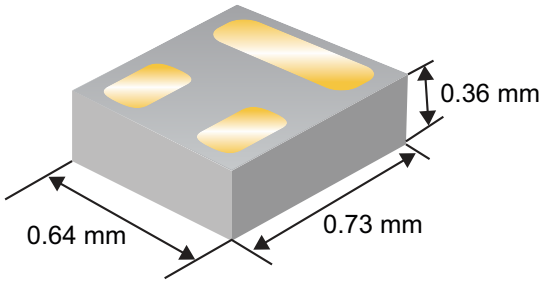
- Low on-resistance
- Ultra-low Q_g and Q_{gd}
- Ultra-small footprint
  - 0.73 mm × 0.64 mm
- Low profile
  - 0.36-mm max height
- Integrated ESD protection diode
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

3 Description

This –20-V, 110-mΩ, P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.



Typical Part Dimensions

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	0.7		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.10		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V	420	mΩ
		V_{GS} = –2.5 V	203	
		V_{GS} = –4.5 V	132	
		V_{GS} = –8.0 V	110	
$V_{GS(th)}$	Threshold Voltage	–0.95		V

Device Information(1)

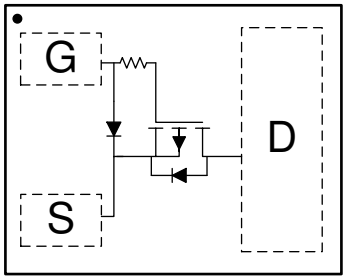
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD25480F3	3000	7-Inch Reel	Femto 0.73-mm × 0.64-mm Land Grid Array (LGA)	Tape and Reel
CSD25480F3T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C (unless otherwise stated)		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–12	V
I_D	Continuous Drain Current(1)	–1.7	A
I_{DM}	Pulsed Drain Current(1) (2)	–10.6	A
P_D	Power Dissipation(1)	500	mW
$V_{(ESD)}$	Human-Body Model (HBM)	4000	V
	Charged-Device Model (CDM)	2000	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C

(1) Typical $R_{\theta JA}$ = 255°C/W mounted on FR4 material with minimum Cu mounting area.
(2) Pulse duration ≤100 µs, duty cycle ≤1%.



Top View

Table of Contents

4 Revision History

Changes from Revision A (August 2017) to Revision B (February 2022) **Page**

- Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.... 1
- Updated ultra-low profile image height from 0.35 mm to 0.36 mm.... 1
- Changed ultra-low profile image height from 0.35 mm to 0.36 mm.... 8
- Added FemtoFET Surface Mount Guide note.... 9

Changes from Revision * (April 2016) to Revision A (August 2017) **Page**

- Added the *Section 6.1* section in *Section 6* 7
- Added Recommended Minimum PCB Layout 9
- Updated the *Section 7.3* 9

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –16 V			–50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V			–25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.70	–0.95	–1.20	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		420	840	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.4 A		203	260	
		V_{GS} = –4.5 V, I_{DS} = –0.4 A		132	159	
		V_{GS} = –8 V, I_{DS} = –0.4 A		110	132	
g_{fs}	Transconductance	V_{DS} = –10 V, I_{DS} = –0.4 A		8.0		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		119	155	pF
C_{oss}	Output capacitance			48	62	pF
C_{rss}	Reverse transfer capacitance			3.6	4.7	pF
R_G	Series gate resistance			16		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –0.4 A		0.70	0.91	nC
Q_{gd}	Gate charge gate-to-drain			0.10		nC
Q_{gs}	Gate charge gate-to-source			0.26		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.15		nC
Q_{oss}	Output charge	V_{DS} = –10 V, V_{GS} = 0 V		1.3		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.4 A, R_G = 10 Ω		9		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turnoff delay time			13		ns
t_f	Fall time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.4 A, V_{GS} = 0 V		–0.78	–1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= –10 V, I_F = –0.4 A, di/dt = 100 A/µs		1.2		nC
t_{rr}	Reverse recovery time			6.4		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	90	°C/W
	Junction-to-ambient thermal resistance(2)	255	

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz. (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

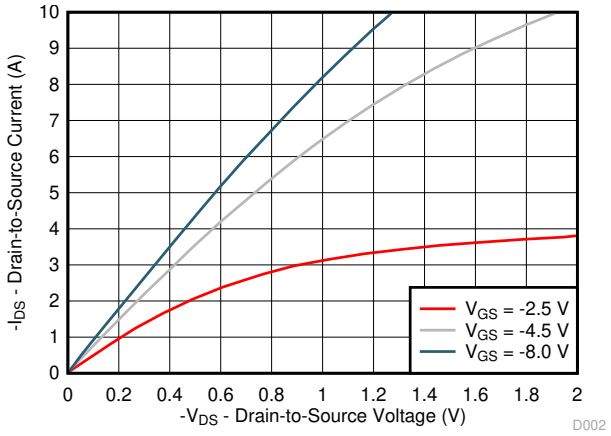
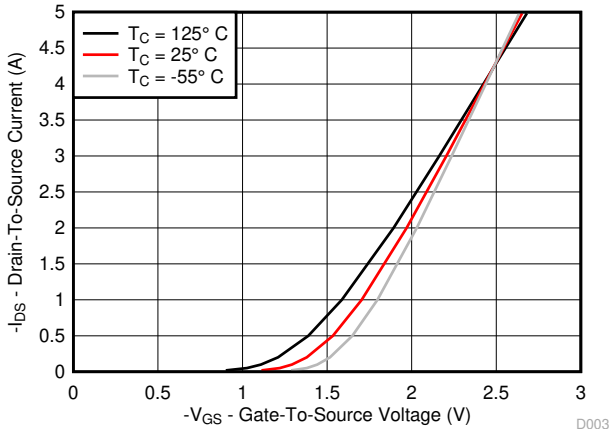


Figure 5-1. Saturation Characteristics



V_{DS} = –5 V

Figure 5-2. Transfer Characteristics

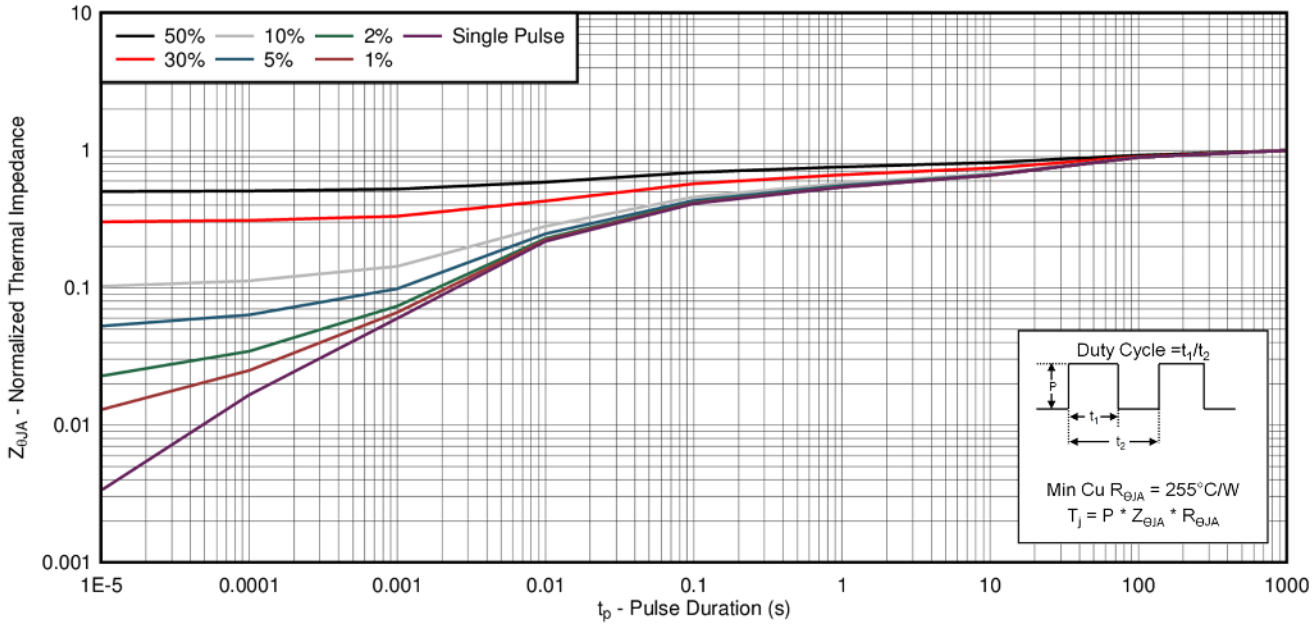
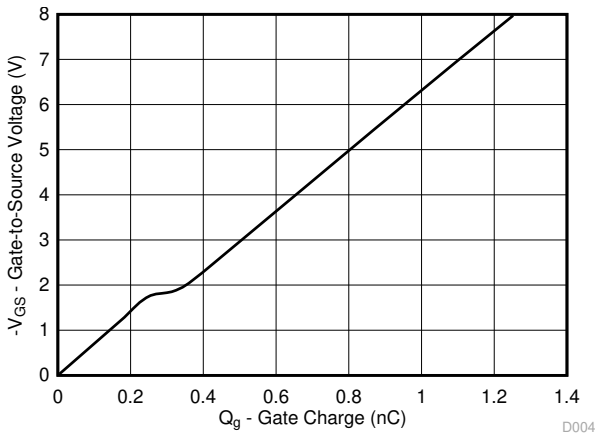


Figure 5-3. Transient Thermal Impedance



I_D = –0.4 A V_{DS} = –10 V

Figure 5-4. Gate Charge

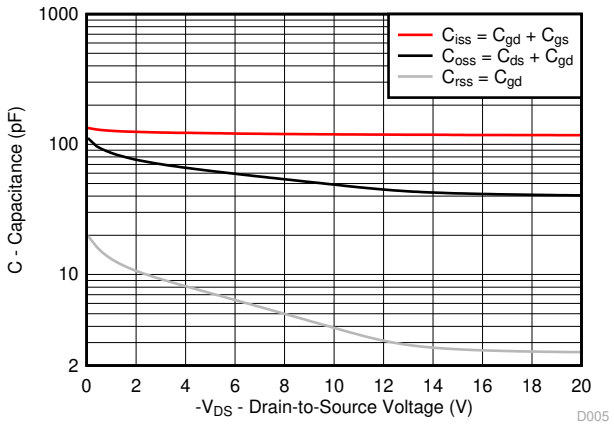
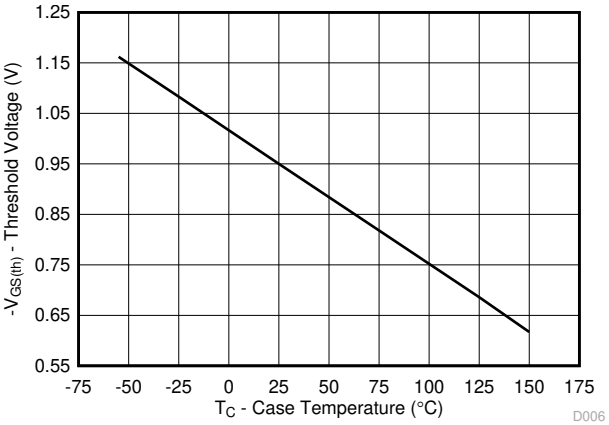


Figure 5-5. Capacitance



I_D = –250 µA

Figure 5-6. Threshold Voltage vs Temperature

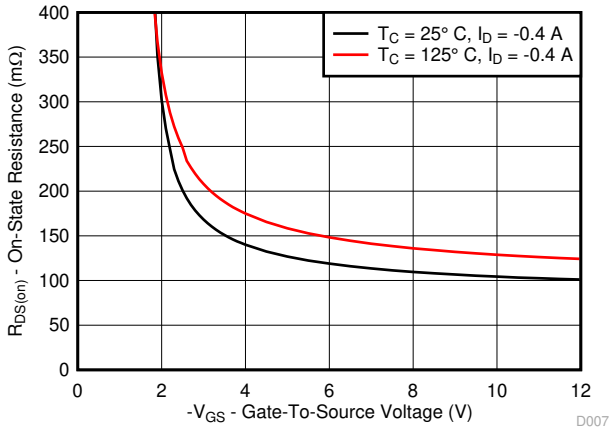
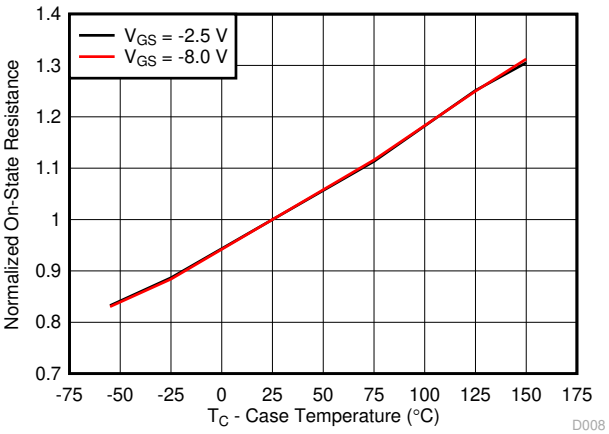


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –0.4 A

Figure 5-8. Normalized On-State Resistance vs Temperature

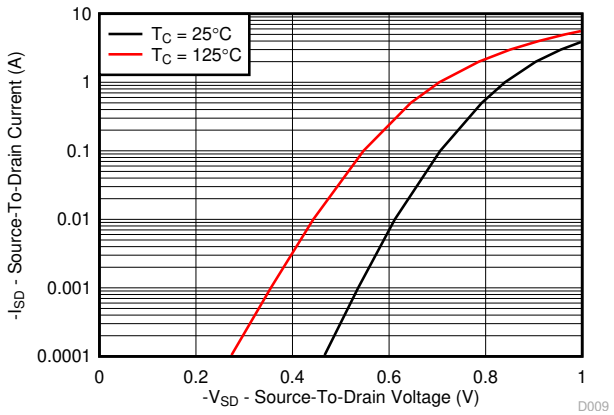
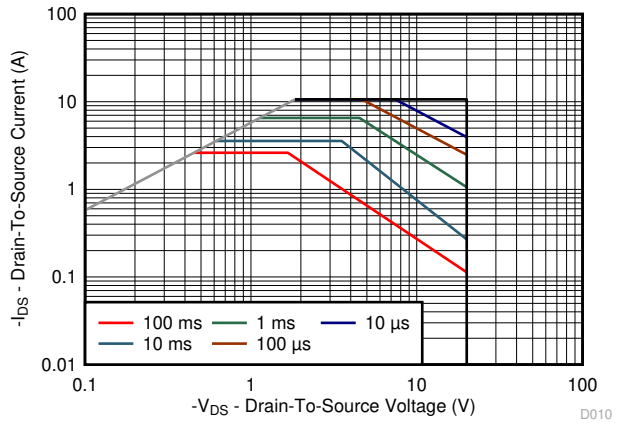


Figure 5-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JA}$ = 245°C/W

Figure 5-10. Maximum Safe Operating Area

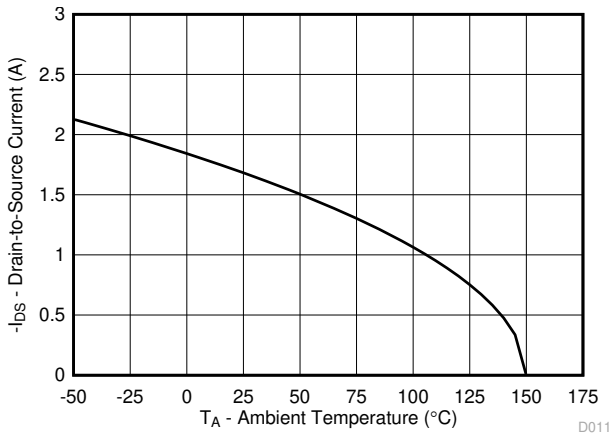


Figure 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
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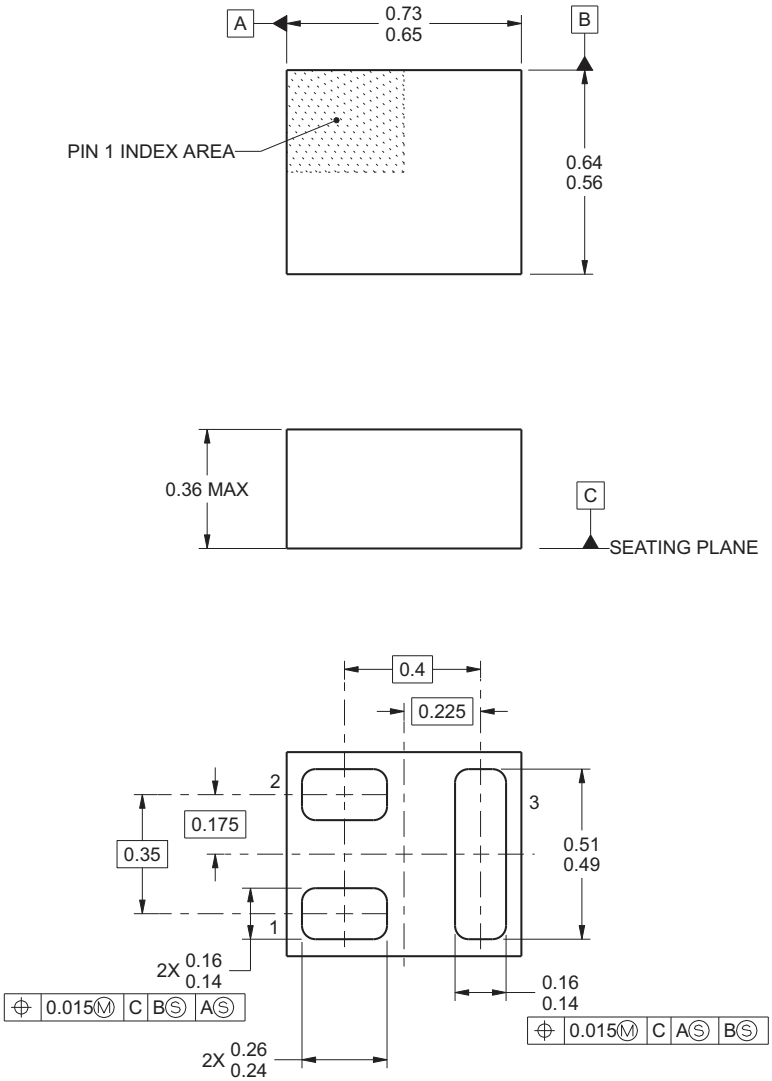
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

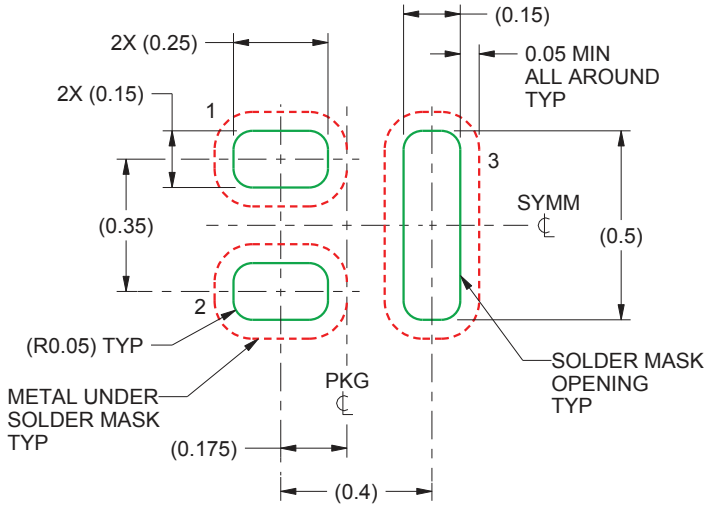


A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a lead-free solder land design.

Table 7-1. Pin Configuration

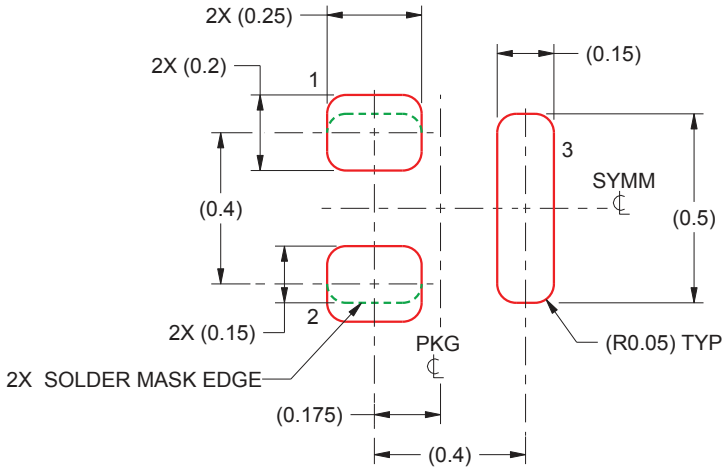
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

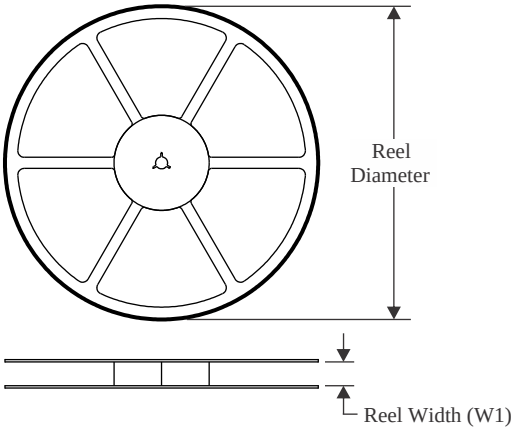
7.3 Recommended Stencil Pattern



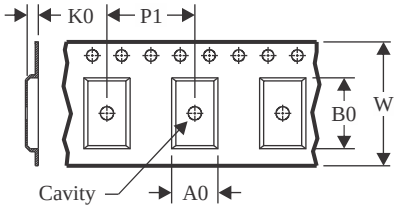
A. All dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

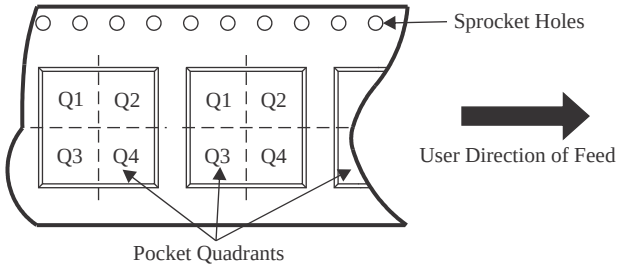


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

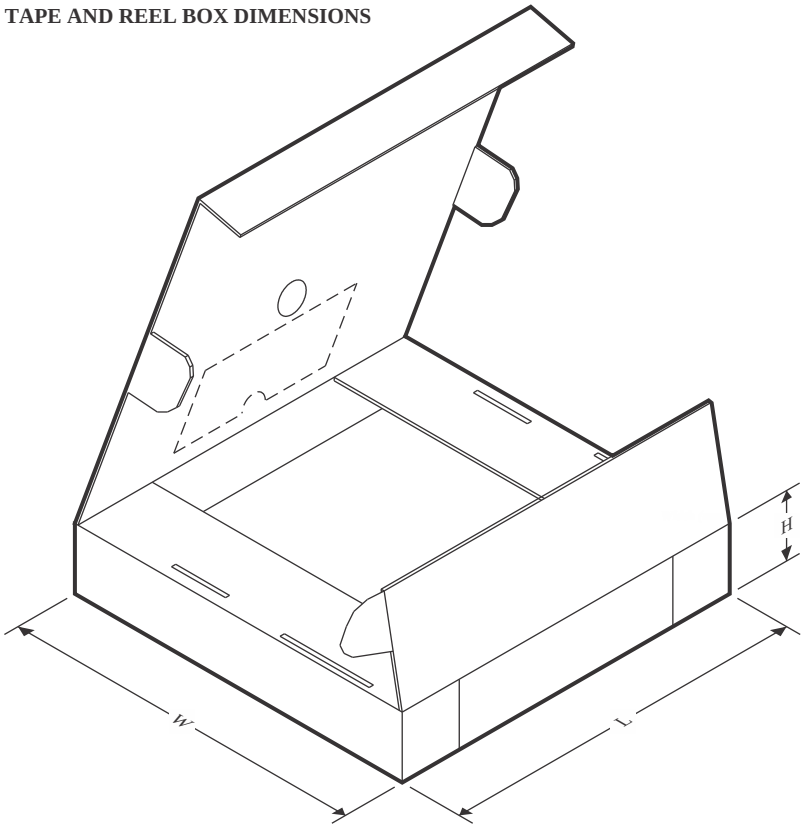
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25480F3	PICOSTAR	YJM	3	3000	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
CSD25480F3T	PICOSTAR	YJM	3	250	178.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2
CSD25480F3T	PICOSTAR	YJM	3	250	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

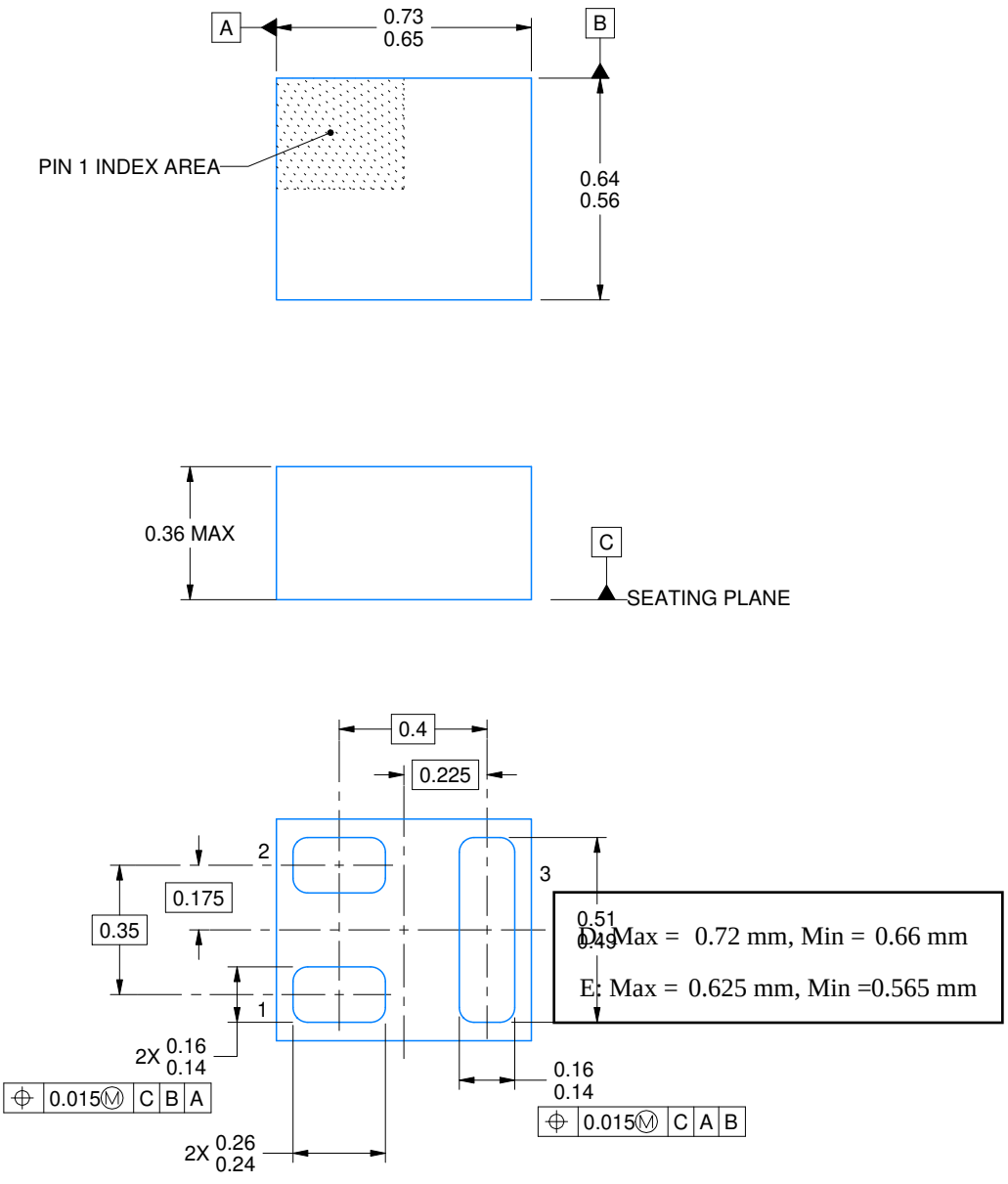
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25480F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD25480F3T	PICOSTAR	YJM	3	250	220.0	220.0	35.0
CSD25480F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0

YJM0003A

PACKAGE OUTLINE

PicoStar™ - 0.36 mm max height

PicoStar™



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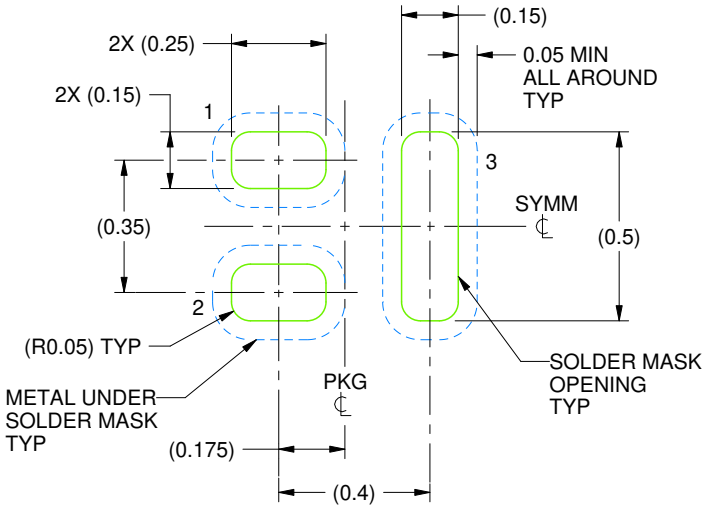
PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

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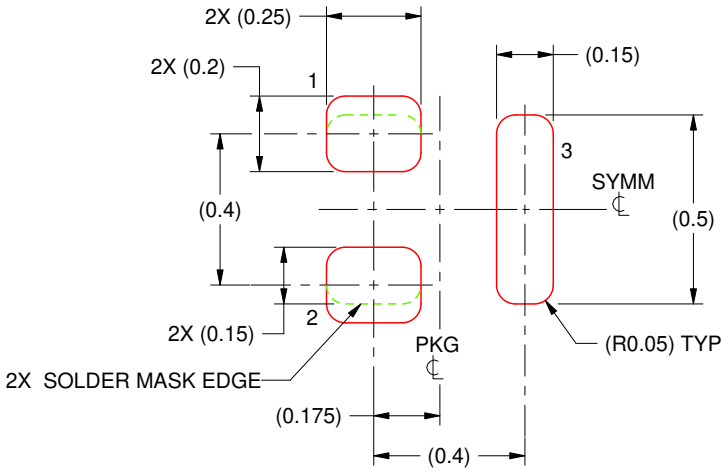
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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