Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

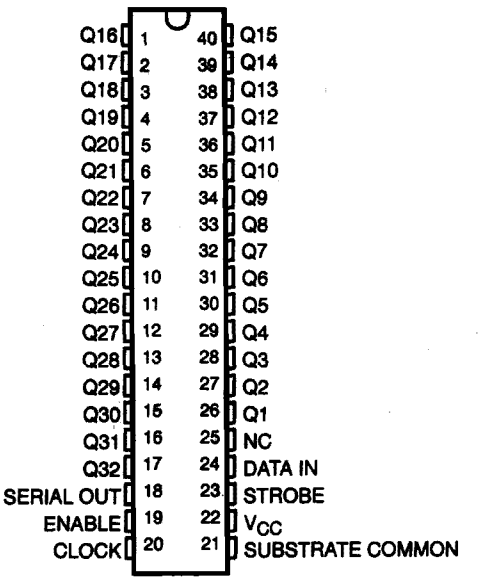
Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SLDS023B – D2743, MARCH 1983 – REVISED APRIL 1993

- **Each Device Drives 32 Electrodes**
- **High-Voltage Open-Drain DMOS Outputs**
- **50-mA Output Current Capability**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

SN65551 . . . N PACKAGE
(TOP VIEW)



NC – No internal connection

description

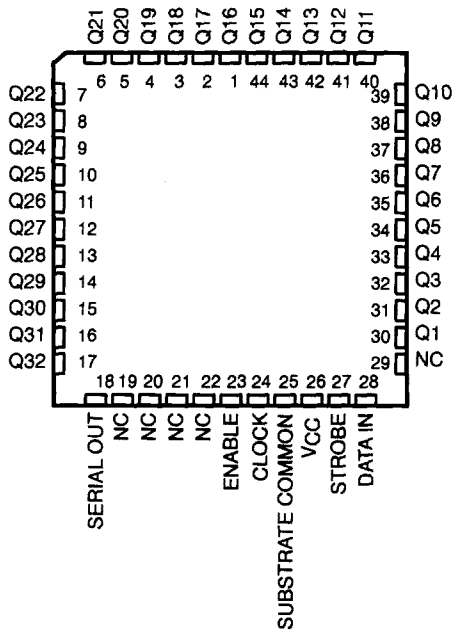
The SN65551, SN65552, SN75551, and SN75552 are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible and all outputs are high-voltage open-drain DMOS transistors. The SN75552 output sequence is reversed from the SN75551 for ease in printed-circuit-board layout.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to SUBSTRATE COMMON. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at ENABLE allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The serial data output (SERIAL OUT) from the shift register can be used to cascade additional devices. This output is not affected by ENABLE or STROBE.

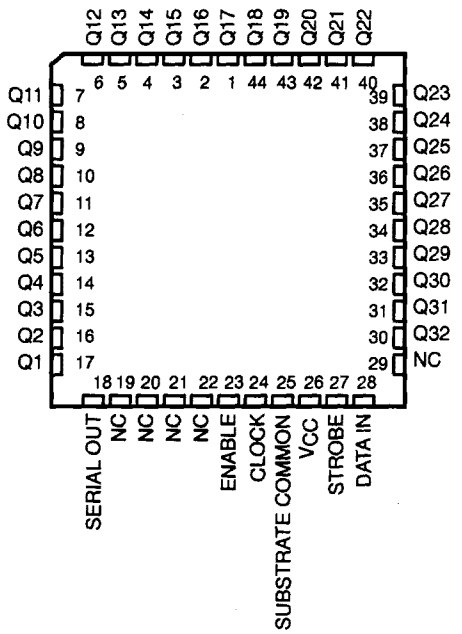
The SN65551 and SN65552 are characterized for operation from –40°C to 85°C. The SN75551 and SN75552 are characterized for operation from 0°C to 70°C.

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

SN65551, SN75551 . . . FN PACKAGE
(TOP VIEW)

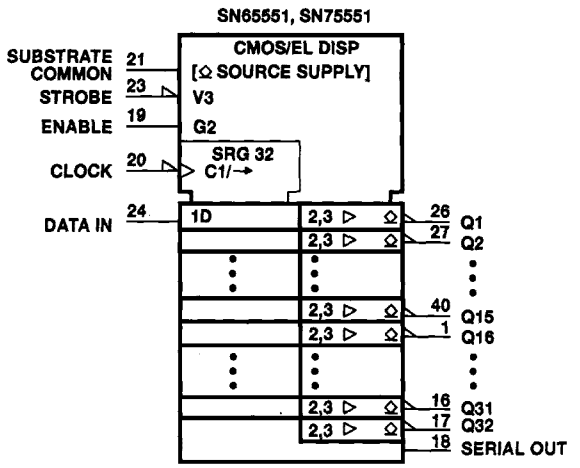


SN65552, SN75552 . . . FN PACKAGE
(TOP VIEW)



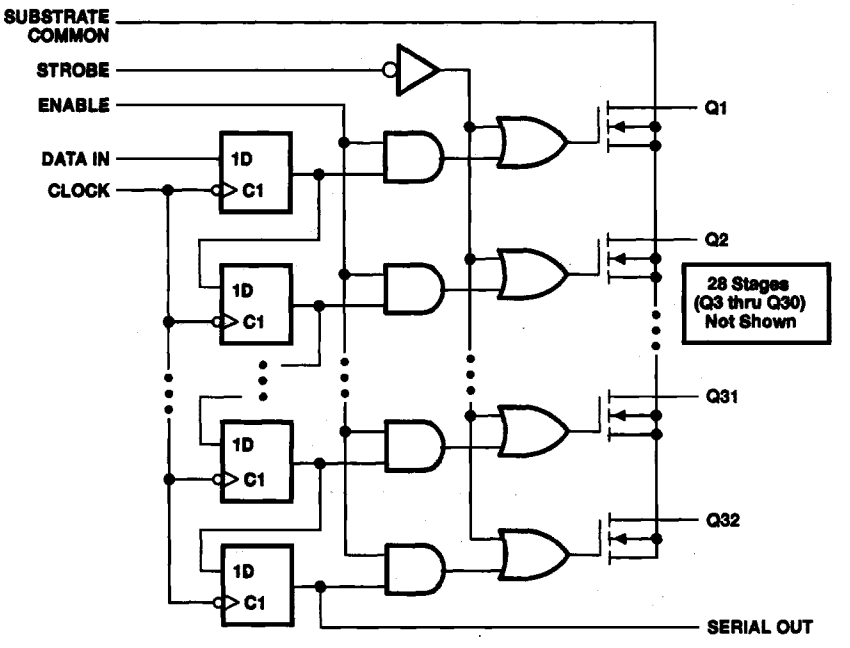
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The symbol ⏀ here indicates an n-channel open-drain output.
Pin numbers shown are for the N package.

logic diagram (positive logic)



FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	ENABLE	STROBE		SERIAL	Q1 THRU Q32
Load	↓	X	X	Load and shift†	R32	Determined by ENABLE and STROBE
	No ↓	X	X	No change	R32	Determined by ENABLE and STROBE
Enable	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
Strobe	X	X	L	As determined above	R32	All Q outputs on

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.

† Register R32 takes on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

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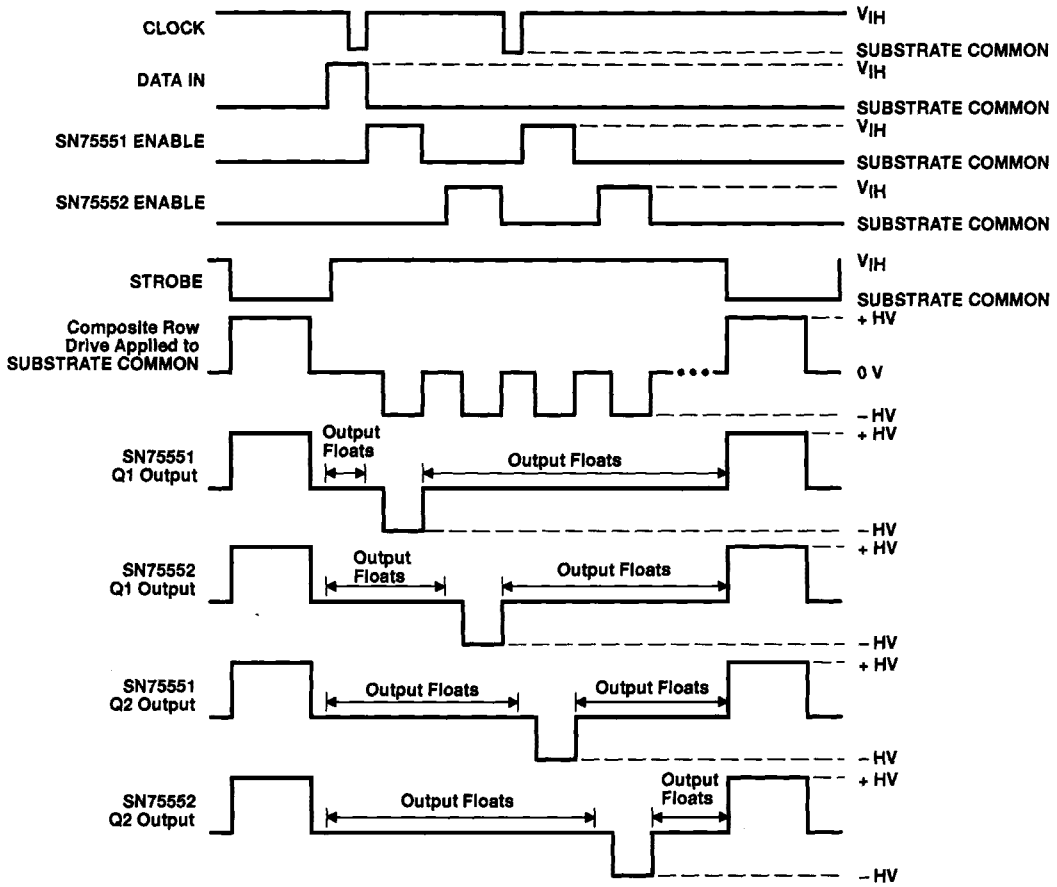
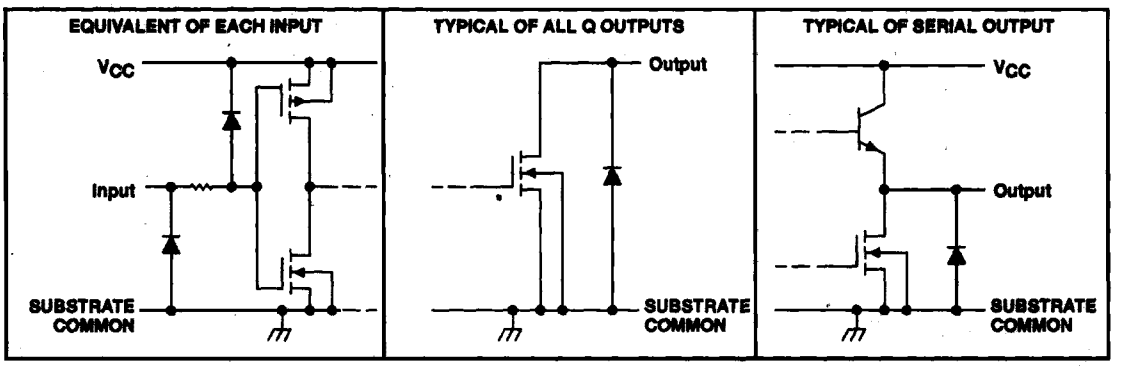
typical operating sequence



HV = high voltage

NOTE: During operation, CLOCK, DATA IN, ENABLE, and STROBE are referenced to the composite row drive signal received at SUBSTRATE COMMON of the device.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 18 V
Off-state Q output voltage, $V_{O(off)}$ ..... 225 V
Input voltage ..... V_{CC} + 0.3 V
Substrate common terminal current (see Note 2) ..... 1.5 A
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65551, SN65552 ..... – 40°C to 85°C
SN75551, SN75552 ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTES: 1. Voltage values are with respect to SUBSTRATE COMMON.
2. Duty cycle is limited by package dissipation.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		10.8	12	15	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC} = 10.8 V	8.1		11.1	V
	V_{CC} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)	V_{CC} = 10.8 V	−0.3		2.7	V
	V_{CC} = 15 V	−0.3		3.75	
Off-state Q output voltage, $V_{O(off)}$		0		200	V
On-state output current, duty cycle ≤ 1%, $I_{O(on)}$ (see Figures 2, 3, and 4)	V_{CC} = 10.8 V, T_A = 25°C			50	mA
	V_{CC} = 15 V, T_A = 25°C			80	
Output clamp current, I_{OK}				−45	mA
Clock frequency, f_{clock}		0		4	MHz
Pulse duration, CLOCK high or low, t_w		125			ns
Setup time, DATA IN before CLOCK, t_{su} (see Figure 5)		50			ns
Hold time, DATA IN after CLOCK, t_h (see Figure 5)		100			ns
Operating free-air temperature, T_A	SN65551, SN65552	−40		85	°C
	SN75551, SN75552	0		70	

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	SERIAL OUT	I_O = −100 µA	V_{CC}−1.5		V
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 50 mA, See Figure 3		30	V
		SERIAL OUT	I_{OL} = 100 µA		1	
$I_{O(off)}$	Off-state Q-output current		V_O = 200 V		10	µA
I_{IH}	High-level input current		$V_I = V_{CC}$		1	µA
I_{IL}	Low-level input current		V_I = 0		−1	µA
I_{CC}	Supply current from V_{CC}				250	mA

switching characteristics, V_{CC} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level, SERIAL OUT from CLOCK	C_L = 20 pF to GND, See Figure 6		200	ns
t_{PLH}	Propagation delay time, low-to-high level, SERIAL OUT from CLOCK			200	ns
$t_{d(on)}$	Turn-on delay time, Q outputs from ENABLE	I_{OL} = 50 mA, STROBE at V_{CC}, R_L = 1.4 kΩ to 100 V, See Figure 7		500	ns

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS
vs
SUPPLY VOLTAGE V_{CC}

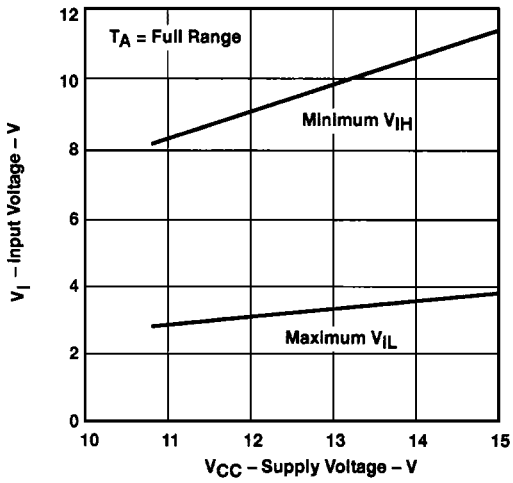


Figure 1

MAXIMUM ON-STATE Q OUTPUT CURRENT
vs
SUPPLY VOLTAGE

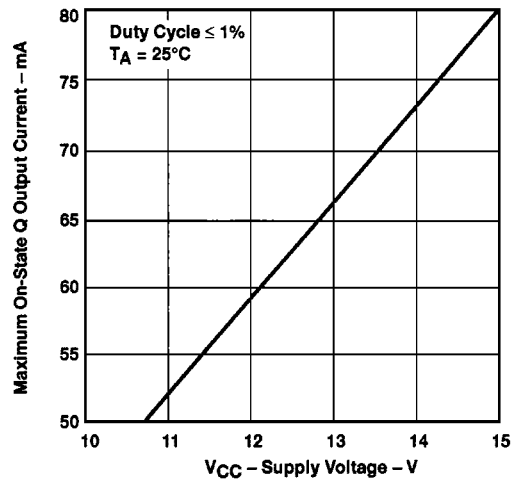
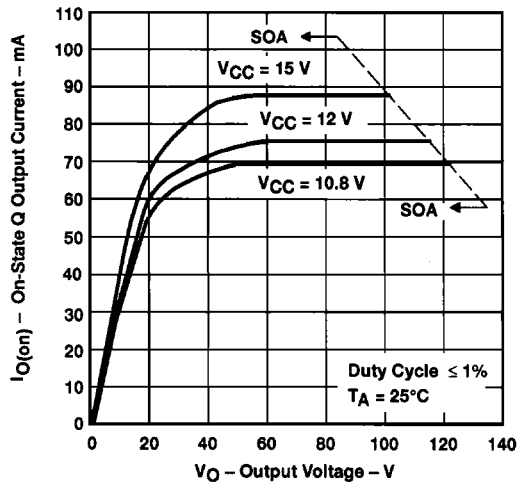


Figure 2

ON-STATE Q OUTPUT CURRENT
vs
OUTPUT VOLTAGE



SOA = Safe Operating Area

Figure 3

OUTPUT SATURATION CURRENT
vs
FREE-AIR TEMPERATURE†

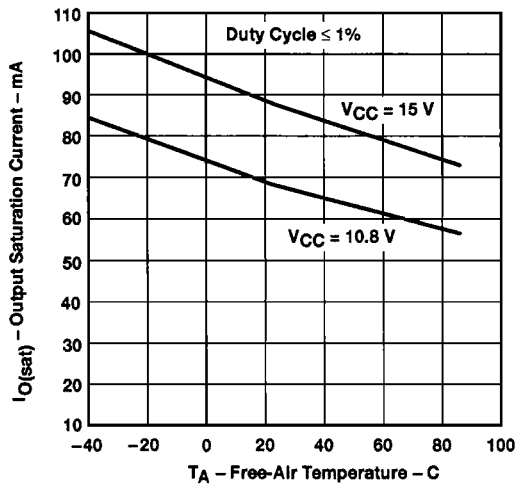


Figure 4

† Data for temperatures between 0°C and 70°C apply only for the SN75551 and SN75552 devices.

PARAMETER MEASUREMENT INFORMATION

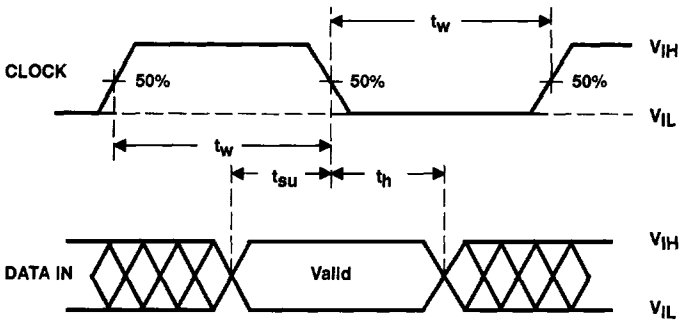


Figure 5. Input Timing Voltage Waveforms

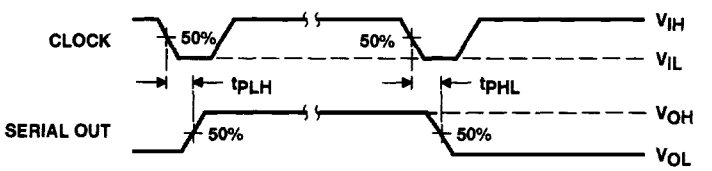


Figure 6. Voltage Waveforms, SERIAL OUT

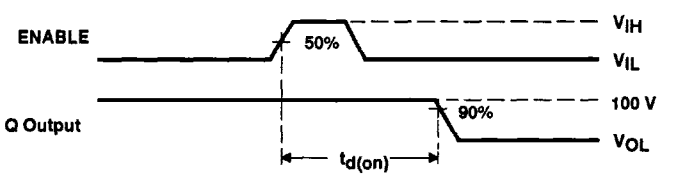


Figure 7. Voltage Waveforms, Q Outputs