20-Output PCIe Gen 1, 2 ,3, 4 and 5 Buffer with Ultra-Low Additive Jitter

Features

- Fully Compliant with PCIe 1, 2, 3, 4 and 5 Specifications
- 20 Low-Power Push-Pull HCSL PCIe Outputs
- Ultra-low additive jitter: 10fs maximum
- Supports clock frequencies from 0 to 250MHz
- Supports 3.3V power supplies
- Embedded Low Drop Out (LDO) Voltage regulator provides superior Power Supply Noise Rejection
- Maximum output to output skew of 50ps
- SMBus Interface
- Eight OE pins
- Embedded series terminations adjusted for 100Ω differential transmission line
- Transparent for Spread-Spectrum Clock

Ordering Information

ZL40293LDG1	72 pin QFN	Trays
ZL40293LDF1	72 pin QFN	Tape and Reel

Package size: 10 x 10 mm

-40°C to +85°C

Applications

- PCI Express generation 1/2/3/4/5 clock distribution
- Intel QPI
- Servers
- Storage and Data Centers
- Switches and Routers

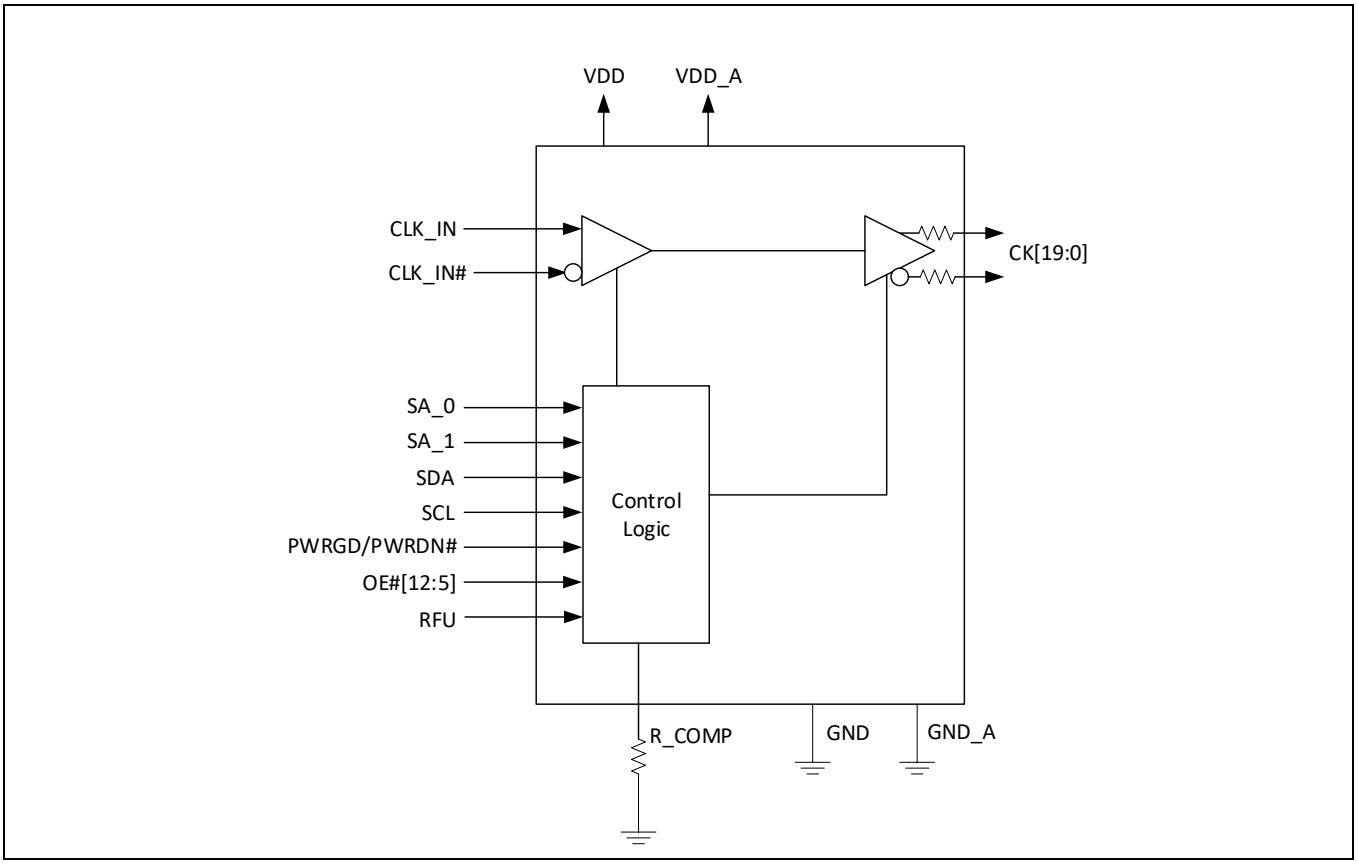

Figure 1. Functional Block Diagram

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Pin Diagram

The device is packaged in a 10x10mm 72-pin QFN.

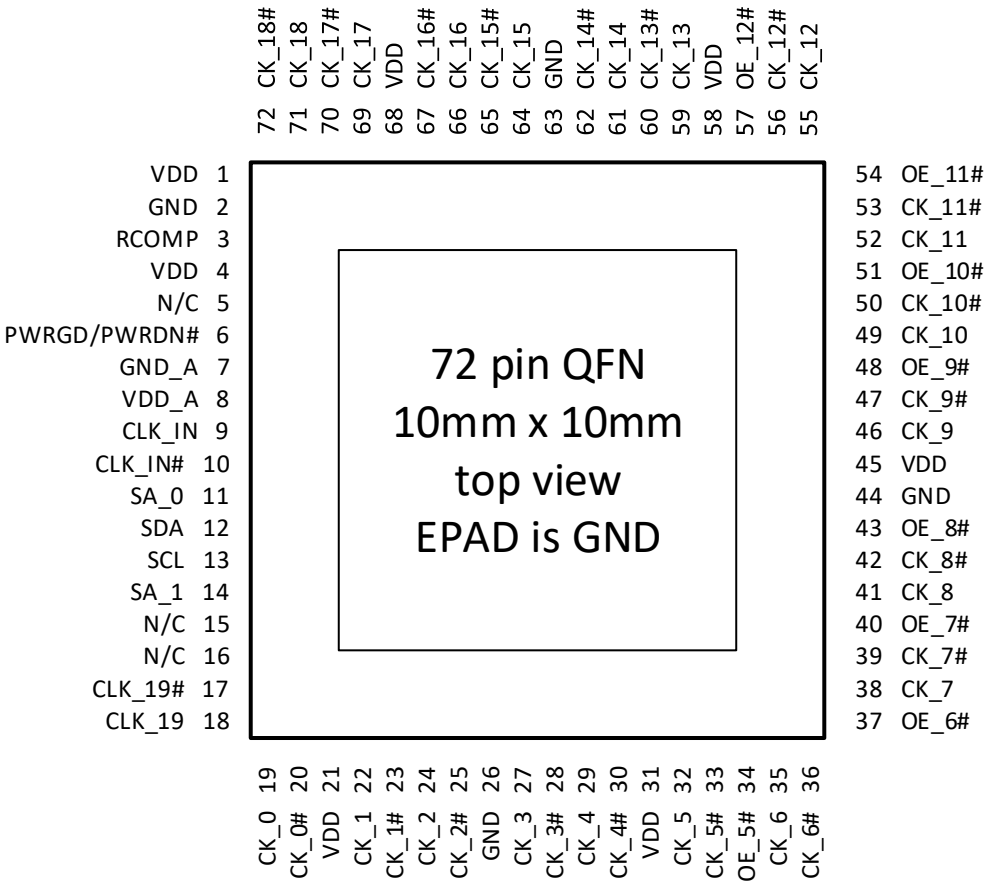


Figure 2. Pin Diagram

Pin Descriptions

The I/O column uses the following symbols: I – input, I_{PU} – input with 120kΩ internal pull-up resistor, I_{PD} – input with 300kΩ internal pull-down resistor, O – output, I/O – Input/Output Drain pin, NC-No connect pin, P – power supply pin, . I_{TRI} – Tri-level input pin biased to VDD/2 by internal 120kΩ pull-up and 120kΩ pull-down resistor.

Table 1Pin Descriptions

#	Name	I/O	Description
Input Reference			
9 10	CLK_IN CLK_IN#	I	**Input Differential or Single Ended Reference** Input frequency range 0Hz to 250MHz.
Output Clocks			
19 20 22 23 24 25 27 28 29 30 32 33 35 36 38 39 41 42 46 47 49 50 52 53 55 56 59 60 61 62 64 65	CK_0 CK_0# CK_1 CK_1# CK_2 CK_2# CK_3 CK_3# CK_4 CK_4# CK_5 CK_5# CK_6 CK_6# CK_7 CK_7# CK_8 CK_8# CK_9 CK_9# CK_10 CK_10# CK_11 CK_11# CK_12 CK_12# CK_13 CK_13# CK_14 CK_14# CK_15 CK_15#	O	**Ultra-Low Additive Jitter Differential Outputs 0 to 19** Output frequency range 0 to 250MHz

<table>
<tr><td>66
67
69
70
71
72
17
18</td><td>CK_16
CK_16#
CK_17
CK_17#
CK_18
CK_18#
CK_19#
CK_19</td><td></td><td></td></tr>
<tr><td colspan="4">Hardware Control</td></tr>
<tr><td>34
37
40
43
48
51
54
57</td><td>OE_5#
OE_6#
OE_7#
OE_8#
OE_9#
OE_10#
OE_11#
OE_12#</td><td>I_{PD}</td><td>Output Enable. Logic level on these pins enables/disables the corresponding output.
<table><tr><td>OE_n#</td><td>CK_n/n#</td></tr><tr><td>0</td><td>Active</td></tr><tr><td>1</td><td>Low/Low both pulled low by 50 Ω resistor</td></tr></table></td></tr>
<tr><td>6</td><td>PWRGD/PWRDN#</td><td>I</td><td>Power up / power down</td></tr>
<tr><td>3</td><td>R_COMP</td><td>I</td><td>Not used</td></tr>
<tr><td colspan="4">SMBus Control</td></tr>
<tr><td>13</td><td>SCL</td><td>I</td><td>SMBus slave clock input</td></tr>
<tr><td>12</td><td>SDA</td><td>I/O</td><td>Input/Open drain SMBus data</td></tr>
<tr><td>11
14</td><td>SA_0
SA_1</td><td>I_{TRI}</td><td>Tri level address selection inputs</td></tr>
<tr><td colspan="4">Power and Ground</td></tr>
<tr><td>1
4
21
31
45
58
68</td><td>VDD</td><td>P</td><td>Positive Supply Voltage. Connect to 3.3V supply.</td></tr>
<tr><td>8</td><td>VDD_A</td><td>P</td><td>Positive Analog Supply Voltage Connect 3.3V power supply.</td></tr>
<tr><td>2
26
44
63</td><td>GND</td><td>P</td><td>Ground Connect to ground</td></tr>
<tr><td>7</td><td>GND_A</td><td>P</td><td>Analog Ground. Connect to ground</td></tr>
</table>

E-Pad	GND	P	**Ground.** Connect to ground
No Connect Pins			
5 15 16	N/C		**No Connect.** These pins are not connected to the die. Leave them open.

Functional Description

The ZL40293 is an ultra-low additive jitter, low power 1 to 20 fanout buffer which is fully compliant with PCIe Gen 1, 2, 3, 4 and 5 Standards.

The device operates from 3.3V+/-5% supply as per Intel spec. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40293 inputs.

The device input can be fed with transmission lines of any impedance. Examples below show only 50 Ω single ended, 85 Ω differential and 100 Ω differential which are the most common ones in practice. Figure 3 and Figure 4 show how to terminate the input when driven from a push-pull and traditional HCSL drivers respectively.

Figure 5 shows how to terminate a single ended output such as LVCMOS. This example assumes 50 Ω transmission line which is the most common for single ended CMOS signaling. Resistors R1 and R2 are chosen to provide 50 Ω termination and proper biasing and Ro + Rs ideally should be 50 Ω so that the transmission line is terminated at both ends with its characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Figure 5). The source resistors of Rs = 270Ω could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270Ω + 50Ω)) = 5.16mA.
For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

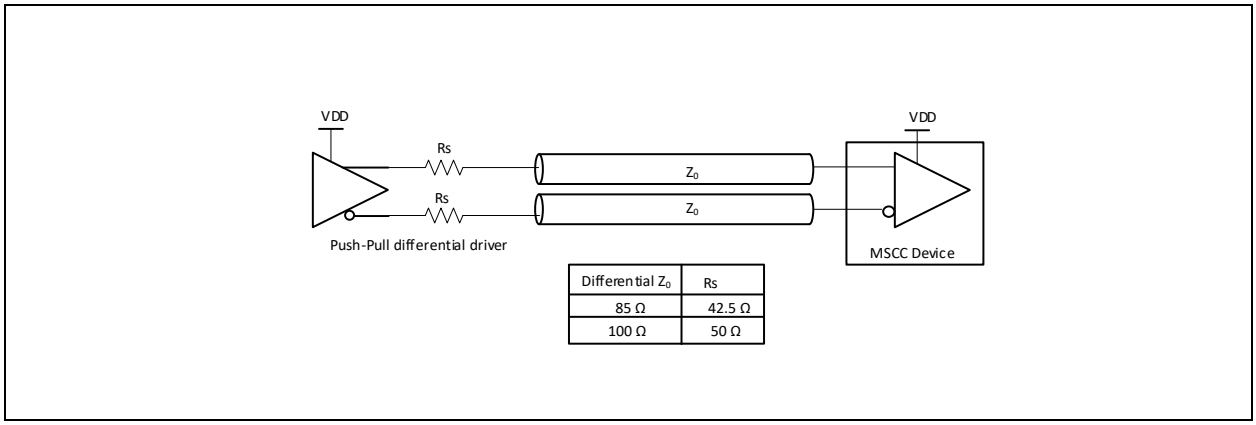


Figure 3. Input driven by a push-pull differential output

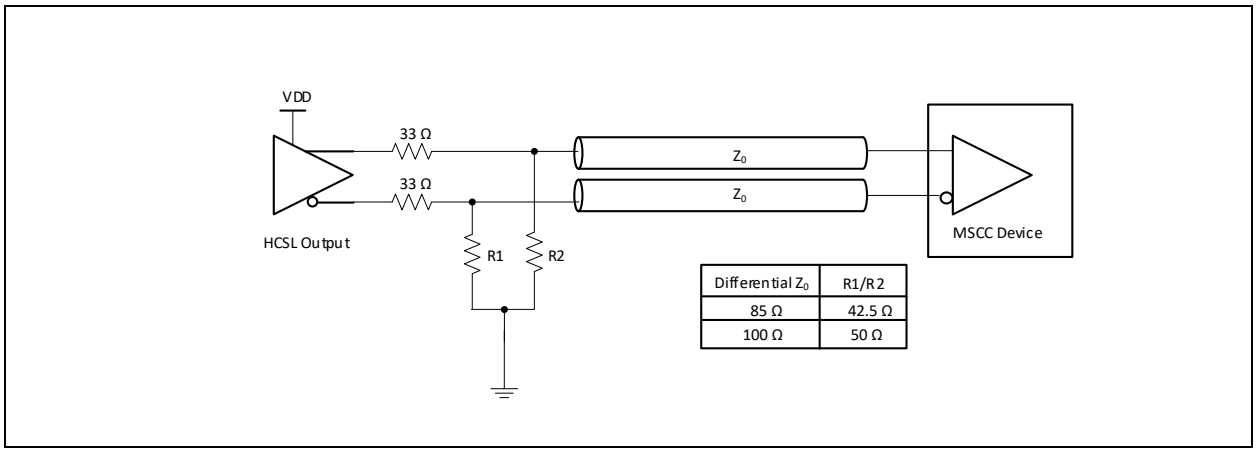


Figure 4. Input driven by an HCSL output

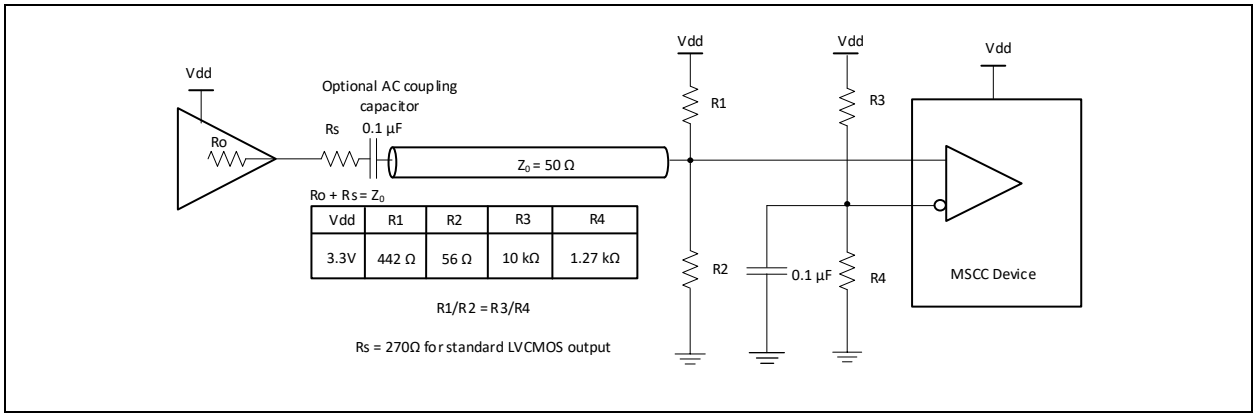


Figure 5. Input driven by a single ended output

Clock Outputs

Differential outputs have embedded termination resistors as shown in Figure 6. This provides significant saving relative to traditional current based HCSL outputs which require four resistors per differential pair (80 resistors for 20 outputs).

Embedded series termination resistors are matched for 100Ω differential transmission line.

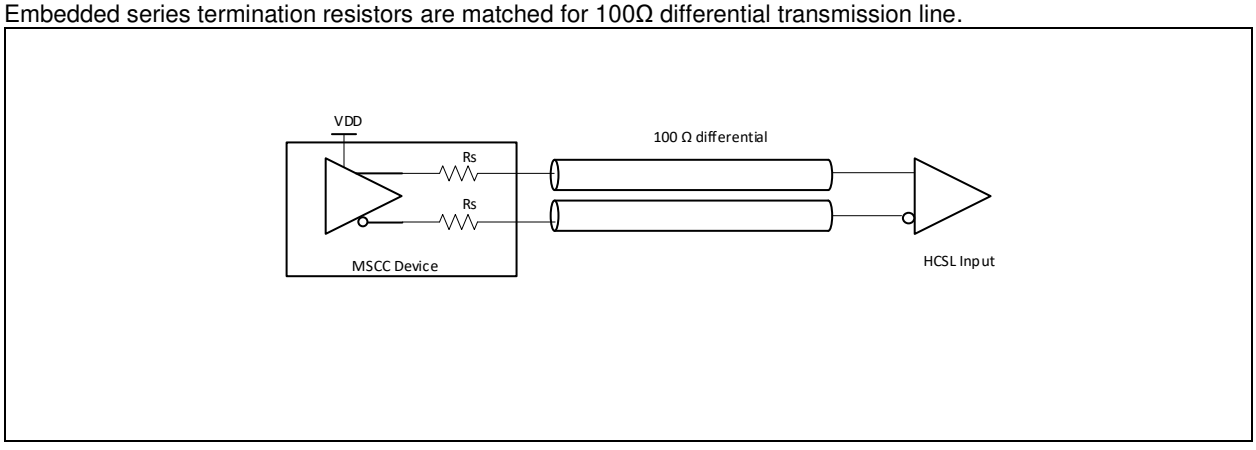


Figure 6. Terminating differential outputs.

Termination of unused outputs

Unused outputs should be left unconnected.

Power Supply Filtering

Each power pin (VDDA and VDD) should be decoupled with 0.1µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulated with low DC resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling.

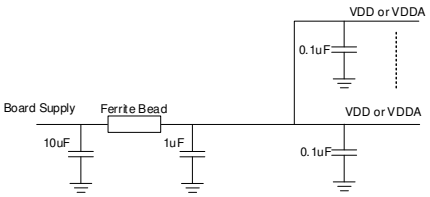


Figure 7. Power Supply Filtering

OE# and Output Enables (Control Register)

Each output can be individually enabled or disabled by SMBus control register bits or via OE# pin. The OE# pins are asynchronous asserted-low signals. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

OE# pins are mapped to CK[12:5] outputs.

Note that the logic level for assertion or de-assertion is different in software than it is on hardware. This follows hardware default nomenclature for communication channels (e.g., output is enabled if OE# pin is pulled low) and still maintains software programming logic (e.g., output is enabled if OE register is true).

Refer to Table 2 for the truth table for enabling and disabling outputs via hardware and software. Note that both the control register bit must be a ‘1’ AND the OE# pin must be a ‘0’ for the output to be active.

Table 2 OE Functionality

Inputs		OE# Hardware Pins and Control Register Bits			
PWRGD/ PWRDN#	CK_IN/ CK_IN#	SMBUS Enable Bit	OE# Pin	CK/CK# [12:5]	CK/CK# [4:0] and [19:13]
0	X	X	X	0	0
1	Running	0	X	0	0
		1	0	Running	Running
		1	1	0	Running

OE# Assertion (Transition from ‘1’ to ‘0’)

All differential outputs that were disabled are to resume normal operation in a glitch free manner. The latency from the assertion to active outputs is 0 - 10 CK clock periods.

OE# De-Assertion (Transition from '0' to '1')

The impact of de-asserting OE# is each corresponding output will transition from normal operation to disabled in a glitch free manner. A minimum of four valid clocks will be provided after the de-assertion of OE#. The maximum latency from the de-assertion to disabled outputs is 10 CK clock periods.

PWRGD / PWRDN#

PWRGD is asserted high and de-asserted low. De-assertion of PWRGD (pulling the signal low) is equivalent to indicating a powerdown condition. PWRGD (assertion) is used by the ZL40293 to sample initial configurations such as SA selections.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin which is used to disable (drive low/low) all clocks cleanly and instruct the device to invoke power savings mode. PWRDN# is a completely asynchronous active low input. When entering power savings mode, PWRDN# should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When PWRDN# is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters.

The assertion and de-assertion of PWRDN# is asynchronous.

Disabling of the CK_IN input clock prior to assertion of PWRDN# is an undefined mode and not recommended. Operation in this mode may result in glitches.

Table 3 PWRGD / PWRDN# Functionality

PWRGD / PWRDN#	CK	CK#
0	LOW	LOW
1	Normal	Normal

PWRDN# Assertion

When PWRDN# is sampled low by two consecutive rising edges of CK#, all differential outputs will be disabled on the next CK# high to low transition.

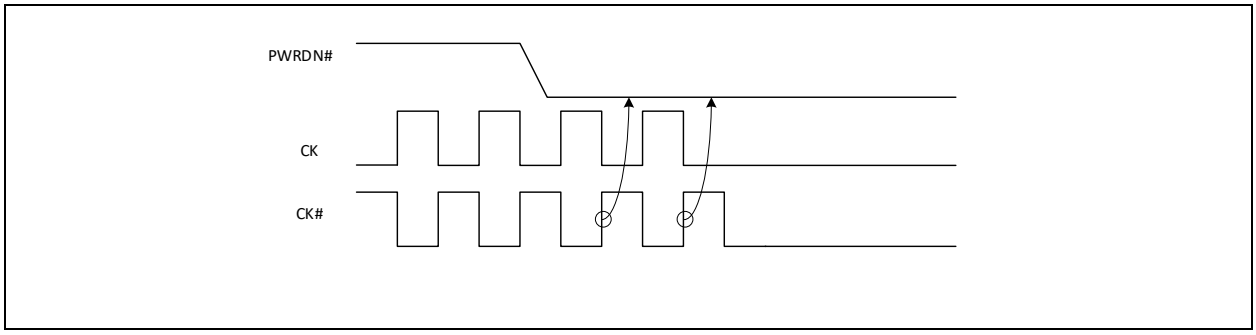


Figure 8. PWRDN# Assertion

PWRGD Assertion

PWRGD to the clock buffer should not be asserted before V_{DD} reaches V_{DDmin}. Prior to V_{DDmin} it is recommended to hold PWRGD low (less than 0.5 V)

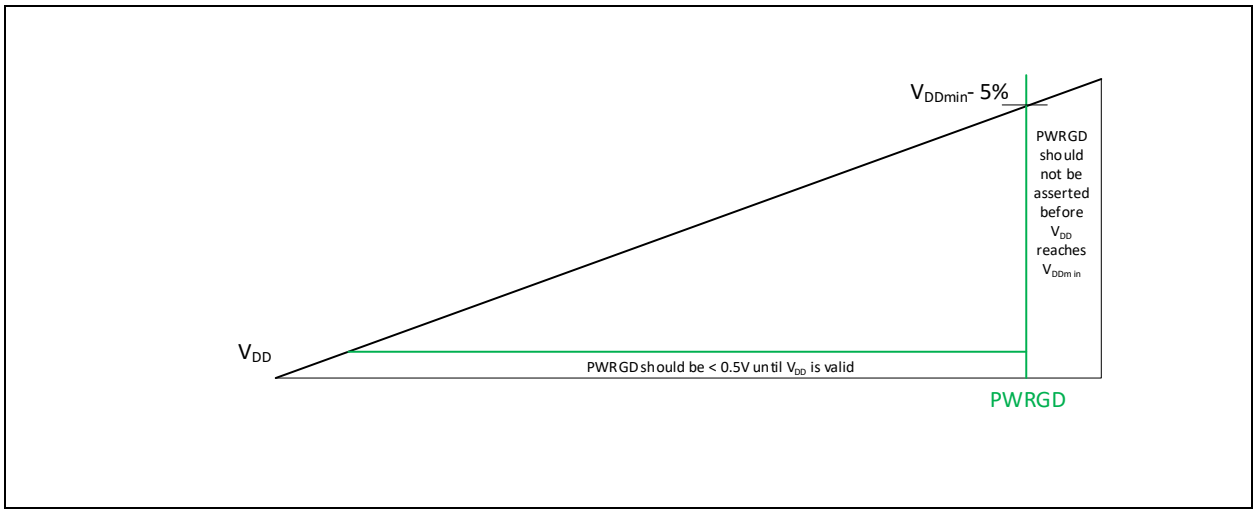


Figure 9. PWRGD and V_{DD} Relationship diagram

The power-up latency Tstable is to be less than 1.8 ms. This is the time from the valid CLK_IN input clocks and the assertion of the PWRGD signal to the time that stable clocks are output from the buffer chip. All differential outputs stopped in a disabled condition resulting from power down must be driven high in less than 300 µs of PWRGD assertion to a voltage greater than 200 mV.

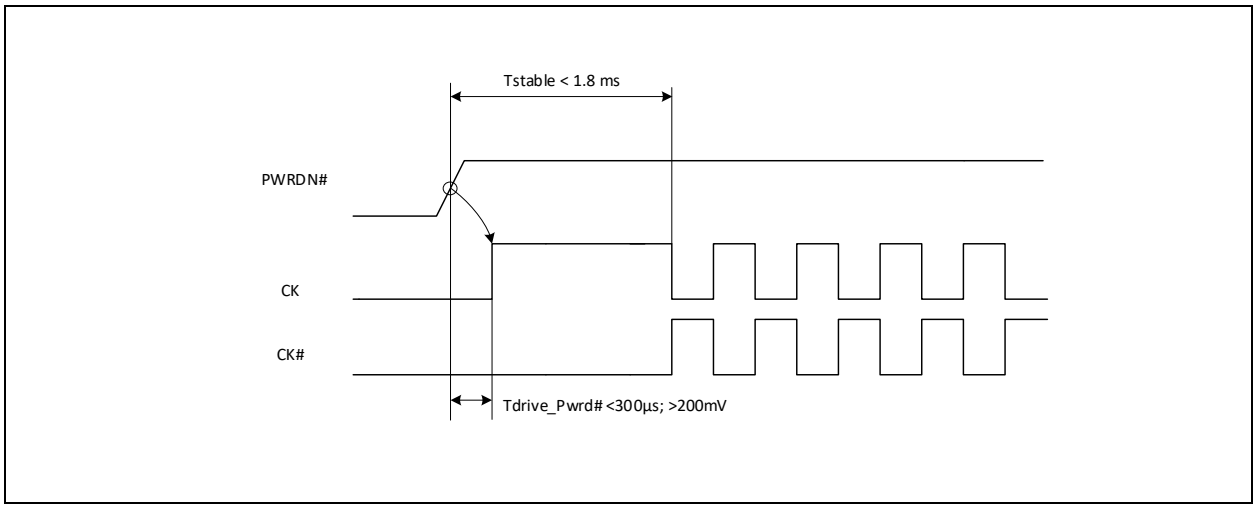


Figure 10. PWRGD Assertion

Programming via SMBus

The address selection is done via SA_0 and SA_1 tri-level hardware pins, which select the appropriate address for the device. The two tri-level input pins that can configure the ZL40293 to nine different addresses (refer to Table 15 for VIL_Tri, VIM_Tri, VIH_Tri signal level).

Table 4 SMBus Address Table

SA_1	SA_0	SMBus Address
L	L	D8
L	M	DA
L	H	DE
M	L	C2
M	M	C4
M	H	C6
H	L	CA
H	M	CC
H	H	CE

SMBus Byte Read/Write

Reading or writing a register in a SMBus slave device in byte mode always involves specifying the register number.

Read. The standard byte read is as shown in Figure 11. It is an extension of the byte write. The write start condition is repeated then the slave device starts sending data and the master acknowledges it until the last byte is sent. The master terminates the transfer with a NAK then a stop condition. For byte operation, the 2*7th bit of the command byte must be set. For block operations, the 2*7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count.

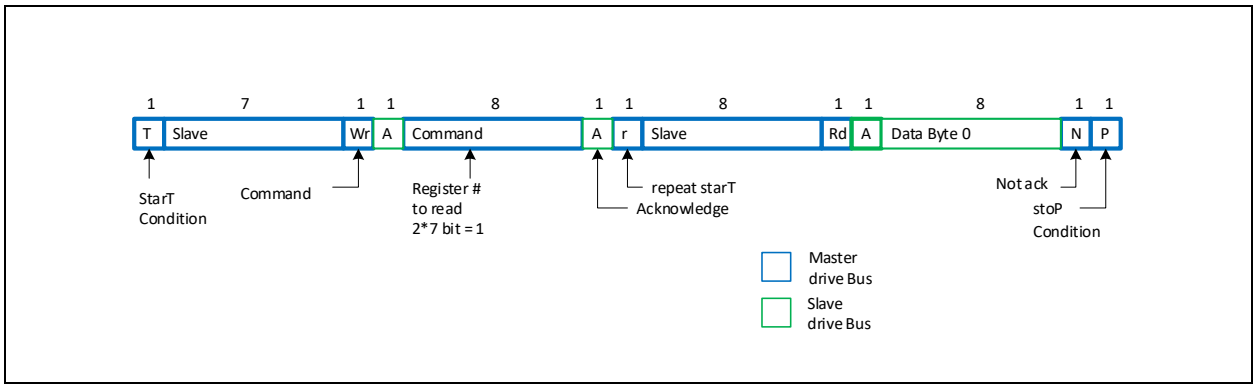


Figure 11. SMBus Byte Read

Write. Figure 12 illustrates a simple typical byte write. For byte operation the 2*7th bit of the command byte must be set. For block operations, the 2*7th bit must be reset. If the bit is not set the next byte must be the byte transfer count. The count can be between 1 and 32. It cannot be zero or exceed 32.

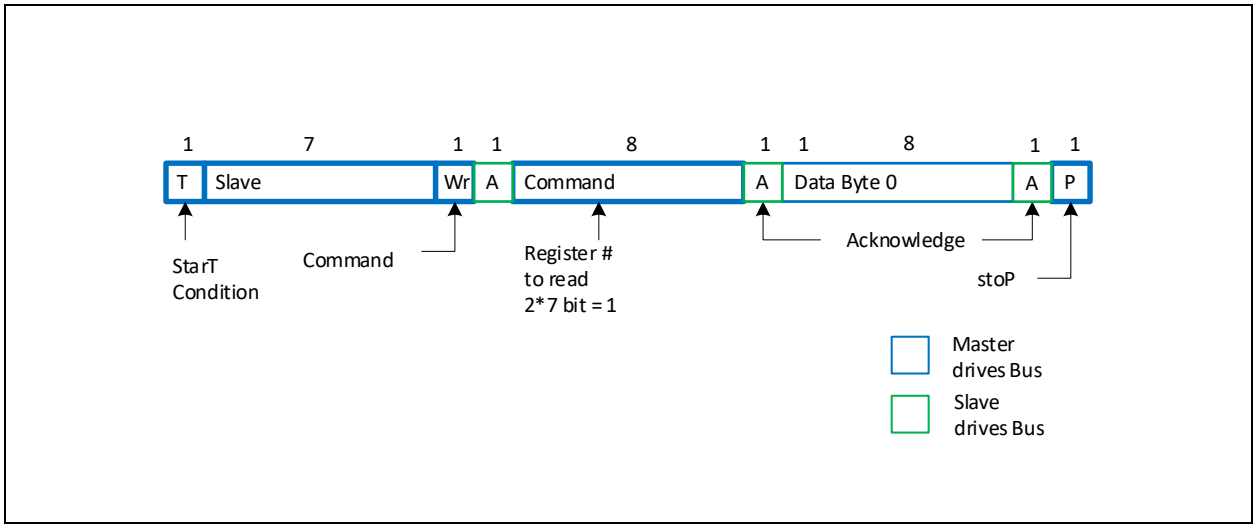


Figure 12. SMBus Byte Write

SMBus Block Read/Write

Read. After the slave address is sent with the r/w condition bit *set*, the command byte is sent with the MSB = 0. The slave Ack's the register index in the command byte. The master sends a repeat start function. After the slave Ack's this the slave sends the number of bytes it wants to transfer (>0 and <33). The master Ack's each byte except the last and sends a stop function.

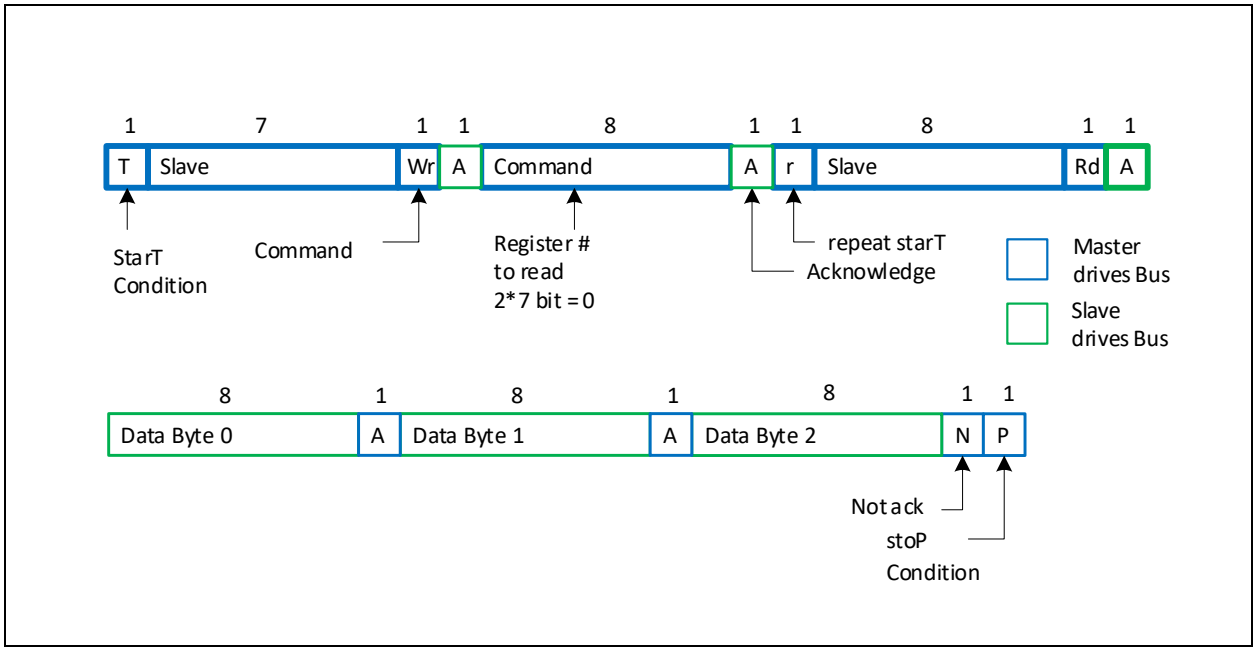


Figure 13. SMBus Block Read

Write. After the slave address is sent with the r/w condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate what register to start the transfer at. If the command byte is 00h, the slave device will be compatible with existing block mode slave devices. The next byte of a write must be the count of bytes that the master will transfer to the slave device. The byte count must be greater than zero and less than 33. Following this byte are the data bytes to be transferred to the slave device. The slave device always acknowledges each byte received. The transfer is terminated after the slave sends the Ack and the master sends a stop function.

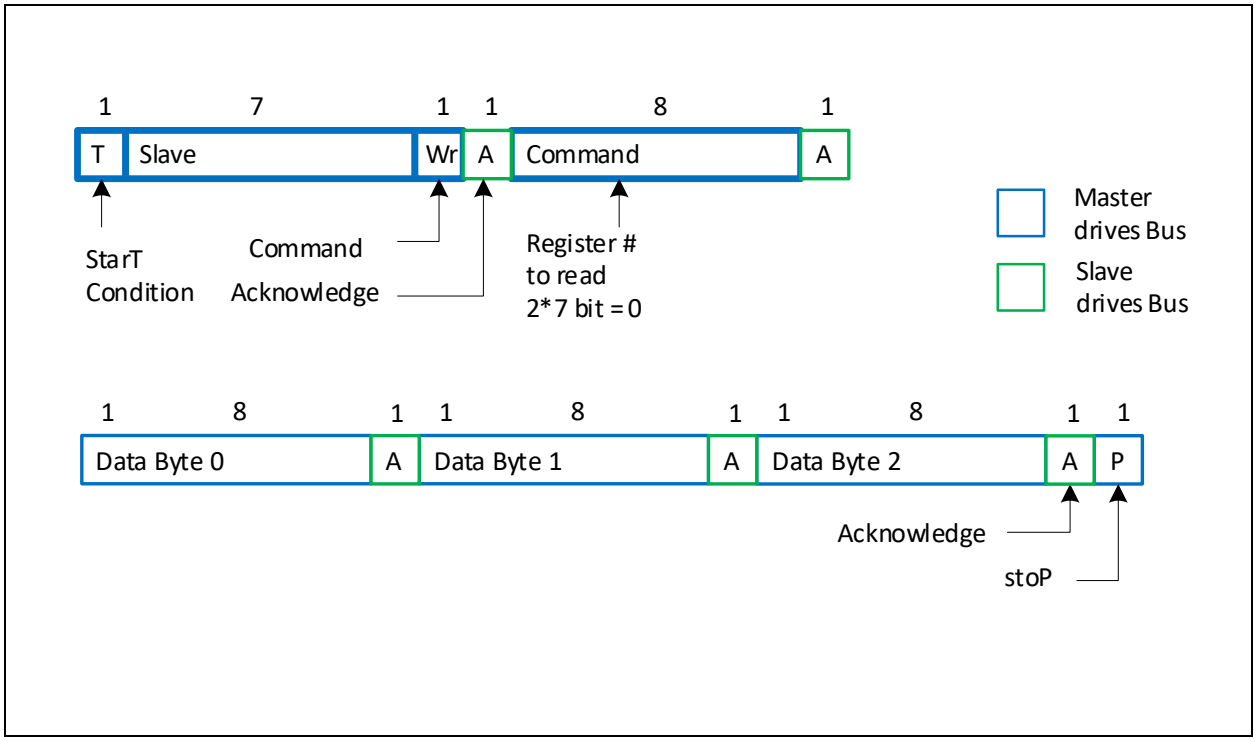


Figure 14. SMBus Block Write

Register Map

Table 5 Byte 0: Output Enable

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Reserved				0	
1	Reserved				0	
2	Reserved				0	
3	Output Enable CK 16	LOW	Enable	RW	1	CK[16]
4	Output Enable CK 17	LOW	Enable	RW	1	CK[17]
5	Output Enable CK 18	LOW	Enable	RW	1	CK[18]
6	Output Enable CK 19	LOW	Enable	RW	1	CK[19]
7	Reserved				0	

Table 6 Byte 1: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable CK 0	LOW	Enabled	RW	1	CK[0]
1	Output Enable CK 1	LOW	Enabled	RW	1	CK[1]
2	Output Enable CK 2	LOW	Enabled	RW	1	CK[2]
3	Output Enable CK 3	LOW	Enabled	RW	1	CK[3]
4	Output Enable CK 4	LOW	Enabled	RW	1	CK[4]
5	Output Enable CK 5	LOW	Enabled	RW	1	CK[5]
6	Output Enable CK 6	LOW	Enabled	RW	1	CK[6]
7	Output Enable CK 7	LOW	Enabled	RW	1	CK[7]

Table 7 Byte 2: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable CK 8	LOW	Enabled	RW	1	CK[8]
1	Output Enable CK 9	LOW	Enabled	RW	1	CK[9]
2	Output Enable CK 10	LOW	Enabled	RW	1	CK[10]
3	Output Enable CK 11	LOW	Enabled	RW	1	CK[11]
4	Output Enable CK 12	LOW	Enabled	RW	1	CK[12]
5	Output Enable CK 13	LOW	Enabled	RW	1	CK[13]
6	Output Enable CK 14	LOW	Enabled	RW	1	CK[14]
7	Output Enable CK 15	LOW	Enabled	RW	1	CK[15]

Table 8 Byte 3: OE# Pin Realtime Readback Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Realtime Readback of OE_5#	OE_5# Low	OE_5# High	R	Realtime	CK[5]
1	Realtime Readback of OE_6#	OE_6# Low	OE_6# High	R	Realtime	CK[6]
2	Realtime Readback of OE_7#	OE_7# Low	OE_7# High	R	Realtime	CK[7]
3	Realtime Readback of OE_8#	OE_8# Low	OE_8# High	R	Realtime	CK[8]
4	Realtime Readback of OE_9#	OE_9# Low	OE_9# High	R	Realtime	CK[9]
5	Realtime Readback of OE_10#	OE_10# Low	OE_10# High	R	Realtime	CK[10]
6	Realtime Readback of OE_11#	OE_11# Low	OE_11# High	R	Realtime	CK[11]
7	Realtime Readback of OE_12#	OE_12# Low	OE_12# High	R	Realtime	CK[12]

Table 9 Byte 4: Reserved Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Reserved				0	
1	Reserved				0	
2	Reserved				0	
3	Reserved				0	
4	Reserved				0	
5	Reserved				0	
6	Reserved				0	
7	Reserved				0	

Table 10 Byte 5: Vendor/Revision Identification Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Vendor ID Bit 0			R	1	
1	Vendor ID Bit 1			R	1	
2	Vendor ID Bit 2			R	0	
3	Vendor ID Bit 3			R	0	
4	Revision Code Bit 0			R	0	
5	Revision Code Bit 1			R	1	
6	Revision Code Bit 2			R	0	
7	Revision Code Bit 3			R	0	

Table 11 Byte 6: Device ID Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Device ID 0			R	1	
1	Device ID 1			R	0	
2	Device ID 2			R	1	
3	Device ID 3			R	1	
4	Device ID 4			R	1	
5	Device ID 5			R	0	
6	Device ID 6			R	1	
7	Device ID 7 (MSB)			R	0	

Table 12 Byte 7: Byte Count Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	BC0 - Writing to this register configures how many bytes will be read back			RW	0	
1	BC1 - Writing to this register configures how many bytes will be read back			RW	0	
2	BC2 - Writing to this register configures how many bytes will be read back			RW	0	
3	BC2 - Writing to this register configures how many bytes will be read back			RW	1	
4	BC3 - Writing to this register configures how many bytes will be read back			RW	0	
5	BC4 - Writing to this register configures how many bytes will be read back			RW	0	
6	Reserved				0	
7	Reserved				0	

AC and DC Electrical Characteristics

Absolute Maximum Ratings

Table 13 Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Max.	Units	Notes
1	3.3 V Core Supply Voltage	V_{DD_A}	-	4.6	V	3
2	3.3 V I/O Supply Voltage	V_{DD}	-	4.6	V	3
5	3.3 V Input High Voltage	V_{IH}	-	4.6	V	1, 3
	3.3 V Input Low Voltage	V_{IL}	-0.5	-	V	3
	Storage Temperature	Ts	-65	150	°C	3
6	Input ESD protection	V_{DD-IN}	2000		V	2

* Exceeding these values may cause permanent damage
* Functional operation under these conditions is not implied
* Voltages are with respect to ground (GND) unless otherwise stated

1. Maximum VIH is not to exceed maximum VDD.
2. Human body model.
3. Consult manufacturer regarding extended operation in excess of normal DC operating parameters.

Current Consumption

Table 14 Current Consumption

	Parameter	Parameter Condition	Symbol	Min.	Typ.	Max	Units	Notes
1	Active Mode Supply Current	fIN = 100MHz All CK_xP/N outputs enabled	I_{DDPG}		196	210	mA	1,2
2		fIN = 100MHz All CK_xP/N outputs disabled			46	50		1,3
3		fIN = 133MHz All CK_xP/N outputs enabled			203	220		1,2
4		fIN = 133MHz All CK_xP/N outputs disabled			46	51		1,3
5	Power Down Mode Supply Current	fIN = 100MHz	I_{DDPD}		21	25	mA	1,4
6		fIN = 133MHz			22	26		1,4

1. VDD = 3.3V + 5%
2. Device operating in active mode (Pin PWRGD/PWRDN_N = 1) with all 20 CK_xP/N outputs enabled (all OE_xN pin = 0, all OCR1, OCR2, OCR3 register OEx bits = 1)
3. Device operating in active mode (Pin PWRGD/PWRDN_N = 1) with all 20 CK_xP/N outputs disabled (all OCR1, OCR2, OCR3 register OEx bits = 0)
4. Device operating in low power mode (Pin PWRGD/PWRDN_N=0)

DC Electrical Specification

Table 15 DC Operating Characteristics*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	3.3 V Core Supply Voltage	V_{DD_A}	3.135	3.3	3.465	V	
2	3.3 V I/O Supply Voltage	V_{DD}	3.135	3.3	3.465	V	
3	3.3 V Input High Voltage	V_{IH}	2.0		VDD+0.3	V	
4	3.3 V Input Low Voltage	V_{IL}	VSS-0.3		0.8	V	
5	Input Leakage Current	I_{IL}	-5		+5	µA	
6	Input Low Voltage, 3-level CMOS Input	V_{IL3}	VSS-0.3		0.9	V	
7	Input Midrange Voltage, 3-level CMOS Input	V_{IM3}	1.3		1.8	V	
8	Input High Voltage, 3-level CMOS Input	V_{IH3}	2.4		VDD	V	
9	Input Capacitance	C_{IN}			4.5	pF	1
10	Output Capacitance	C_{OUT}			4.5	pF	1
11	Ambient Temperature	T_A	-40		85	°C	

* Voltages are with respect to ground (GND) unless otherwise stated
1 For parasitic simulation use IBIS model.

Power Noise Tolerance

Table 16 Power Noise Tolerance*

	VDD Electrical Noise Range	Symbol	Min.	Typ.	Max	Units	Notes
1	f_{NOISE} = 12kHz to 20MHz	N_{VDD_MID}	100			mV,p-p	1,2,3
2	f_{NOISE} > 20MHz	N_{VDD_HIGH}	50			mV,p-p	1,2,3
3	f_{NOISE} = 12kHz to 20MHz	$N_{VDD\_A\_MID}$	40			mV,p-p	1,2,3
4	f_{NOISE} > 20MHz	$N_{VDD\_A\_HIGH}$	20			mV,p-p	1,2,3

* The device meets all specification in the presence of noise specified in this table
1 Jitter and electrical characteristics are met with specified AC noise present on any of the power pins.
2 Over the specified frequency range, a single sinusoid tone should be assumed swept as the worst case.
3 Maximum measured frequency for VDD was 650kHz and for VDD_A the maximum frequency was 900kHz due to limitation of the test setup.

PCIe Electrical Characteristics

PCIe measurement are related only to ZL40293 device. Test setup is shown Figure 20.

Table 17 PCIe Electrical Characteristics

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Rising edge rate	Rise_rate	1.4	1.6	2	V/ns	(2), (3)
2	Falling edge rate	Fall_rate	1.4	1.6	2	V/ns	(2), (3)
3	Differential High Voltage	V_{IH}	0.7			V	(2)
4	Differential Low Voltage	V_{IL}			-0.7	V	(2)
5	Single ended high voltage	V_{SIH}	0.7	0.76	0.82`	V	DC Measurement
6	Single ended low voltage	V_{SIL}	-0.05	0	0.05	V	DC Measurement
7	Absolute Crossing Voltage	V_{CROSS}	0.275		0.35	V	(1), (4), (5)
8	Variation of V_{CROSS} over all rising clock edges	ΔV_{CROSS}			0.08	V	(1), (4), (9)
9	Ring back voltage margin	V_{RB}	-0.3		-0.3	V	(2), (11)
10	Time before V_{RB} is allowed	t_{STABLE}	500				(2), (11)
11	Average Clock Period Accuracy	T_{PERIOD_AVG}	NA		NA	ppm	(10)
12	Absolute Period	T_{PERIOD_ABS}	NA		NA	ns	(6)
13	Cycle-to-cycle jitter	T_{JCC}		3.5	6	ps peak to peak	(2)
14	Absolute Maximum voltage	V_{MAX}			0.8	V	(1), (7)
15	Absolute Minimum voltage	V_{MIN}			-0.3	V	(1), (8)
16	Output Duty-Cycle (when input has 50% duty-cycle)	Duty_cycle	49	50	51	%	(2)
17	Rising to falling edge matching	r/f match			6	%	(1), (7)
18	Clock Source DC impedance (CK)	$Z_{C\text{-}DC\_CK}$	50 - 5%	50	50 + 5%	Ω	DC Measurement
19	Clock Source DC impedance (CK#)	$Z_{C\text{-}DC\_CK\#}$	50 – 5%	50	50 + 5%	Ω	DC Measurement
20	Output frequency	F_{MAX}	0		250	MHz	
21	Output to output skew	t_{OOSK}			50	ps	
22	Device to device output skew	t_{DOOSK}			0.5	ns	
23	Input to output delay	t_{IOD}	0.9		1.5	ns	
24	Output enable time	t_{EN}			10	cycles	
25	Output disable time	t_{DIS}			10	cycles	

* Values are over Recommended Operating Conditions

(0) Output differential swing is calculated as $V_{SW} = V_{OH}-V_{OL}$. It should not be confused with $V_{SW} = 2 * (V_{OH}-V_{OL})$ used in some datasheets

(1) Measurement taken from single ended waveform

(2) Measurement taken from differential waveform.

(3) Measured from -150 mV to +150 mV on the differential waveform (derived from CK minus CK#) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 18

(4) Measured at crossing point where the instantaneous voltage value of the rising edge of CK equals the falling edge of CK# . See Figure 15

(5) Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 15.

(6) This requirement, from PCI Express Base Specification, Revision 4.0 is applicable only to clock generators and not to buffers. A clock buffer is a transparent device whose output clock period follows the input clock period.

(7) Defined as the maximum instantaneous voltage including overshoot. See Figure 15.

(8) Defined as the minimum instantaneous voltage including undershoot. See Figure 15.

(9) Defined as the total variation of all crossing voltages of Rising CK and Falling CK# This is the maximum allowed variance in VCROSS for any particular system. See Figure 16.

(10) The PPM requirement from PCIe Express Base Specification, Revision 4.0 is related to clock generation devices. This requirement is not applicable to buffers because buffer's output frequency accuracy is identical to the frequency accuracy of the source driving the buffer.

(11) TSTABLE is the time the differential clock must maintain a minimum ±150 mV differential voltage after20 rising/falling edges before it is allowed to droop back into the VRB ±100 mV differential range. See Figure 19.

(12) Matching applies to rising edge rate for CKx and falling edge rate for CK#x. It is measured using a ±75 mV window centered on the median cross point where CKx rising meets CK#x falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of CKx should be compared to the Fall Edge Rate of CK#x the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 17.

Table 18 Skew and Jitter Performance

	Parameter	Symbol	Min.	Typ.	Max	Units	Notes
1	Input-to-Output Delay	I/O_{DELAY}	0.9		1.5	ns	1,3
2	Output-to-Output Skew	O/O_{DELAY}			50	ps	1,2
3	Peak-to-Peak Additive Jitter	$p\text{-}pAJ_{RMS}$			0.7	ps	1,2
4	Additive Jitter as per PCIe 1.0 (1.5MHz to 22MHz)	$T_{jPCIe\_1.0}$		0.7	0.8	ps RMS	1, 2
5	Additive Jitter as per PCIe 2.0 high band (1.5MHz to 50MHz)	$T_{jPCIe\_2.0\_high}$		75	94	fs RMS	1, 2
6	Additive Jitter as per PCIe 2.0 low band (10kHz to 1.5MHz)	$T_{jPCIe\_2.0\_low}$		20	28	fs RMS	1, 2
7	Additive Jitter as per PCIe 2.0 mid band (5MHz to 16MHz)	$T_{jPCIe\_2.0\_mid}$		59	74	fs RMS	1, 2
8	Additive Jitter as per PCIe 3.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{jPCIe\_3.0}$		19	24	fs RMS	1, 2
9	Additive Jitter as per PCIe 4.0 (PLL_BW = 2 to 5MHz, CDR = 10MHz)	$T_{jPCIe\_4.0}$		19	24	fs RMS	1, 2
10	Additive Jitter as per PCIe 5.0 (PLL_BW = 0.5 to 1.8MHz, CDR for 32 GT/s CC)	$T_{jPCIe\_5.0}$		7.5	10	fs RMS	1, 2
11	Additive jitter as per Intel QPI 9.6Gbps	T_{jQPI}		35	45	fs RMS	1, 2
12	Additive RMS jitter in 1MHz to 20MHz band	$T_{j\_1M\_20M}$		49	62	fs RMS	1, 2 (100MHz clock)
				40	54	fs RMS	1, 2 (133MHz clock)
13	Additive RMS jitter in 12kHz to 20MHz band	$T_{j\_12k\_20M}$		52	65	fs RMS	1, 2 (100MHz clock)
				42	56	fs RMS	1, 2 (133MHz clock)
14	Noise floor	N_F		-164	-163	dBc/Hz	1, 2 (100MHz clock)
				-163	-162	dBc/Hz	1, 2 (133MHz clock)

1. Measured into AC test load as per Figure 20 .
2. Measured from differential crossing point to differential crossing point.
3. Input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

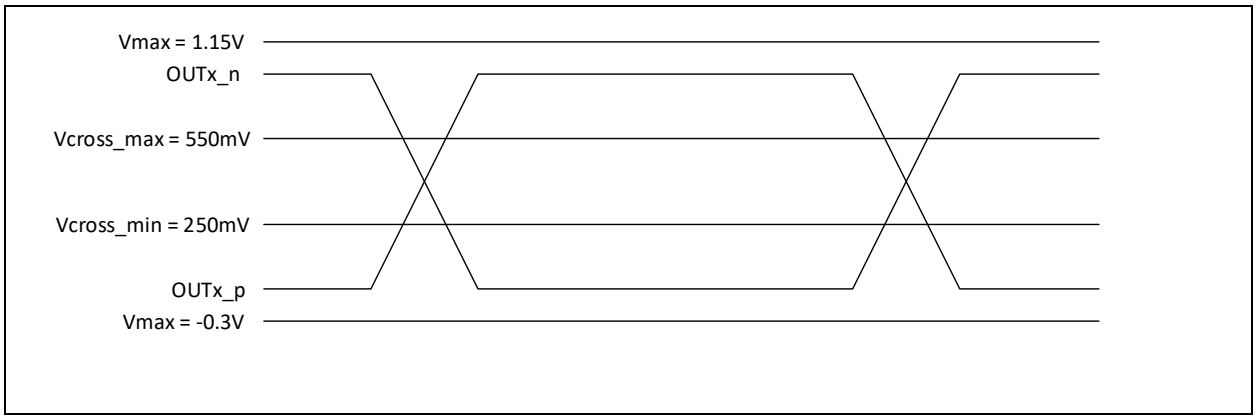


Figure 15. Single-Ended Measurement Points for Absolute Cross Point and Swing

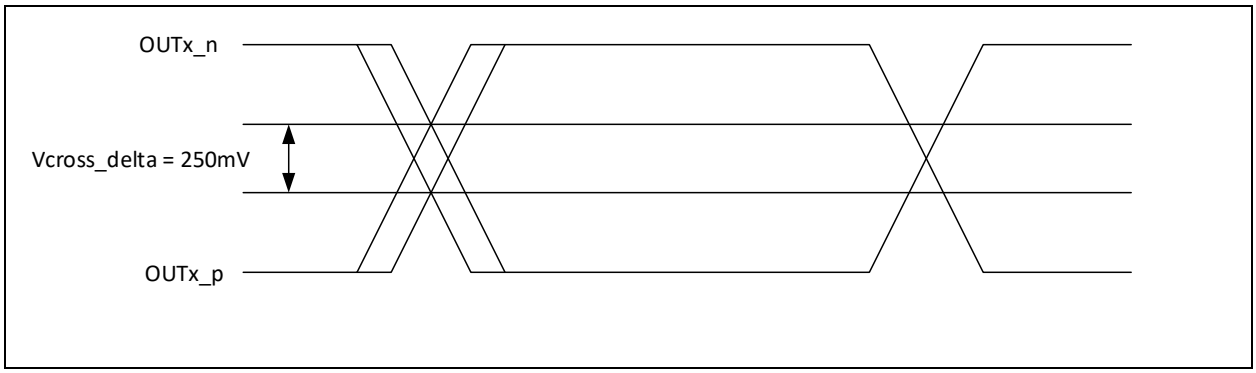


Figure 16. Single-Ended Measurement Points for Delta Cross Point

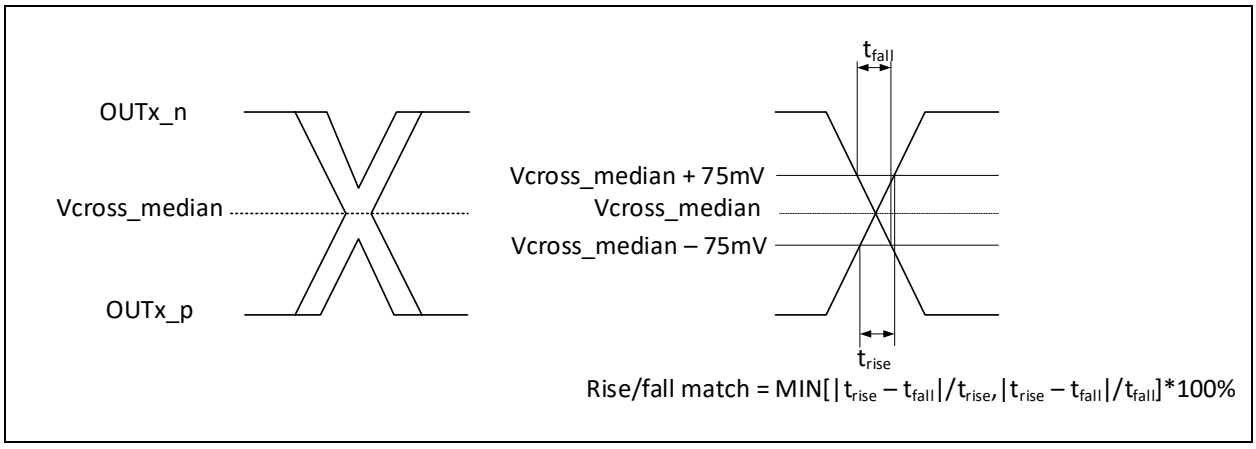


Figure 17. Single-Ended Measurement Points for Rise and Fall Time Matching

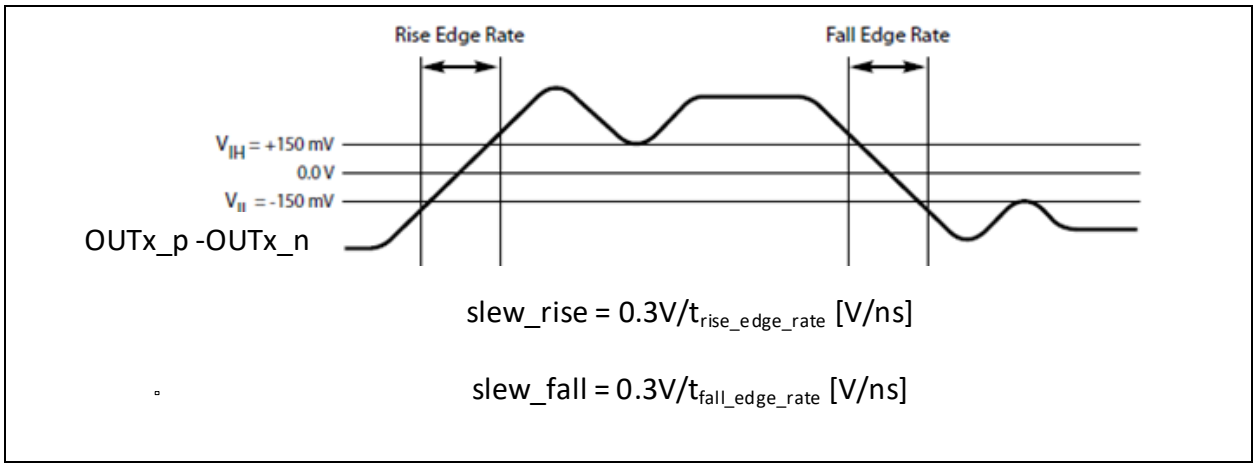


Figure 18. Differential Measurement Points for Rise and Fall Time

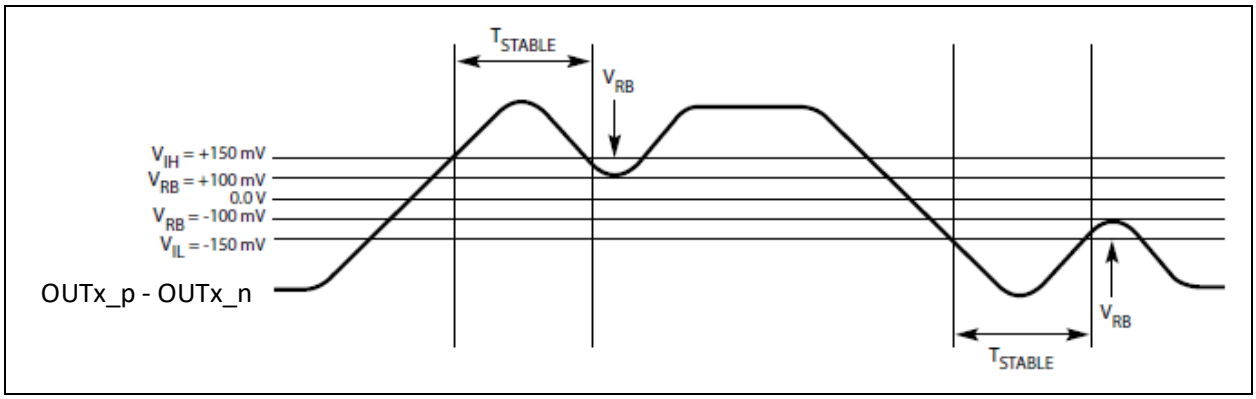


Figure 19. Differential Measurement Points for Ringback

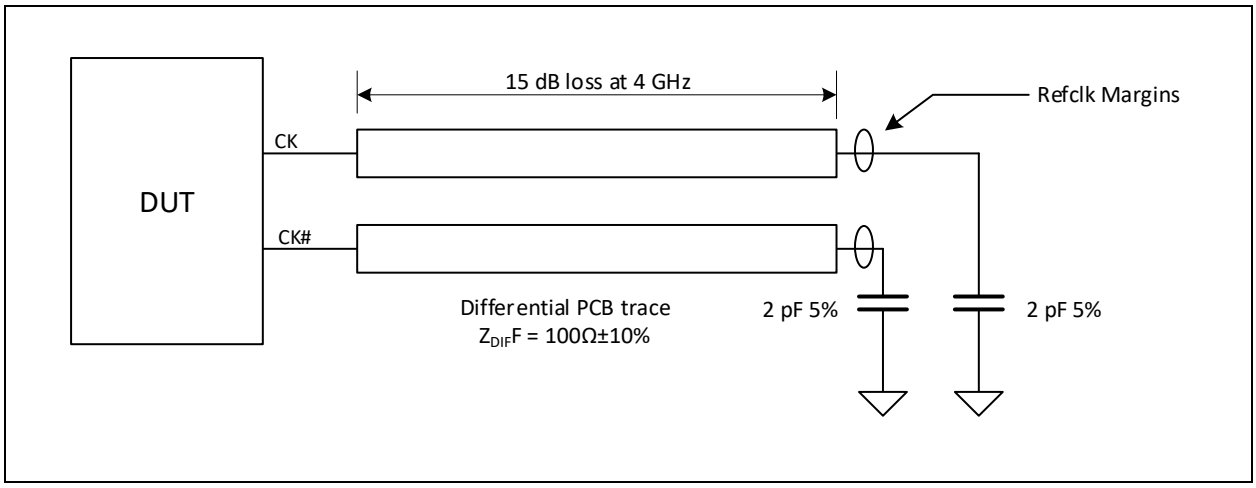


Figure 20. PCIe Test Circuit

Input Clock Requirements

Table 19 Differential Input Clock AC Characteristics

	Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
1	Edge_rate	Input_Slew_Rate	0.7			V/ns	
2	Total Variation of Vcross Over All Edges	Total_Δ_Vcross			140	mV	
3	Input Voltage	Input_Voltage	200			mv diff	

SMBus Electrical Characteristics

Table 20 SMBus Electrical Characteristics

	Parameter	Symbol	Min.	Typ.	Max	Units	Notes
1	Nominal Bus Voltage	VDD_{SMB}	2.7		5.5	V	1
2	Input Low Voltage	V_{IL}			0.8	V	
3	Input High Voltage	V_{IH}	2.1		VDD_{SMB}	V	
4	Output Low Voltage	V_{OL}			0.4	V	At $I_{PULLUP,MAX}$
5	Input Leakage Current	I_{LEAK}			±10	µA	
6	Current sinking at $V_{OL,max}$	I_{PULLUP}	4			mA	
7	Pin capacitive load	C_I			12	pF	
8	Signal noise immunity from 10MHz to 100MHz	V_{NOISE}	300			mV_{P-P}	
9	Noise spike suppression time	T_{SPIKE}	0		50	ns	3
10	SMBus Operating Frequency	F_{SMB}	10		400	kHz	
11	Bus free time between Stop and Start Condition	T_{BUF}	4.7			µs	
12	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	$T_{HD:STA}$	4.0			µs	
13	Repeated Start Condition setup time	$T_{SU:STA}$	4.7			µs	
14	Stop Condition setup time	$T_{SU:STO}$	4.0			µs	
15	Data hold time	$T_{HD:DAT}$	300			ns	
16	Data setup time	$T_{SU:DAT}$	250			ns	
17	Clock low period	T_{LOW}	4.7			µs	
18	Clock high period	T_{HIGH}	4.0		50	µs	
19	Clock/Data Fall Time	T_F			300	ns	2
20	Clock/Data Rise Time	T_R			1000	ns	2

1. 3V to 5V ±10%
2. Rise and fall time is defined as follows:
TR = (VIL,MAX – 0.15) to (VIH,MIN + 0.15)
TF = (VIH,MIN + 0.15) to (VIL,MAX - 0.15)
3. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

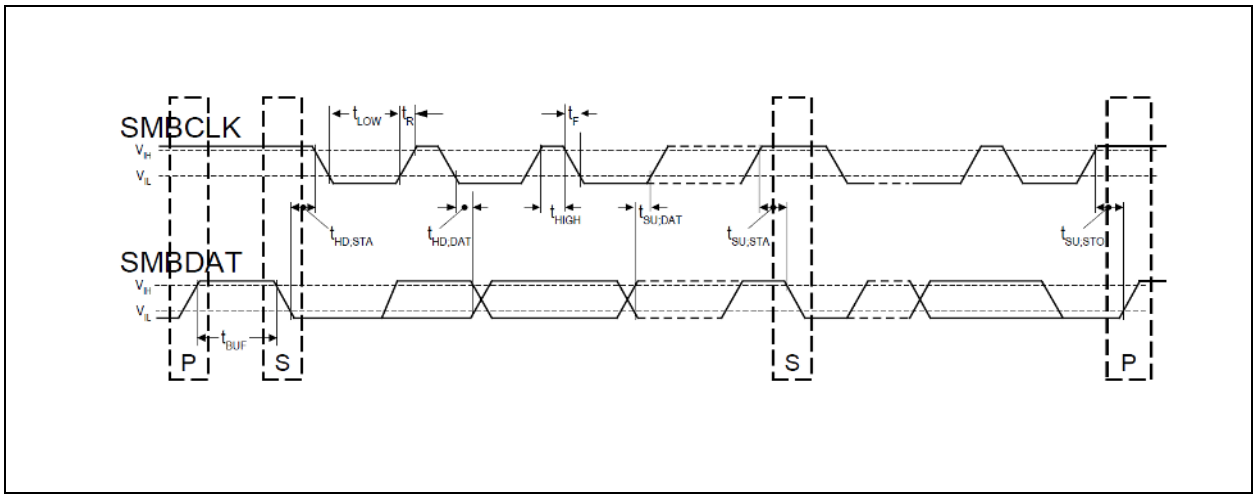


Figure 21. SMBus Timing

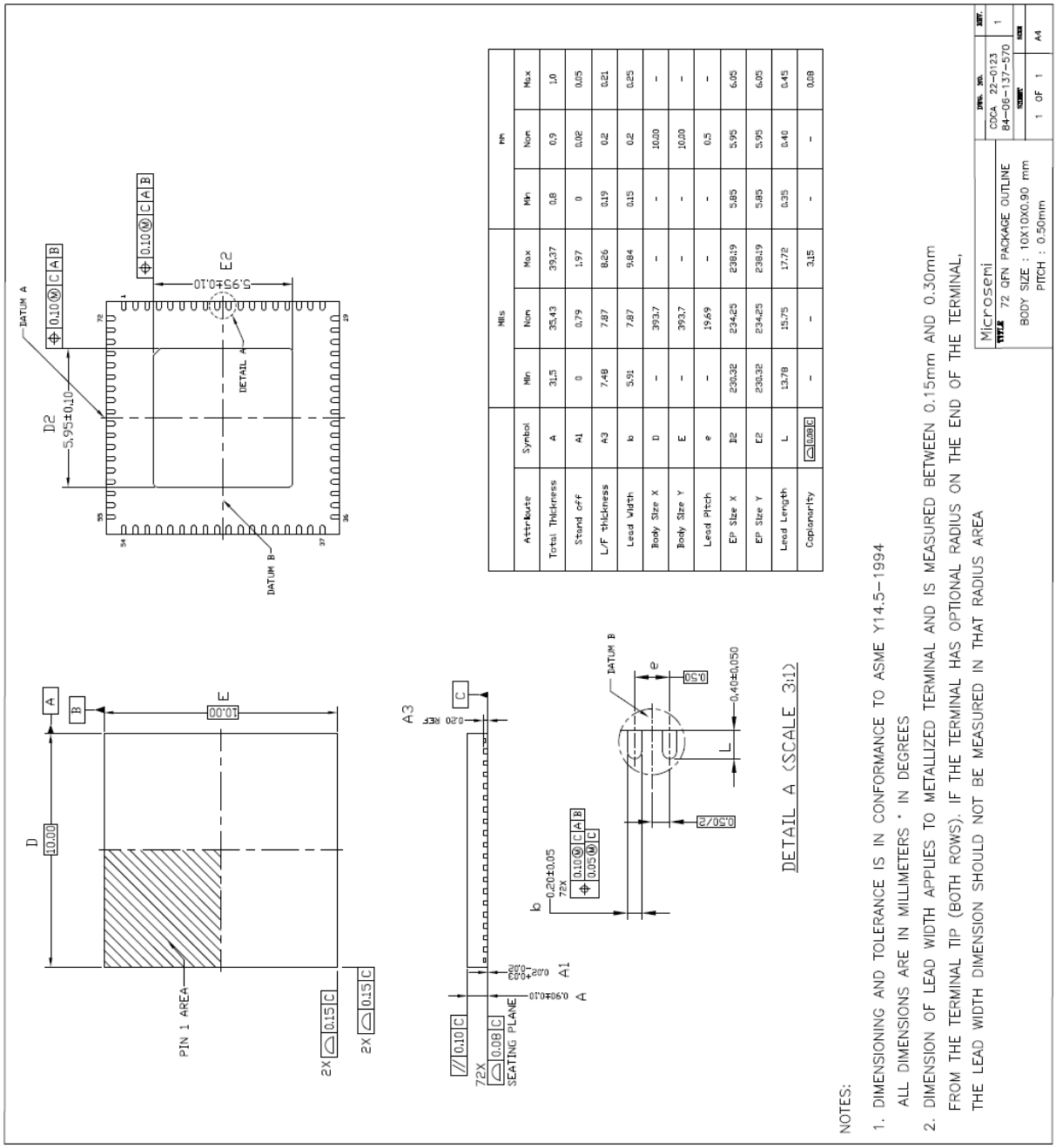
Table 21 10x10mm QFN Package Thermal Properties

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance(1) (Note 1)	θ_{JA}	still air	22.6	°C/W
		1m/s airflow	18.7	
		2.5m/s airflow	16.9	
Junction to Board Thermal Resistance	θ_{JB}		9.7	°C/W
Junction to Case Thermal Resistance	θ_{JC}		12.4	°C/W
Junction to Pad Thermal Resistance(2)	θ_{JP}	Still air	5.1	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	0.4	°C/W

(1) Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on a 4-layer JEDEC standard test board and dissipating maximum power

(2) Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

Package Outline



Attribute	Symbol	Mils Min	Mils Nom	Mils Max	mm Min	mm Nom	mm Max
Total Thickness	A	31.5	35.43	39.37	0.8	0.9	1.0
Stand off	A1	0	0.79	1.97	0	0.02	0.05
L/F thickness	A3	7.48	7.87	8.26	0.19	0.2	0.21
Lead Width	b	5.91	7.87	9.84	0.15	0.2	0.25
Body Size X	D	-	393.7	-	-	10.00	-
Body Size Y	E	-	393.7	-	-	10.00	-
Lead Pitch	e	-	19.69	-	-	0.5	-
EP Size X	D2	230.32	234.25	238.19	5.85	5.95	6.05
EP Size Y	E2	230.32	234.25	238.19	5.85	5.95	6.05
Lead Length	L	13.78	15.75	17.72	0.35	0.40	0.45
Coplanarity	0.08 C	-	-	3.15	-	-	0.08

NOTES:
1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
   ALL DIMENSIONS ARE IN MILLIMETERS ' IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Microsemi
TITLE: 72 QFN PACKAGE OUTLINE
BODY SIZE : 10X10X0.90 mm
PITCH : 0.50mm
DWG. NO. CODA 22-0123
84-06-137-570
REV. 1
SHEET 1 OF 1
SIZE A4

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