Mars ZX2 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mars ZX2 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mars ZX2 SoC module.

Summary

This document first gives an overview of the Mars ZX2 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	MA-ZX2	Mars ZX2 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-410-004	08	16.02.2021

Approval Information	Name	Position	Date
Written by	DIUN	Design Engineer	16.10.2015
Verified by	GLAC	Design Expert	22.10.2015
Approved by	DIUN	Manager, BU SP	16.02.2021

Enclustra GmbH – Räffelstrasse 28 – CH-8045 Zürich – Switzerland
Phone +41 43 343 39 43 – www.enclustra.com

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Document History

Version	Date	Author	Comment
08	16.02.2021	DIUN	Cleaned-up product variants, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, other style updates
07	25.07.2019	DIUN	Added information on voltage monitoring, power supplies, heat sink, Linux how-to guide, other style updates
06	21.08.2018	DIUN	Minor corrections and style updates
05	04.05.2017	DIUN	Updated EEPROM map, block diagram and footprint information
04	27.12.2016	DIUN	Added tool support information and analog inputs section
03	18.08.2016	DIUN	Updated for revision 2
02	10.11.2015	DIUN	Updated module connector information
01	28.10.2015	DIUN	Version 01

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1 Overview

1.1 General

1.1.1 Introduction

The Mars ZX2 SoC module combines the Xilinx Zynq® -7010/7020 All Programmable SoC (System-on-Chip) device with fast DDR3L SDRAM, quad SPI flash, a Gigabit Ethernet PHY, USB 2.0 On-The-Go PHY and a real-time clock, forming a complete and powerful embedded processing system.

The SO-DIMM form factor allows space-saving hardware designs and quick and simple integration of the module into the target application.

The use of the Mars ZX2 SoC module, in contrast to building a custom SoC hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system.

Together with Mars base boards, the Mars ZX2 SoC module allows the user to quickly build a system prototype and start with application development.

The Enclustra Build Environment [15] is available for the Mars ZX2 SoC module. This build system allows the user to quickly set up and run Linux on any Enclustra SoC module. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and FSBL (First Stage Boot Loader). It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

Warning!

Please note that the warranty of an Enclustra module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. Enclustra cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Mars ZX2 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mars ZX2 SoC module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mars ZX2 SoC module.

1.1.5 Safety Recommendations and Warnings

Mars modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mars ZX2 SoC module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; over-voltage on power or signal lines can also cause permanent damage to the module.

Warning!

Use the Mars ZX2 SoC module only with base boards designed for the Enclustra Mars module family. Inserting the Mars ZX2 SoC module into a SO-DIMM connector designed for memory (e.g. a computer main board) may damage the module and the carrier board.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mars ZX2 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Xilinx Zynq®-7010/7020 All Programmable SoC, CLG400 package
  - Dual ARM® Cortex™-A9 MPCore™with CoreSight™ and NEON™ extension
  - Xilinx Artix-7 28 nm FPGA fabric
- 108 user I/Os up to 3.3 V
  - 12 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART) shared with FPGA I/Os
  - 96 FPGA I/Os (single-ended, differential or analog)
- 512 MB DDR3L SDRAM
- 64 MB quad SPI flash
- Gigabit Ethernet
- USB 2.0 On-The-Go (OTG)
- Real-time clock
- SO-DIMM form factor (30 × 67.6 mm, 200 pins)
- The module can be operated using a single 3.3 V supply voltage

1.3 Deliverables

- Mars ZX2 SoC module
- Mars ZX2 SoC module documentation, available via download:
  - Mars ZX2 SoC Module User Manual (this document)
  - Mars ZX2 SoC Module Reference Design [2]
  - Mars ZX2 SoC Module IO Net Length Excel Sheet [3]
  - Mars ZX2 SoC Module FPGA Pinout Excel Sheet [4]
  - Mars ZX2 SoC Module User Schematics (PDF) [5]
  - Mars ZX2 SoC Module Known Issues and Changes [6]
  - Mars ZX2 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [7]
  - Mars ZX2 SoC Module 3D Model (PDF) [8]
  - Mars ZX2 SoC Module STEP 3D Model [9]
  - Mercury Mars Module Pin Connection Guidelines [10]
  - Mars Master Pinout [11]
  - Mars Heatsink Mounting Guide [18]

- Enclustra Build Environment [15] (Linux build environment; refer to Section 1.4.2 for details)
- Enclustra Build Environment How-To Guide [16]

1.4 Accessories

1.4.1 Reference Design

The Mars ZX2 SoC module reference design features an example configuration for the Zynq-7000 SoC device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from Github: `https://github.com/enclustra`.

1.4.2 Enclustra Build Environment

The Enclustra Build Environment (EBE) [15] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and FSBL. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [16] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

1.4.3 Enclustra Heat Sink

For Mars modules an Enclustra heat sink is available for purchase along with the product. Please refer to section 2.10.6 for further information on the available cooling options.

1.4.4 Mars ST3 Base Board

- Mars 200-pin SO-DIMM socket
- MIPI D-PHY connector (requires FPGA support)
- Mini DisplayPort connector (requires FPGA support)
- HDMI connector (requires FPGA support)
- USB 3.0 host connector
- RJ45 Ethernet connector
- 2 × 40-pin GPIO connector (Anios)
- 1 × 8-pin and 1 × 4-pin GPIO connectors (Pmod™ compatible pinout)
- FTDI USB 2.0 device controller with micro USB device connector
- microSD card holder
- User LEDs
- Integrated Xilinx compatible JTAG adapter
- Support for low I/O voltages (1.2 V, 1.8 V)
- Single 12 V DC supply voltage
- Form factor: 100 × 80 mm

Please note that the available features depend on the equipped Mars module type.

1.4.5 Mars EB1 Base Board

- Mars 200-pin SO-DIMM socket
- 2 × Mini Camera Link connectors (requires FPGA support)
- HDMI 1.3 connector (requires FPGA support)
- 40-pin GPIO connector (Anios)
- 3 × 12-pin GPIO connector (two of the connectors with Pmod™ compatible pinout)
- RJ45 Ethernet connector
- USB 2.0 A host connector
- Micro USB 2.0 device connector (shared)
- FTDI USB 2.0 device controller with micro USB device connector
- microSD card holder
- Various switches and LEDs
- Integrated Xilinx compatible JTAG adapter
- Single 12 V DC supply voltage or USB bus-powered (with restrictions)
- Form factor: 120 × 80 mm

Please note that the available features depend on the equipped Mars module type.

1.4.6 Mars PM3 Base Board

- Mars 200-pin SO-DIMM socket
- FMC LPC (Low Pin Count) connector (72 I/Os)
- 40-pin GPIO connector (optional, shared with FMC I/Os)
- RJ45 Gigabit Ethernet connector
- Mini HDMI connector for PCIe and LVDS applications (module dependent)
- Cypress FX3 USB 3.0 device controller (16-bit Slave-FIFO interface or 32-bit Slave-FIFO interface shared with FMC I/Os)
- USB 3.0 B device connector
- USB 2.0 A host connector
- Micro USB 2.0 B device connector with FTDI USB device controller
- Battery holder for the real-time clock
- microSD card holder
- Fan connector, various switches and LEDs
- Single 12 V DC supply voltage or USB bus-powered (with restrictions)
- Form factor: 100 × 72 mm (pico-ITX)

Please note that the available features depend on the equipped Mars module type.

1.5 Xilinx Tool Support

The SoC devices equipped on the Mars ZX2 SoC module are supported by the Vivado HL WebPACK Edition software, which is available free of charge. Please contact Xilinx for further information.

2 Module Description

2.1 Block Diagram

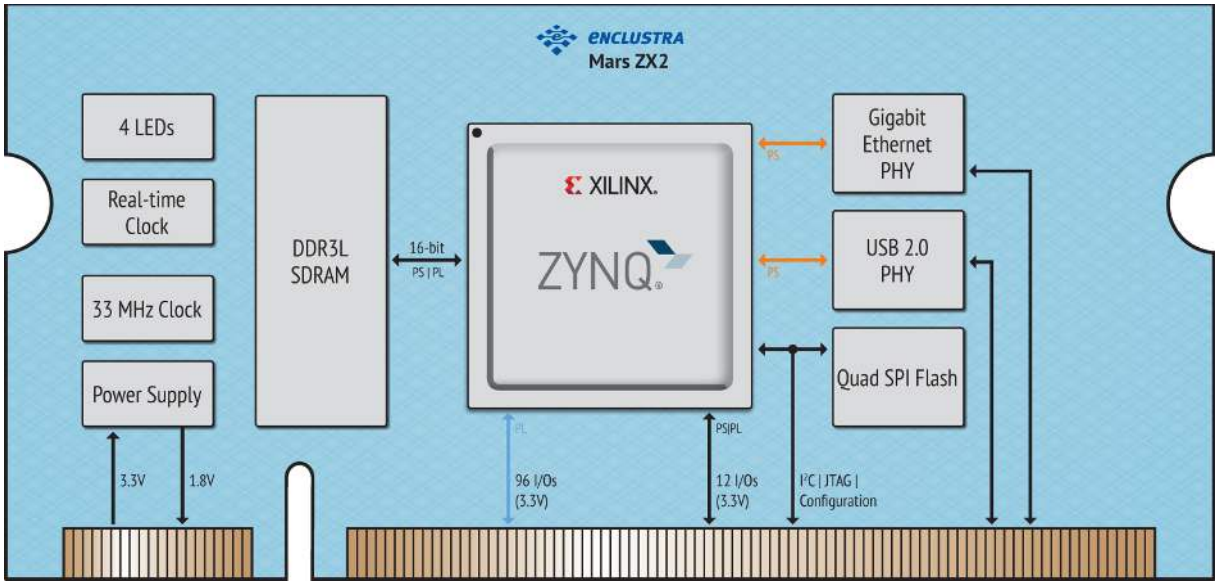

Figure 1: Hardware Block Diagram

The main component of the Mars ZX2 SoC module is the Xilinx Zynq-7000 SoC device. Most of its I/O pins are connected to the Mars module connector, making 108 user I/Os available to the user.

The SoC device can boot from the on-board QSPI flash or from an SD card. For development purposes, a JTAG interface is connected to Mars module connector.

The available standard configurations include a 64 MB quad SPI flash and 512 MB DDR3L SDRAM.

Further, the module is equipped with a Gigabit Ethernet PHY and a USB 2.0 OTG PHY, making it ideal for communication applications.

A real-time clock is available on the module and is connected to the global I2C bus.

On-board clock generation is based on a 33.33 MHz crystal oscillator.

The module can be operated using a single input supply of 3.3 V DC. All other necessary supply voltages are generated on-board. Some of these voltages are available on the Mars module connector to supply circuits on the base board.

Four LEDs are connected to the SoC pins for status signaling.

2.2 Module Configuration and Product Codes

Table 1 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Code	SoC	DDR3L SDRAM	Temperature Range
MA-ZX2-10-2I-D9	XC7Z010-2CLG400I	512 MB	-40 to +85° C
MA-ZX2-20-2I-D9	XC7Z020-2CLG400I	512 MB	-40 to +85° C

Table 1: Standard Module Configurations

The product code indicates the module type and main features. Figure 2 describes the fields within the product code.

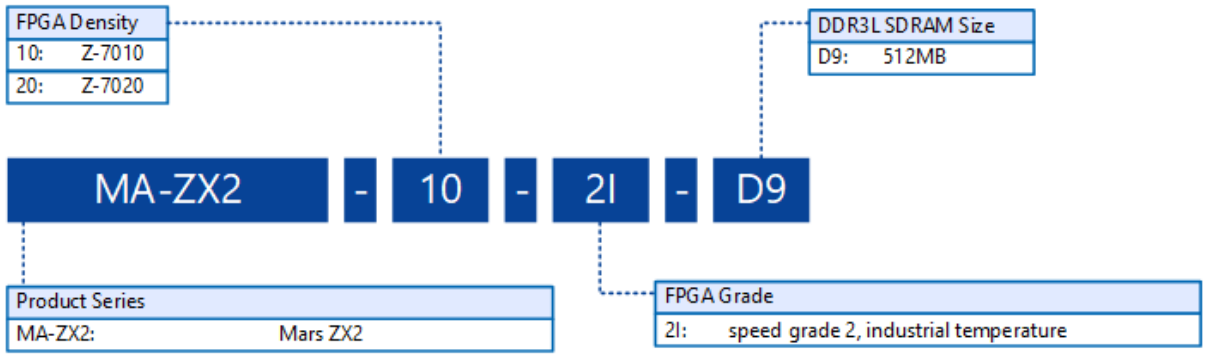

Figure 2: Product Code Fields

Please note that for the first revision modules or early access modules, the product code may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 Article Numbers and Article Codes

Every module is uniquely labeled, showing the article number and serial number. An example is presented in Figure 3.

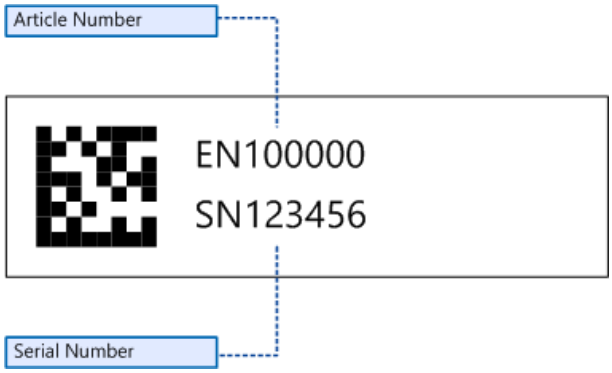

Figure 3: Module Label

The correspondence between article number and article code is shown in Table 2. The article code represents the product code, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mars ZX2 SoC Module Known Issues and Changes document [6].

Article Number	Article Code
EN101030	MA-ZX2-10-1C-D9-R1
EN101031	MA-ZX2-10-2I-D9-R1
EN101032	MA-ZX2-20-1C-D9-R1
EN101033	MA-ZX2-20-2I-D9-R1
EN101497	MA-ZX2-10-1C-D9-R2
EN101498	MA-ZX2-10-2I-D9-R2
EN101499	MA-ZX2-20-1C-D9-R2
EN101500	MA-ZX2-20-2I-D9-R2

Table 2: Article Numbers and Article Codes

2.4 Top and Bottom Views

2.4.1 Top View

Figure 4: Module Top View

2.4.2 Bottom View

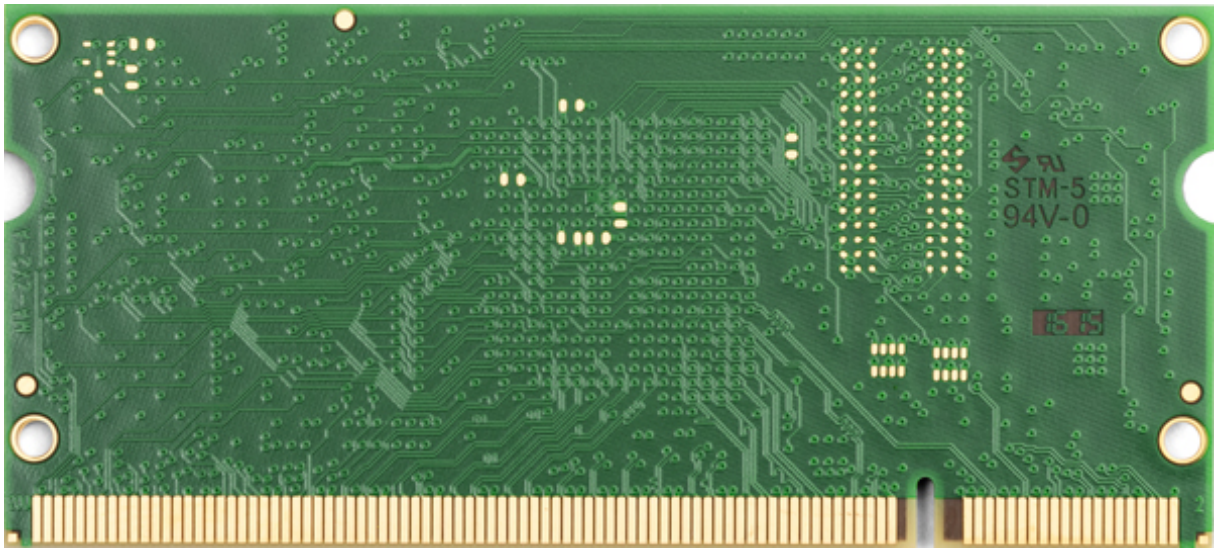

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

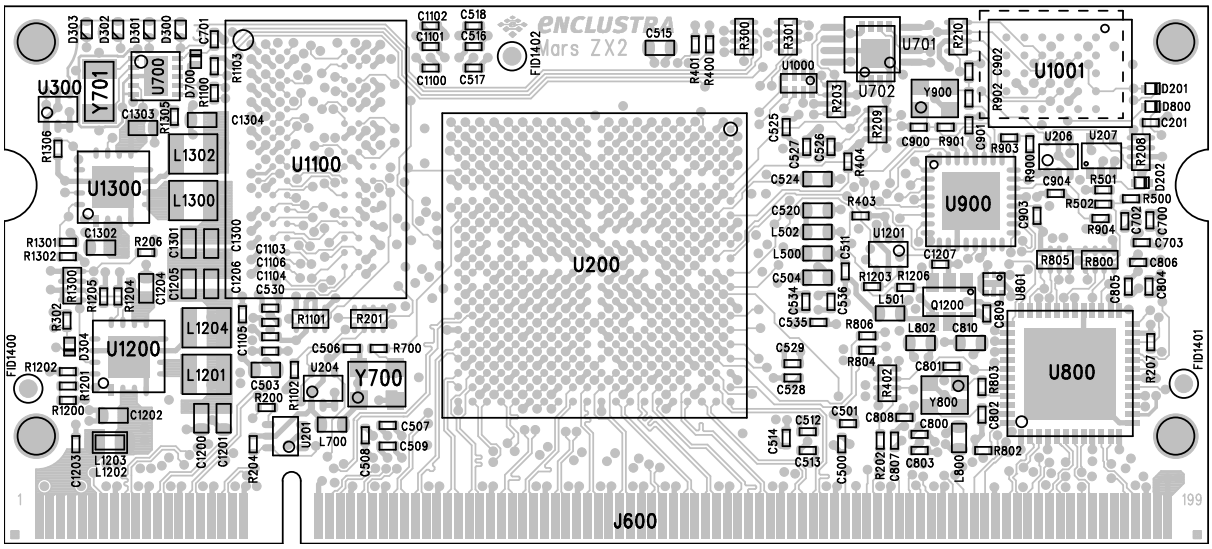

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

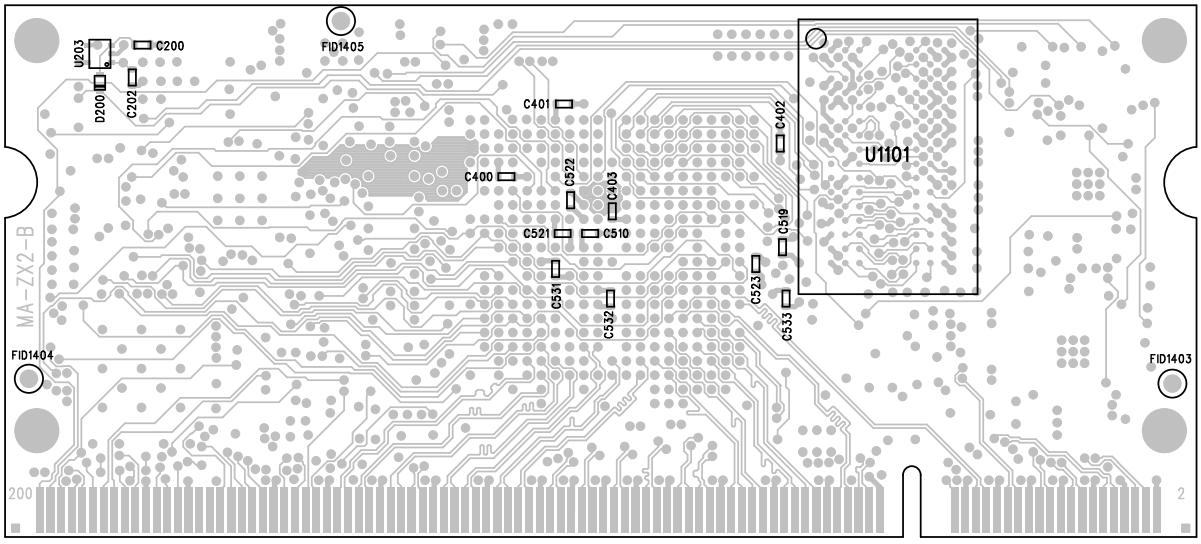

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint

Figure 8 shows the dimensions of the module footprint on the base board.

In the standard configuration of the Mars ZX2 SoC module, there are no components placed on the bottom side. In custom configurations, depending on the size of the DDR3L SDRAM, additional components may be assembled on the bottom side of the module.

The maximum component height under the module is dependent on the connector type - refer to Section 2.8 for detailed connector information.

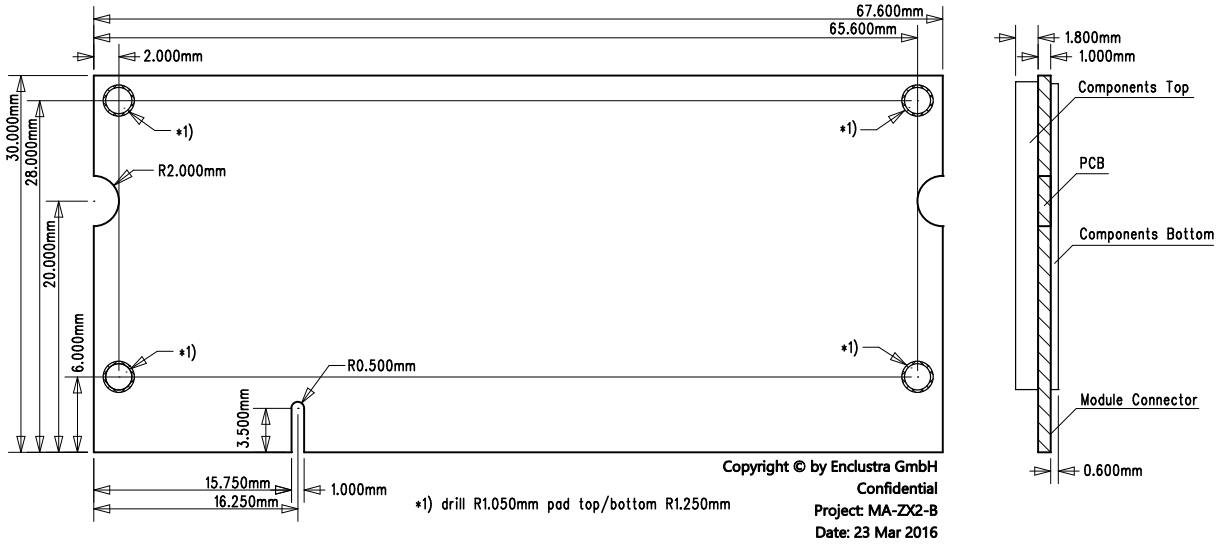

Figure 8: Module Footprint - Top View

The footprint of the module connector is available for different PCB design tools (Altium, Eagle, Orcad, PADS) [7].

2.7 Mechanical Data

Table 3 describes the mechanical characteristics of the Mars ZX2 SoC module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Symbol	Value
Size	67.6 × 30 mm
Component height top	1.8 mm
Component height bottom	0.6 mm (when components are equipped on the bottom side)
Weight	7 g

Table 3: Mechanical Data

2.8 Module Connector

The Mars ZX2 SoC module fits into a 200-pin DDR2 SO-DIMM (1.8 V) socket. Up to four M2 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mars Master Pinout Excel Sheet [11]. The connector to be mounted on the base board is available in different heights. Some examples are presented in Table 4. Please refer to the connector datasheet for more information.

Height	Type	Description	Max component height under the module
4.0 mm	TE 292406-4	DDR2-SODIMM, 1.8 V	0 mm
5.2 mm	TE 1565917-4	DDR2-SODIMM, 1.8 V	1 mm
6.5 mm	TE 5-1746530-4	DDR2-SODIMM, 1.8 V	2 mm
8.0 mm	TE 1827341-4	DDR2-SODIMM, 1.8 V	4 mm

Table 4: Module Connector Types

2.9 User I/O

2.9.1 Pinout

Information on the Mars ZX2 SoC module pinout can be found in the Enclustra Mars Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

Warning!

Please note that the pin types on the schematics symbol of the module connector and in the Master Pinout document are for reference only. On the Mars ZX2 SoC module it may be possible that the connected pins do not have the targeted functions (such as primary clocks, differential pins, MGT signals, etc).

The naming convention for the user I/Os is:
IO_B<BANK>_L<PAIR><_SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, IO_B35_L12_MRCC_K18_N is located on pin K18 of I/O bank 35, pair 12, it is an MRCC (Multi-Region Clock Capable) pin and it has negative polarity, when used in a differential pair.

For the signal lines shared between Programmable Logic (PL) and Processing System (PS), the naming convention is:
IO_<MIO_PIN>_B<BANK>_L<PAIR>_<PACKAGE_PIN>

For example, IO_MIO42_B13_L18_W11 is connected to FPGA pin W11 and in parallel to the PS MIO pin 42.

Please note that for the shared pins only one of the driving pins (FPGA pin, MIO pin) may be active.

The multi-region clock capable pins are marked with "MRCC", while the single region clock capable pins are marked with "SRCC" in the signal name. For details on their function and usage, please refer to the Xilinx documentation.

Table 5 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Signals	Pairs	Differential	Single-ended	I/O Bank
IO_<MIO_PIN>_<...>	12	6	In/Out	In/Out	13 (not available on XC7Z010 device)
IO_B34_<...>	48	24	In/Out	In/Out	34
IO_B35_<...>	48	24	In/Out	In/Out	35
Total	**108**	**54**	-	-	-

Table 5: User I/Os

Please note that for the 7 Series FPGAs there are restrictions on the VCCO voltage when using LVDS I/Os; refer to Xilinx AR# 43989 for details.

2.9.2 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the SoC device to the module connector is available in Mars ZX2 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Warning!

Please note that the trace length of various signals may change between revisions of the Mars ZX2 SoC module. Please use the information provided in the Mars ZX2 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will still be routed differentially in subsequent product revisions.

2.9.3 I/O Banks

Table 6 describes the main attributes of the FPGA and PS I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

Bank	Connectivity	VCC_IO	VREF
Bank 0	Configuration	User selectable VCC_CFG_MIO_B13	-
Bank 13 (not available on XC7Z010 device)	Module connector Most pins shared with MIO 40-51	User selectable VCC_CFG_MIO_B13	-

Continued on next page...

Bank	Connectivity	VCC_IO	VREF
Bank 34	Module connector	User selectable VCC_IO_B34	IO_B34_L6_VREF_R14_N IO_B34_L19_VREF_R17_N
Bank 35	Module connector	User selectable VCC_IO_B35	IO_B35_L6_VREF_F17_N IO_B35_L19_VREF_G15_N
PS MIO0	QSPI flash, LEDs, module connector	User selectable VCC_CFG_MIO_B13	-
PS MIO1	Ethernet PHY, USB PHY, module connector	User selectable VCC_CFG_MIO_B13	0.9 V
PS DDR	DDR3L SDRAM	1.35 V	0.68 V

Table 6: I/O Banks

Warning!

Some of the I/Os are connected to MIO pins and to user logic I/Os in parallel - make sure that at least one of the two pins is configured to high impedance, and that pull-up or pull-down resistors are disabled on both if they are not used.

Some of the system pins must be defined as input or high impedance. Please refer to the Mars ZX2 SoC module reference design for details [2].

2.9.4 VREF Usage

I/O standards referenced using VREF can be used on the Mars module connector. The reference voltage has to be applied to all VREF pins of the respective I/O banks. If a bank is configured to use an I/O standard that does not need a reference voltage, the VREF pins of this bank on the module connector are available as user I/O pins.

The VREF pins are listed in the Mars Master Pinout Excel Sheet [11].

Warning!

Use only VREF voltages compliant with the equipped SoC device; any other voltages may damage the equipped SoC device, as well as other devices on the Mars ZX2 SoC module.

Do not leave a VREF pin floating when the used I/O standard requires a reference voltage, as this may damage the equipped SoC device, as well as other devices on the Mars ZX2 SoC module.

2.9.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x], respectively VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mars base boards and modules, it is recommended to use a single I/O voltage.

Signal Name	SoC Pins	Supported Voltages	Connector Pins
VCC_CFG_MIO_B13	VCCO_13, VCC_MIO0, VCC_MIO1	1.8 V, 2.5 V - 3.3 V[1] ±5%	137, 146
VCC_IO_B34	VCCO_34	1.8 V - 3.3 V[2] ±5%	53, 62, 73
VCC_IO_B35	VCCO_35	1.8 V - 3.3 V[2] ±5%	82, 117, 126

Table 7: VCC_IO Pins

Note that the CFGBVS_0 pin is set automatically to GND (if VCC_CFG_MIO_B13 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_MIO_B13 is 2.5 V or 3.3 V).

Warning!

Use only VCC_IO voltages compliant with the equipped SoC device; any other voltages may damage the equipped SoC device, as well as other devices on the Mars ZX2 SoC module.

Do not leave a VCC_IO pin floating, as this may damage the equipped SoC device, as well as other devices on the Mars ZX2 SoC module.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 9 illustrates the VCC_IO power requirements.

[1] The RGMII Ethernet interface is only specified up to 2.5 V on the MIO pins by Xilinx. Please refer to Section 2.17 for details.
[2] I/O banks 34 and 35 can run down to 1.2 V, but the FPGA LEDs will be always on in this case.

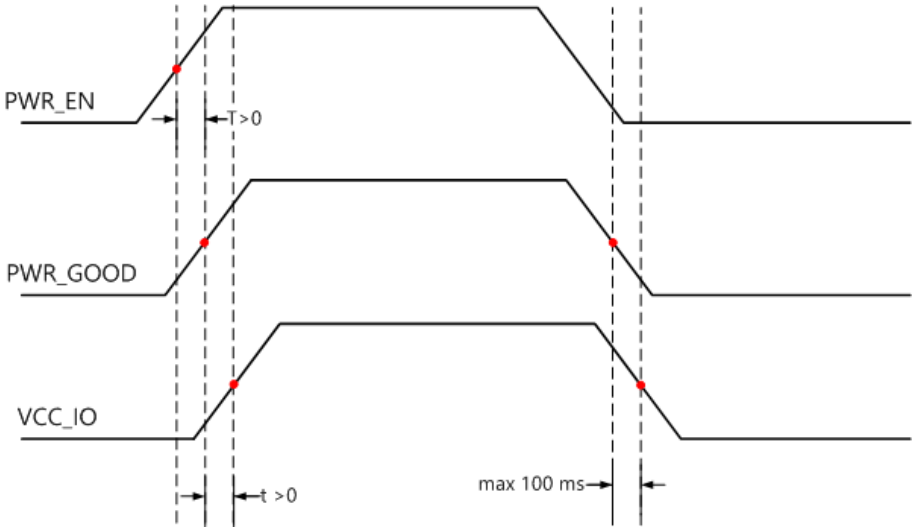

Figure 9: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

2.9.6 Signal Terminations

Differential Inputs

There are no external differential termination resistors on the Mars ZX2 SoC module for differential inputs. Differential input pairs on the module connector may be terminated either by external termination resistors on the base board (close to the module pins), or by the SoC device's internal termination resistors.

Internal differential termination is available only for certain VCCO voltages; please refer to Xilinx AR# 43989 for details.

Single-Ended Outputs

There are no series termination resistors on the Mars ZX2 SoC module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

2.9.7 Multiplexed I/O (MIO) Pins

Details on the MIO/EMIO terminology are available in the Zynq-7000 All Programmable SoC Technical Reference Manual [19].

Some of the MIO pins on the Mars ZX2 SoC module are connected to on-board peripherals, while others are available as GPIOs; the suggested functions below are for reference only - always verify your MIO pinout with the Xilinx device handbook.

Table 8 gives an overview over the MIO pin connections on the Mars ZX2 SoC module. Only the pins marked with "user functionality" are available on the module connector.

MIO group	Function	Connection
0	PWR_EN#_PL	Power enable signal for PL; refer to Section 2.10.1 for details.
1-6, 8	QSPI flash	QSPI flash
7	I2C interrupt	On-board I2C interrupt line
10-13	LEDs	On-board LEDs (shared with PL LED signals)
14-15	I2C	On-board I2C bus and module connector via level shifter
16-27	Ethernet	Gigabit Ethernet PHY
28-39	USB	USB 2.0 OTG PHY
40-45	SD card/user functionality	Module connector
46 47	UART RX[3]/user functionality UART TX[3]/user functionality	Module connector
48-51	User functionality	Module connector
52-53	Ethernet MDIO	Gigabit Ethernet PHY

Table 8: MIO Pins Connections Overview

2.9.8 Analog Inputs

The Zynq-7000 SoC devices provide a dual 12-bit ADC. The auxiliary analog inputs of the SoC device are connected to the module connector; these I/Os have the abbreviation "AD" followed by the ADC channel in the signal name.

The two dedicated ADC pins VP and VN are not available on the module connector.

The ADC can also be used for internal voltage and temperature monitoring. For detailed information, refer to the Xilinx 7 Series XADC User Guide [20].

The ADC lines are always used differentially; for single-ended applications, the *_N line must be connected to GND.

Table 9 presents the ADC Parameters.

[3]UART RX is an SoC input; UART TX is an SoC output.

Parameter	Value
VCC_ADC	1.8 V
GND_ADC	0 V (connected to GND via ferrite)
VREF_ADC	Internal
ADC Range	0-1 V
Sampling Rate per ADC	1 MSPS
Total number of channels available on the module connector	16 (only auxiliary inputs)

Table 9: ADC Parameters

2.10 Power

2.10.1 Power Generation Overview

The Mars ZX2 SoC module uses a 3.3 - 5.0 V DC power input for generating the on-board supply voltages (1.0 V, 1.35 V, 1.8 V). These internally-generated voltages are accessible on the module connector. In addition, a separate 3.3 V power input is used to supply peripherals, such as the Ethernet PHY, QSPI flash, oscillator, RTC, EEPROM and LEDs.

The Mars ZX2 SoC module can be powered using a single power supply. In this case, the two voltage supply inputs VCC_MOD and VCC_3V3 must be connected together to a 3.3 V supply. Please refer to Section 2.10.3 for details on the voltage supply inputs.

Table 10 describes the power supplies generated on the module. Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN	Influences PWR_GOOD
VCC_1V0_PS	1.0 V (PS core supply)	1 A	VCC_MOD	Yes	Yes
VCC_1V0_PL	1.0 V (PL core supply)	1.5 A	VCC_MOD	Yes	No
VCC_1V35	1.35 V	1 A	VCC_MOD	Yes	Yes
VCC_1V8_PS	1.8 V	1.5 A	VCC_MOD	Yes	Yes

Table 10: Generated Power Supplies

The voltage supplies for the PL side (VCC_1V0_PL, VCC_1V8_PL, VCC_1V8_ADC) can be shut down by pulling high MIO0 pin (PWR_EN#_PL) from the PS. The PS side of the SoC chip will still be functional if the PL side is turned off, as long as the power sequencing requirements for the SoC device are respected. For details please refer to the Zynq-7000 DC and AC Switching Characteristics Datasheet [24].

Warning!

Special care must be taken when using the PWR_EN#_PL signal to shut down the PL side of the SoC device. Only certain VCC_CFG and VCC_IO configurations can allow this low-power mode, without violating the power sequencing requirements. Violating the Xilinx recommended power-up sequence could cause permanent damage of the Mars ZX2 SoC module.

2.10.2 Power Enable/Power Good

The Mars ZX2 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters for 1.0 V, 1.35 V and 1.8 V, leaving the SoC device and the DDR3L SDRAM unpowered.

The PWR_EN input is pulled to VCC_3V3 on the Mars ZX2 SoC module with a 10 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mars ZX2 SoC module with a 10 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if the on-board regulators fail or if the module is disabled via PWR_EN. The list of regulators that influence the state of PWR_GOOD signal is provided in Section 2.10.1.

Pin Name	Module Connector Pin	Remarks
PWR_EN	13	Floating/3.3 V: module power enabled Driven low: module power disabled
PWR_GOOD	40	0 V: module supply not ok 3.3 V: module supply ok

Table 11: Module Power Status and Control Pins

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mars ZX2 SoC module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins when PWR_EN is driven low to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 9.

2.10.3 Voltage Supply Inputs

Table 12 describes the power supply inputs on the Mars ZX2 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.5.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	1, 3, 5, 7, 9, 11	3.3 - 5.0 V ±10%	Supply for the 1.0 V, 1.35 V and 1.8 V voltage regulators. The input current is rated at 1.8 A (0.3 A per connector pin).
VCC_3V3	197, 199	3.3 V ±5%	Supply for Ethernet PHY, QSPI flash, oscillator, RTC, EEPROM and LEDs
VCC_BAT	200	2.0 - 3.6 V	Battery for the RTC and SoC encryption key storage

Table 12: Voltage Supply Inputs

2.10.4 Voltage Supply Outputs

Table 13 presents the supply voltages generated on the Mars ZX2 SoC module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[4]
VCC_1V0	42	1.0 V ±5%	0.3 A
VCC_1V35	41	1.35 V ±5%	0.3 A
VCC_1V8	89, 94, 101, 106	1.8 V ±5%	0.7 A (and max 0.3 A per connector pin)

Table 13: Voltage Supply Outputs

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mars ZX2 SoC module.

2.10.5 Power Consumption

Please note that the power consumption of any SoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Xilinx Power Estimator available on the Xilinx website.

2.10.6 Heat Dissipation

High performance devices like the Xilinx Zynq-7000 SoC need cooling in most applications; always make sure the SoC is adequately cooled.

For Mars modules an Enclustra heat sink is available for purchase along with the product. It represents an optimal solution to cool the Mars ZX2 SoC module - it is low profile (less than 7 mm tall) and covers the whole module surface. It comes with a gap pad for the SoC device and four screws to attach it to the module

[4] The maximum available output current depends on your SoC design. See sections 2.10.1 and 2.10.5 for details.

PCB. With additional user configured gap pads, it is possible to cool other components on board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. Please note that the Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, mounting material).

Table 14 lists the heat sink and thermal pad part numbers that are compatible with the Mars ZX2 SoC module. Details on the Mars heat sink kit can be found in the Mars Heatsink Mounting Guide [18].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mars ZX2	CSG324 [25]	HS-MA1	ATS-52150G-C1-R0	TG-A6200-16-16-1

Table 14: Heat Sink Type

Please note that the adhesive heat sink part is recommended only for prototyping purposes. In cases where the module in used in environments subject to vibrations, a heat sink with mounting screws or clips may be required for optimal fixation.

Warning!

Depending on the user application, the Mars ZX2 SoC module may consume more power than can be dissipated without additional cooling measures; always make sure the SoC is adequately cooled by installing a heat sink and/or providing air flow.

2.10.7 Voltage Monitoring

Several pins on the module connector on the Mars ZX2 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Table 15 presents the VMON pins on the Mars ZX2 SoC module.

Pin Name	Module Connector Pin	Connection	Description
VMON_1V2	198	VCC_1V2	1.2 V on-board voltage (default)/SoC battery voltage (assembly option)

Table 15: Voltage Monitoring Outputs

Warning!

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

2.11 Clock Generation

A 33.33 MHz oscillator is used for the Mars ZX2 SoC module clock generation. The 33.33 MHz clock is fed to the PS and the FPGA logic. Table 16 describes the clock connections.

Signal Name	Frequency	Package Pin	SoC Pin Type
CLK33	33.33 MHz	E7	PS_CLK
CLK33	33.33 MHz	Y7	IO_L13P_MRCC_13

Table 16: Module Clock Resources

2.12 Reset

The power-on reset signal (POR) and the PS system reset signal (SRST) of the SoC device are available on the module connector.

Pulling PS_POR# low resets the SoC device, the Ethernet and the USB PHYs, and the QSPI flash. Please refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins.

Pulling PS_SRST# low resets the SoC device. For details on the functions of the PS_POR_B and PS_SRST_B signals refer to the Zynq-7000 Technical Reference Manual [19].

Table 17 presents the available reset signals. Both signals, PS_POR# and PS_SRST#, have on-board 10 kΩ pull-up resistors to VCC_CFG_MIO_B13.

Signal Name	Connector Pin	Package Pin	FPGA Pin Type	Description
PS_POR#	196	C7	PS_POR_B	Power-on reset
PS_SRST#	192	B10	PS_SRST_B	System reset

Table 17: Reset Resources

Please note that PS_POR# is automatically asserted if PWR_GOOD is low.

2.13 LEDs

The four LEDs on the Mars ZX2 SoC module are connected to both PL and PS, and they are active-low.

As the LEDs can be driven from both PL and PS, it is recommended to drive the FPGA pins to a high impedance state before driving the PS pins and vice versa.

Signal Name	FPGA Pin	MIO Pin	Remarks
LED0#	R19	MIO10	User function/active-low
LED1#	T19	MIO11	User function/active-low
LED2#	G14	MIO12	User function/active-low
LED3#	J15	MIO13	User function/active-low

Table 18: LEDs

2.14 DDR3L SDRAM

There is a single DDR3 SDRAM channel on the Mars ZX2 SoC module attached directly to the PS side and is available only as a shared resource to the PL side.

The DDR3 SDRAM is operated at 1.35 V (low power mode). In the standard configuration the DDR bus width is 16-bit.

The maximum memory bandwidth on the Mars ZX2 SoC module is:
1066 Mbit/sec × 16 bit = 2132 MB/sec

2.14.1 DDR3L SDRAM Type

Table 19 describes the memory availability and configuration on the Mars ZX2 SoC module.

Module	SDRAM Type	Density	Configuration	Manufacturer
MA-ZX2-D9 (commercial)	NT5CC256M16CP-DI	4 Gbit	256 M × 16 bit	Nanya
MA-ZX2-D9 (industrial)	NT5CC256M16CP-DII	4 Gbit	256 M × 16 bit	Nanya
MA-ZX2-D9 (industrial)	NT5CC256M16ER-EKI	4 Gbit	256 M × 16 bit	Nanya
MA-ZX2-D9 (industrial)	K4B4G1646D-BMK0	4 Gbit	256 M × 16 bit	Samsung
MA-ZX2-D9 (industrial)	K4B4G1646E-BMMA	4 Gbit	256 M × 16 bit	Samsung
MA-ZX2-D9 (industrial)	H5TC4G63CFR-RDI	4 Gbit	256 M × 16 bit	SK Hynix

Table 19: DDR3L SDRAM Types

Warning!

Other DDR3L memory devices may be equipped in future revisions of the Mars ZX2 SoC module. Please check the user manual regularly for updates. Any parts with different speed bins or temperature ranges that fulfill the requirements for the module variant may be used.

2.14.2 Signal Description

Please refer to the Mars ZX2 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR3 SDRAM connections.

2.14.3 Termination

Warning!

No external termination is implemented on the Mars ZX2 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR3 SDRAM device.

2.14.4 Parameters

Please refer to the Mars ZX2 SoC module reference design [2] for DDR3L settings guidelines. The DDR3L SDRAM parameters and the DDR3L board timing information to be set in Vivado project are presented in Tables 20 and 21.

The values given in Table 20 are for reference only. Depending on the equipped memory device on the Mars ZX2 SoC module and on the DDR3L SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
Memory type	DDR3L
DRAM bus width	16 bit
Operating frequency	400-533 MHz
DRAM chip bus width	16 bit
DRAM chip capacity	4096 Mbit
Speed bin	DDR3L_1066F
Bank bits	3
Row bits	15
Column bits	10
CAS latency	7
CAS write latency	6
RAS to CAS delay	7
Precharge time	7
tRC	48.75 ns
tRASmin	35.0 ns
tFAW	40.0 ns

Table 20: DDR3L SDRAM Parameters

Parameter	Byte 3	Byte 2	Byte 1	Byte 0
DQS to clock delay (ns)	0.098	0.077	0.059	-0.012
Board delay (ns)	0.233	0.250	0.248	0.284

Table 21: DDR3L Board Timing

2.15 QSPI Flash

The QSPI flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

2.15.1 QSPI Flash Type

Table 22 describes the memory availability and configuration on the Mars ZX2 SoC module.

As there is one QSPI flash chip equipped on the Mars ZX2 SoC module, type “single” must be selected when programming the flash from Vivado tools.

Flash Type	Size	Manufacturer
S25FL512S	512 Mbit	Cypress (Spansion)

Table 22: QSPI Flash Type

Warning!

Other flash memory devices may be equipped in future revisions of the Mars ZX2 SoC module. Please check the user manual regularly for updates. Any parts with different speeds and temperature ranges that fulfill the requirements for the module variant may be used.

2.15.2 Signal Description

The QSPI flash is connected to the PS MIO pins 1-6. Some of the signals are available on the module connector, allowing the user to program the QSPI flash from an external master.

Please refer to Section 3 for details on programming the flash memory.

Warning!

Special care must be taken when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the SoC and the flash device.

2.15.3 Configuration

The QSPI flash supports up to 50 MHz operation for standard read. For fast, dual and quad read speed values, please refer to the flash device datasheet.

Note that the "Feedback Clk" option on pin MIO8 must be enabled in the Zynq configuration for clock rates higher than 40 MHz.

24-bit Address Compatibility Mode

If the Zynq device boots from the QSPI flash and the 24-bit address compatibility mode of the QSPI flash is used to access the range above 16 MB, then the compatibility mode must be disabled before a system reset is executed. Otherwise, the Zynq device will not be able to boot from the QSPI flash again, as the address register is not pointing to the lower addressed part of the memory, in which the boot image is located.

The reset of the QSPI flash is connected to the PS_POR# power-on reset signal in order to avoid this issue after a power-on reset. The PS_SRST# signal should not be used in this setup.

Please refer to Zynq-7000 Technical Reference Manual [19] for details on booting from the QSPI flash.

2.15.4 QSPI Flash Corruption Risk

There have been cases in which it was observed that the content of the flash device got corrupted. According to Cypress, this issue is caused by power loss during the Write Register (WRR) command. The most common reason to use the WRR command is to turn the QUAD bit ON or OFF - this operation takes place usually at the beginning of the boot process. If required, the bootloader code can be adjusted to set the QUAD bit to a fixed value, without invoking this command during boot.

For additional information on this issue, please refer to the Cypress documentation and forum discussions [27], [28].

2.16 SD Card

An SD card can be connected to the PS MIO pins 40-45 or 46-51, or alternatively via EMIO pins to the PL.

The corresponding MIO pins are available on the module connector. Note that only MIO pins 40-45 allow the Mars ZX2 SoC module to boot from the SD card. Information on this boot mode is available in Section 3.6.

Please note that external pull-ups are needed for SD card operation. Depending on the selected voltage for VCC_CFG_MIO_B13, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

2.17 Gigabit Ethernet

A 10/100/1000 Mbit Ethernet PHY is available on the Mars ZX2 SoC module, connected to the PS via RGMII interface. The RGMII interface is connected to MIO pins 16-27 for use with the hard macro MAC.

Please note that Xilinx recommends operation at 1.8 V/2.5 V for the RGMII interface for the MIO pins [19]. Enclustra tests have shown that the RGMII is functional with a 3.3 V I/O voltage on the MIO pins, as long as the I/O voltage configured in Vivado matches the applied I/O voltage.

2.17.1 Ethernet PHY Type

Table 23 describes the equipped Ethernet PHY device type on the Mars ZX2 SoC module.

PHY Type	Manufacturer	Type
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 23: Gigabit Ethernet PHY Type

2.17.2 Signal Description

The RGMII interface is connected to MIO pins 16-27 for use with the hard macro MAC. The interrupt output of the Ethernet PHY is connected to the I2C interrupt line, available on MIO pin 9 and on an EMIO pin (only on XC7Z020 device).

The Gigabit Ethernet connections are presented in Table 24. All listed pins are operated at VCC_CFG_MIO_B13 I/O voltage.

Signal Name	MIO Pin	PL Pin
ETH_RST#	PS_POR_B	-
I2C_INT#	MIO9	Y6 (not available on XC7Z010 device)
ETH_MDC	MIO52	-
ETH_MDIO	MIO53	-
ETH_RXC	MIO22	-
ETH_RX_CTL	MIO27	-
ETH_RXD0	MIO23	-
ETH_RXD1	MIO24	-
ETH_RXD2	MIO25	-
ETH_RXD3	MIO26	-
ETH_TXC	MIO16	-
ETH_TX_CTL	MIO21	-
ETH_TXD0	MIO17	-
ETH_TXD1	MIO18	-
ETH_TXD2	MIO19	-
ETH_TXD3	MIO20	-

Table 24: Gigabit Ethernet Signal Description

2.17.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.17.4 MDIO Address

The MDIO address assigned to the Gigabit Ethernet PHY is 3. The MDIO interface is connected to MIO pins 52-53.

2.17.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 25.

Please note that the RGMII delays in the Ethernet PHY need to be configured before the Ethernet interface can be used. This is done in the source files within the First Stage Boot Loader (FSBL) application provided in the Mars ZX2 SoC module reference design [2].

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 25: Gigabit Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

2.18 USB 2.0

The Mars ZX2 SoC module has an on-board USB 2.0 PHY connected to the SoC device. The USB interface can be configured for USB host, USB device and USB On-The-Go (host and device capable) operations.

2.18.1 USB PHY Type

Table 26 describes the equipped USB PHY device type on the Mars ZX2 SoC module.

PHY Type	Manufacturer	Type
USB3320C	Microchip	USB 2.0 PHY

Table 26: USB 2.0 PHY Type

2.18.2 Signal Description

The ULPI interface is connected to MIO pins 28-39 for use with the integrated USB controller.

2.19 Real-Time Clock (RTC)

A real-time clock is connected to the I2C bus. VCC pin of the RTC is connected to VCC_BAT on the module connector, and can be connected directly to a 3 V battery. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details.

Refer to Section 4 for details on the I2C bus on the Mars ZX2 SoC module.

The interrupt output of the RTC is connected to the I2C interrupt line, available on MIO pin 9 and on an EMIO pin (only on XC7Z020 device).

2.19.1 RTC Type

Table 27 describes the equipped RTC device type on the Mars ZX2 SoC module.

Type	Manufacturer
PCF85063ATL/1,118	NXP Semiconductors

Table 27: RTC Type

An example demonstrating how to use the RTC is included in the Mars ZX2 SoC module reference design [2].

2.20 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

2.20.1 EEPROM Type

Table 28 describes the equipped EEPROM device type on the Mars ZX2 SoC module.

Type	Manufacturer
ATSHA204A-MAHDA-T (default)	Atmel
DS28CN01 (assembly option)	Maxim

Table 28: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mars ZX2 SoC module reference design [2].

3 Device Configuration

3.1 Configuration Signals

The PS of the SoC needs to be configured before the FPGA logic can be used. Xilinx Zynq devices need special boot images to boot from QSPI flash or SD card. For more information, please refer to the Xilinx Zynq-7000: Concepts, Tools, and Techniques document [21].

Table 29 describes the most important configuration pins and their location on the module connector. These signals allow the SoC to boot from QSPI flash or SD card, and can be used to program the QSPI flash from an external master. Please refer to Section 3.8 for details.

Signal Name	SoC Pin Type	Module Connector Pin	Description	Comments
FLASH_CLK	MIO6	182	SPI CLK	20 kΩ pull-down
FLASH_DO	MIO3	184	SPI MISO	20 kΩ pull-down
FLASH_DI	MIO2	186	SPI MOSI	20 kΩ pull-down
FLASH_CS#	MIO1	188	SPI CS#	10 kΩ pull-up to VCC_CFG_MIO_B13
FPGA_DONE	DONE_0	194	FPGA configuration done	1 kΩ pull-up to VCC_CFG_MIO_B13
FPGA_CFGBVS	CFGBVS_0	-	Configuration bank voltage select[5]	10 kΩ pull-up to VCC_CFG_MIO_B13
PS_POR#	PS_POR_B	196	Must be pulled to GND for a short period before QSPI flash programming. PS_SRST# must be low when PS_POR# is released.	10 kΩ pull-up to VCC_CFG_MIO_B13
PS_SRST#	PS_SRST_B	192	Must be pulled to GND during QSPI flash programming. When released, all other pins of the SPI interface must be high impedance.	10 kΩ pull-up to VCC_CFG_MIO_B13
BOOT_MODE	-	190	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO_B13

Table 29: SoC Configuration Pins

[5] The CFGBVS_0 pin is set automatically to GND (if VCC_CFG_MIO_B13 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_MIO_B13 is 2.5 V or 3.3 V).

Warning!

All configuration signals except for BOOT_MODE signal must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped SoC device, as well as other devices on the Mars ZX2 SoC module.

3.2 Pull-Up During Configuration

Figure 10 illustrates the configuration of the I/O signals during power-up.

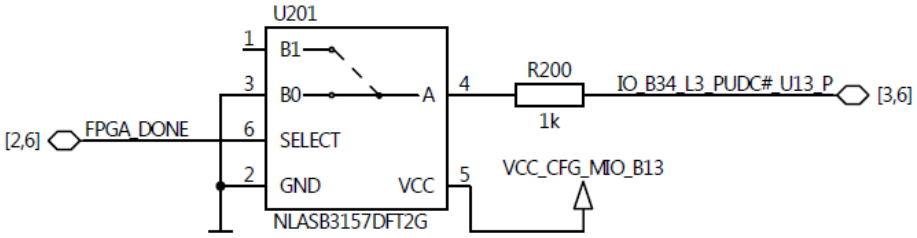

Figure 10: Pull-Up During Configuration (PUDC)

The Pull-Up During Configuration signal (PUDC) is configured using a multiplexer to low state during FPGA configuration, and to high impedance after this process is done.

If the user does not drive a high value on this signal during configuration, then the PUDC signal will be pulled to GND via a 1 kΩ resistor. As PUDC is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires that all FPGA I/Os have the internal pull-up resistors disabled during device configuration, the user must attach to the module connector a driver capable to pull IO_B34_L3_PUDC#_U13_P signal high.

For details on the PUDC signal please refer to the Zynq-7000 All Programmable SoC Technical Reference Manual [19].

3.3 Boot Mode

The boot mode can be selected via a signal available on the module connector.

Table 30 describes the available boot modes on the Mars ZX2 SoC module.

BOOT_MODE[6]	Description
0	Boot from QSPI flash
1	Boot from SD card

Table 30: Boot Mode Selection

[6]Revision 1 modules have two boot mode selection signals, offering an extra option: JTAG boot mode. Note that the JTAG configuration interface is always available, regardless of the mode pin settings.

3.4 JTAG

The FPGA and the PS JTAG interfaces are connected into one single chain available on the module connector. The SoC device and the QSPI flash can be configured via JTAG from Xilinx SDK or Xilinx Vivado Hardware Manager.

3.4.1 JTAG on Module Connector

Signal Name	Module Connector Pin	Resistor
JTAG_TCK	158	20 kΩ pull-up to VCC_CFG_MIO_B13
JTAG_TMS	162	SoC internal pull-up
JTAG_TDI	160	SoC internal pull-up
JTAG_TDO	164	-

Table 31: JTAG Interface

3.4.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to VCC_CFG_MIO_B13.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.5 QSPI Boot Mode

In the QSPI boot mode, the PS boots from the QSPI flash located on the module. The flash device is connected to the PS MIO pins 1-6.

In order to boot from the QSPI flash, the user must enable the QSPI flash controller in the Vivado block design and generate a new FSBL to be used for the Zynq boot image creation.

3.6 SD Card Boot Mode

In the SD card boot mode the PS boots from the SD card located on the base board.

For this operation, the following requirements must be met:

- The SD card must be connected to MIO pins 40-45
- A Zynq boot image must be generated from an SoC design having the SDIO controller enabled
- The boot image must be named “boot.bin” and then copied to the SD card
- In software versions older than Vivado 2014.4, the card detect check in the Xilinx FSBL must be disabled. For details, please contact Enclustra Support team.
- The SDIO controller must be fed with a reasonable clock frequency. Please refer to the reference design for guidelines on SDIO settings.

For details on SD card boot, please refer to the Xilinx Zynq documentation [19] [21].

3.7 QSPI Flash Programming via JTAG

The Xilinx Vivado and SDK software offer QSPI flash programming support via JTAG. For more information, please refer to the Xilinx Documentation [23].

3.8 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the SoC device as well, the SoC device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the PS_SRST# signal to GND followed by a pulse on PS_POR#, which puts the SoC device into reset state and tri-states all I/O pins. PS_SRST# must be low when PS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI lines and PS_SRST# must be tri-stated and another reset impulse must be applied to PS_POR#.

Figure 11 shows the signal diagrams corresponding to flash programming from an external master.

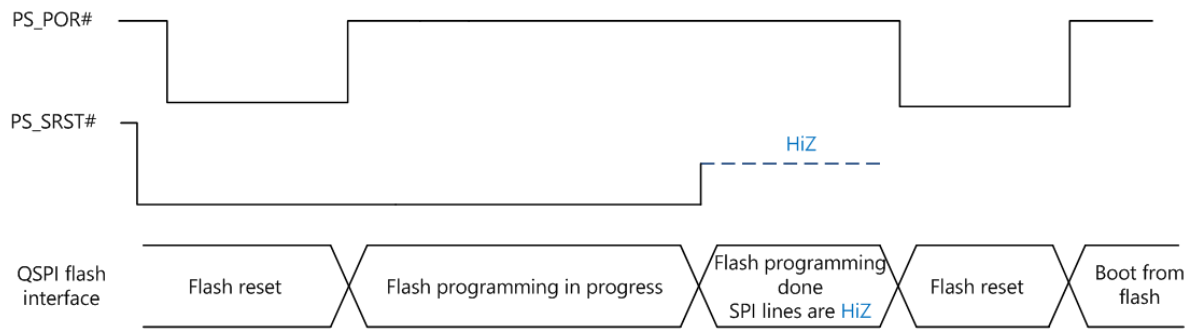

Figure 11: QSPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the QSPI flash directly without putting the SoC device into reset may damage the equipped SoC device, as well as other devices on the Mars ZX2 SoC module.

3.9 FPGA and QSPI Flash Programming using Xilinx Impact

For Zynq-7000 devices, Xilinx Impact requires JTAG boot mode to be selected in order to download the bitstream or program the QSPI flash. For an easy configuration, it is recommended to use Xilinx SDK or Vivado instead of Impact.

3.10 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using the Enclustra Module Configuration Tool (MCT) [17].

Please note that the Xilinx Zynq devices do not support slave serial configuration, therefore only flash programming is supported by the Enclustra MCT for the Mars ZX2 SoC module.

4 I2C Communication

4.1 Overview

The I2C bus on the Mars ZX2 SoC module is connected to the SoC device, EEPROM and RTC, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 32 describes the signals of the I2C interface. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the SoC and must not be driven from the SoC device.

Level shifters are used between the I2C bus and the PS/PL pins to allow I/O voltages lower than 3.3 V. The MIO and EMIO pins are connected in parallel. Please make sure that all pins are configured correctly and no pull-down resistors are enabled.

Signal Name	PS Pin	PL Pin	Connector Pin	Resistor
I2C_SDA	MIO15	W8	176	2.2 kΩ pull-up
I2C_SCL	MIO14	V8	178	2.2 kΩ pull-up
I2C_INT#	MIO9	Y6	174	10 kΩ pull-up

Table 32: I2C Signal Description

4.3 I2C Address Map

Table 33 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description
0x64	Secure EEPROM
0x5C	Secure EEPROM (assembly option, refer to Section 2.20)
0x51	RTC registers

Table 33: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read the module information from the EEPROM memory is included in the Mars ZX2 SoC module reference design.

Warning!

The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	32	Module configuration
0x0C	32	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 34: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mars ZX2 SoC module	0x0329	0x[XX]	0x[YY]	0x0329 [XX][YY]

Table 35: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	SoC type	0	1	See SoC type table (Table 37)
	3-0	SoC device speed grade	1	3	
0x09	7	Temperature range	0 (Commercial)	1 (Industrial)	
	6	Power grade	0 (Normal)	1 (Low Power)	
	5-4	Ethernet port count	0	1	
	3	Ethernet speed	0 (Fast Ethernet)	1 (Gigabit Ethernet)	
	2	RTC equipped	0	1	
	1-0	Reserved	-	-	
0x0A	7-2	Reserved	-	-	
	1-0	USB 2.0 port count	0	1	
0x0B	7-4	DDR3L RAM size (MB)	0 (0 MB)	8 (1 GB)	Resolution = 8 MB
	3-0	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB

Table 36: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 8 MB, DRAM=2: 16 MB, DRAM=3: 32 MB, etc).

Table 37 shows the available SoC types.

Value	SoC Device Type
0	XC7Z010
1	XC7Z020

Table 37: SoC Device Types

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 38 indicates the absolute maximum ratings for Mars ZX2 SoC module. The values given are for reference only; for details please refer to the Zynq-7000 DC and AC Switching Characteristics Datasheet [24].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 6	V
VCC_3V3	3.3 V supply voltage relative to GND	-0.5 to 3.6	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	-0.3 to 3.6	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	-0.5 to 3.6	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCO}+0.5	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 38: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 39 indicates the recommended operating conditions for Mars ZX2 SoC module. The values given are for reference only; for details please refer to the Zynq-7000 DC and AC Switching Characteristics Datasheet [24].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	3.0 to 5.5	V
VCC_3V3	3.3 V supply voltage relative to GND	3.15 to 3.45	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	2.0 to 3.45	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCO}+0.2	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 39: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

List of Figures

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References

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→ Ask Enclustra for details
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