DAC8881 Evaluation Module

This user's guide describes the characteristics, operation, and the use of the DAC8881 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

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1 EVM Overview

This chapter provides a general overview of the DAC8881 evaluation module (EVM) and describes some of the factors that must be considered in using this module.

1.1 Features

This EVM features the DAC8881 digital-to-analog converter. The DAC8881 EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality and performance of the 16-bit high resolution, voltage output, single channel, and serial input DAC. This EVM features a high-speed serial interface of up to 50MHz to communicate with any host microprocessor or DSP-based system.

The DAC8881 is designed for unipolar output operation (default mode), but it can also be configured for bipolar output operation with the addition of an external amplifier and some resistors. The option for bipolar mode of operation is included in the EVM with just some minor jumper configuration.

A +5V precision voltage reference is provided on-board via U3 (REF02) to supply the necessary external reference voltage to set the DAC8881 output range. The footprint of U3 is compatible with many SO-8 package type reference devices, so the user has the flexibility to select the reference supply to set the output range of the DAC8881 other than what is provided on-board. The family of REF50xx precision reference sources works well with this EVM. In addition, the provision of test points, TP1 and TP8, allows the user to use their own external reference supply. Typically, TP1 ($V_{REF}L$) should be connected to ground, but it can accept up to ±0.2V if necessary. The test point, TP8 ($V_{REF}H$), is typically set to +5V, but can accept a minimum of +1.25V and up to a maximum of +5.5V.

The voltage reference configuration implemented on this EVM utilizes the Kelvin connection feature of the DAC8881 device. This connection helps minimize the internal errors caused by the changing reference current and its associated circuit impedances.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The dc power supply requirement for this DAC8881 EVM (AV_{DD} and DV_{DD}) is selectable between +3.3VA and +5VA via the W1 jumper. The +3.3VA comes from the J6-8 terminal and the +5VA comes from the J6-3 terminal. These power supply voltages are referenced to analog ground through the J6-5 and J6-6 terminals.

The logic voltage, IOV_{DD}, is selectable between +1.8VD, +3.3VD, and +5VD via the J3 jumper.

V_{CC} and V_{SS} range from +15V to –15V maximum and connect through the J6-1 and J6-2 terminals respectively. All analog power supplies are referenced to analog ground through the J6-5 and J6-6 terminals.

CAUTION

To avoid potential damage to the EVM board, make sure the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The DAC8881 requires an external reference source to set the DAC operating voltage output range. Applying the desired voltage in the range of 1.25V to AV_{DD} to the $V_{REF}H$ pin sets the positive range of the DAC8881 output. Applying the desired voltage in the range of –0.2V to +0.2V to the $V_{REF}L$ pin sets the negative range of the DAC8881 output, although the $V_{REF}L$ pin should nominally be set to 0V. The voltages applied to the $V_{REF}H$ and $V_{REF}L$ pins set the DAC8881 full output voltage swing.

For optimum performance, the DAC8881 supports a set Kelvin connection to the external reference via the $V_{REFH}F$ and $V_{REFH}S$ pins as well as $V_{REFL}F$ and $V_{REFL}S$ pins. This optional reference configuration minimizes internal errors caused by the changing reference current and its associated circuit impedances.

A +5V precision voltage reference is provided for the external reference source of the DAC through REF02, U3. The power supply for the reference device, U3, is selectable between V_{CC} and +5VA via the W11 jumper to ensure that the correct voltage range of U3 can be set. As mentioned earlier, a device from the family of REF50xx reference devices can be easily selected and the one installed on the EVM can be replaced to provide the desired voltage range that is required for evaluation of the DAC8881.

The reference voltages, $V_{REF}H$ and $V_{REF}L$, are selectable via jumpers W8 and W4. When shorting pins 1 and 2 of both jumpers, the on-board +5V reference via U3 is selected. Shorting pins 2 and 3 of both jumpers selects the reference voltages that are applied via J4 pins 18 and 20 respectively. These voltages normally come from the host platform that is interfaced with the DAC8881EVM.

The test points TP1 and TP8 are also provided to allow the user to connect another external reference source if the on-board reference circuit is not desired. The external voltage reference should not exceed the applied power supplies (AV_{DD} and DV_{DD}) of the DAC under test.

CAUTION

When applying an external voltage reference through TP8 or J4-20, make sure that it does not exceed the applied AV_{DD}. Otherwise, this can permanently damage the DAC8881, U1, device under test.

1.3 EVM Basic Functions

This EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC8881 digital-to-analog converter. Functional evaluation of the installed DAC device can be accomplished with the use of any microprocessor, DSP, or signal/waveform generator.

The headers J2 (top side) and P2 (bottom side) are pass-through connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8881 EVM using a custom built cable.

An adapter interface card (5-6k adapter interface card) is also available to fit and mate with TI's C5000 and C6000 DSP Starter Kit (DSK). This card alleviates the problems involved in building a custom cable. In addition, the Precision Analog Application group of Texas Instruments has other interface boards that are designed to connect to and interface with this EVM as well. For more details or information regarding the 5-6k adapter interface board or the other interface platforms, call Texas Instruments Inc. or send an email to dataconvapps@list.ti.com.

The DAC output can be monitored through pins 2 and 6 of the J4 header connector. The DAC output can be switched through the W2 jumper for stacking the EVM for daisy-chaining purposes.

A block diagram of the EVM is shown in the Figure 1.

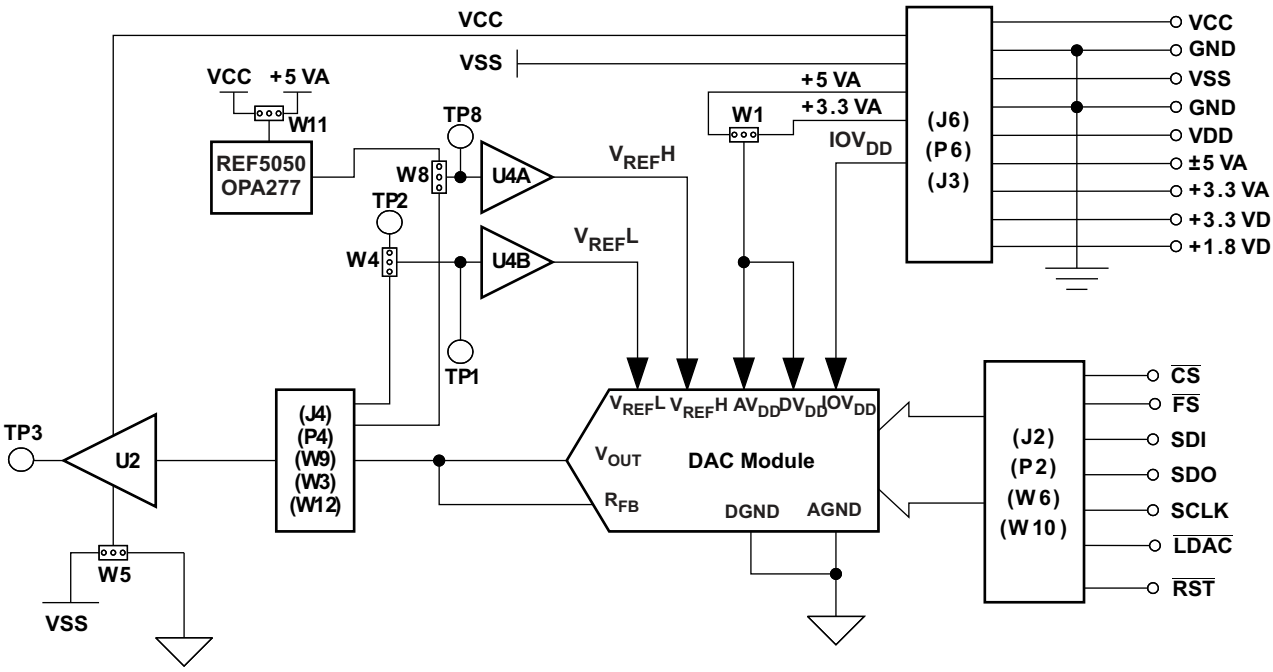


Figure 1. Block Diagram

2 PCB Design and Performance

This chapter describes the layout design of the PCB, the physical and mechanical characteristics of the EVM, and the EVM test performance procedure performed. The list of components on this evaluation module is also included in this section.

2.1 PCB Layout

The DAC8881 EVM is designed to preserve the performance quality of the DAC, device under test, as specified in the datasheet. Carefully analyzing the physical restrictions of the EVM and the given or known elements that contribute to performance degradation of the EVM is key to a successful design implementation. These obvious attributes that diminish the performance of the EVM can be addressed during the schematic design phase by selecting appropriate components and building a correct circuit. The circuit should include adequate bypassing, identifying and managing analog and digital signals, and knowing or understanding the mechanical attributes of the components.

The critical part of the design is the layout process. The main concern is primarily the placement of components and the proper routing of signals. The bypass capacitors should be placed as close as possible to the pins, and the analog and digital signals should be properly separated from each other. The power and ground plane is very important and should be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical, so when a solid plane is not possible, a split plane is an acceptable alternative. When considering a split plane design, analyze component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling noise and other effects that otherwise contribute to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the largest possible trace width allowable in the design. These design practices can be seen in the following figures.

The DAC8881 EVM board is constructed on a four-layer printed circuit board using a copper-clad FR-4 laminate material. The printed circuit board has dimensions of 43,1800 mm (1.7000 inch) × 82,5500 mm (3.2500 inch), and the board thickness is 1,5748 mm (0.062 inch). Figure 2 through Figure 8 show the individual artwork layers.

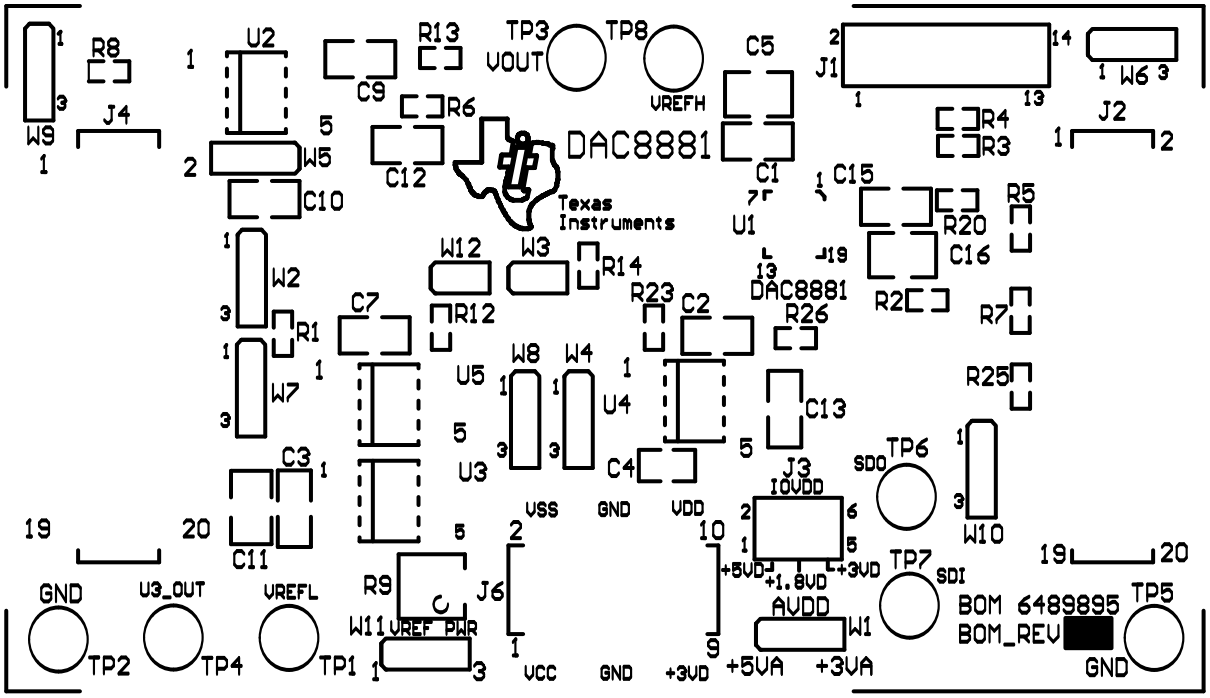


Figure 2. Top Silkscreen

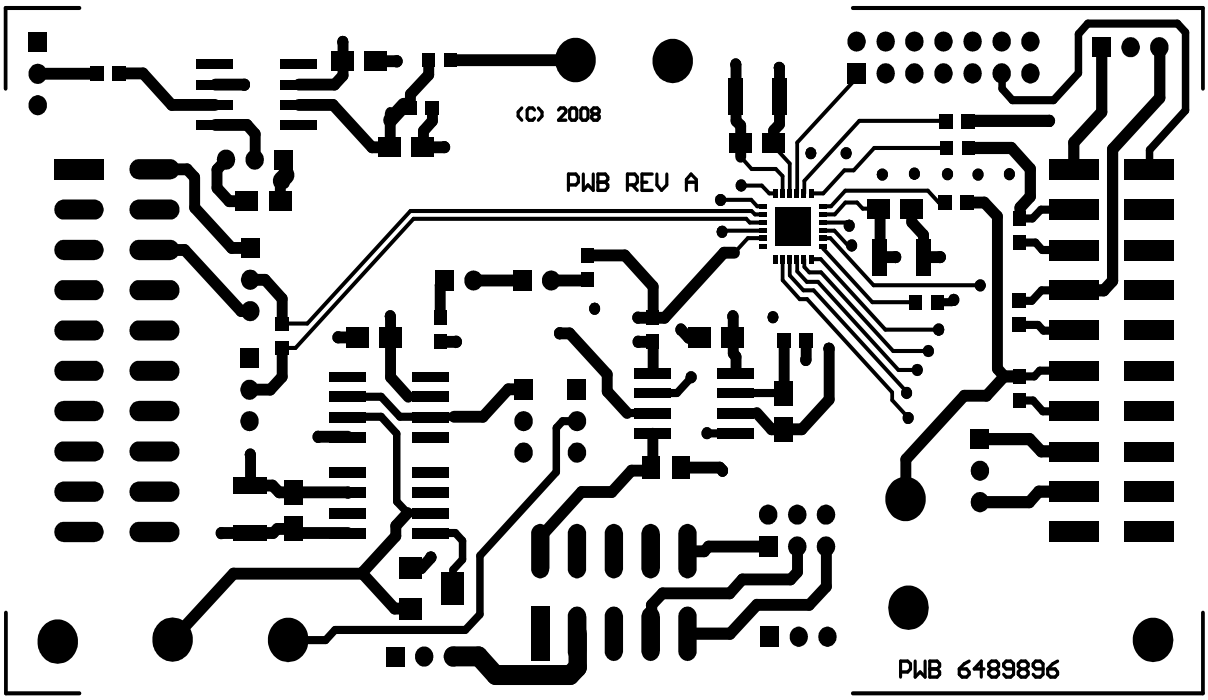


Figure 3. Layer 1 (Top Signal Plane)

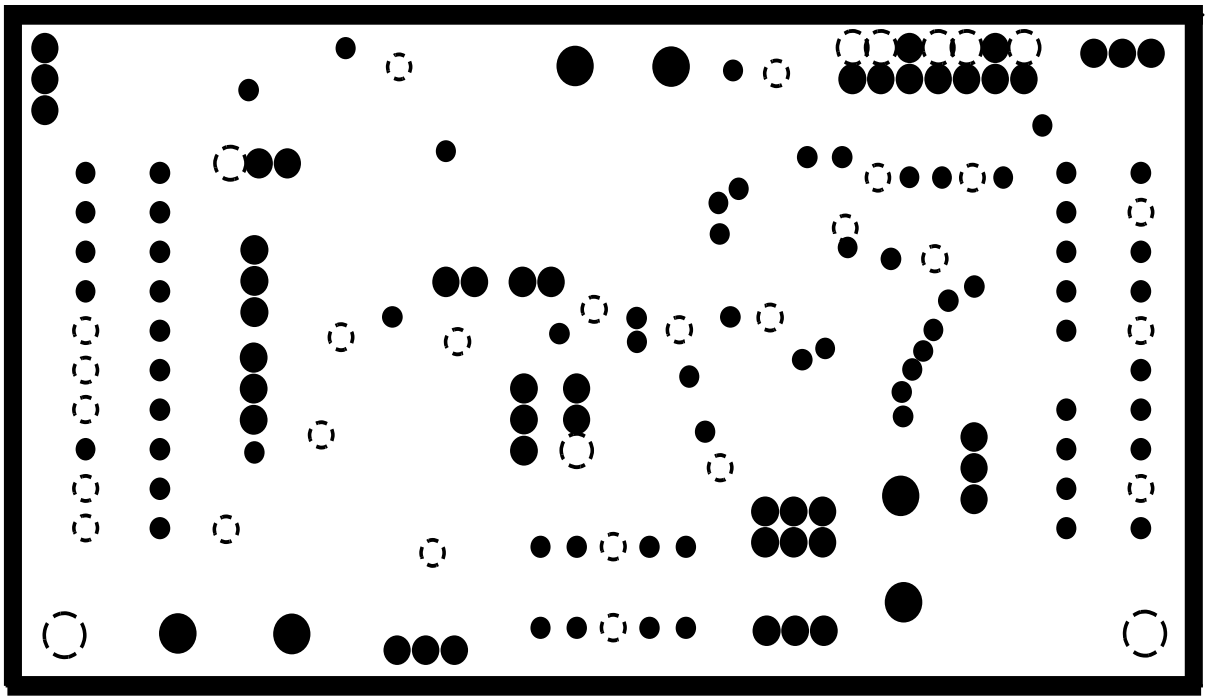


Figure 4. Layer 2 (Ground Plane)

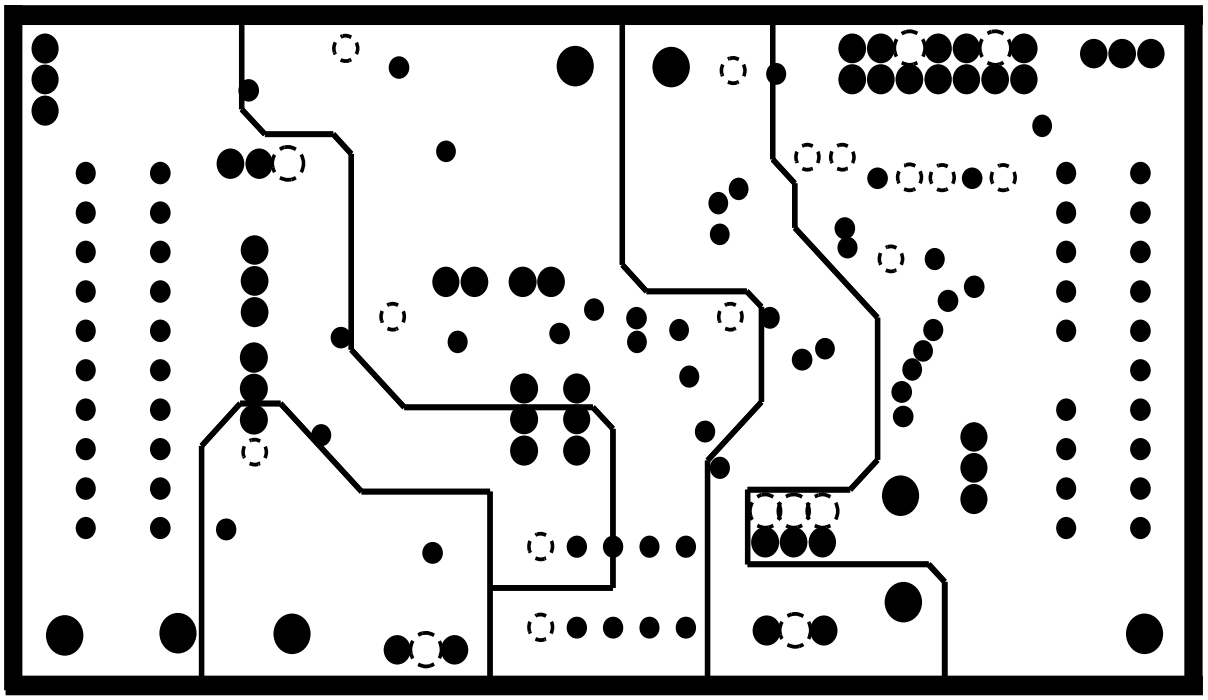


Figure 5. Layer 3 (Power Plane)

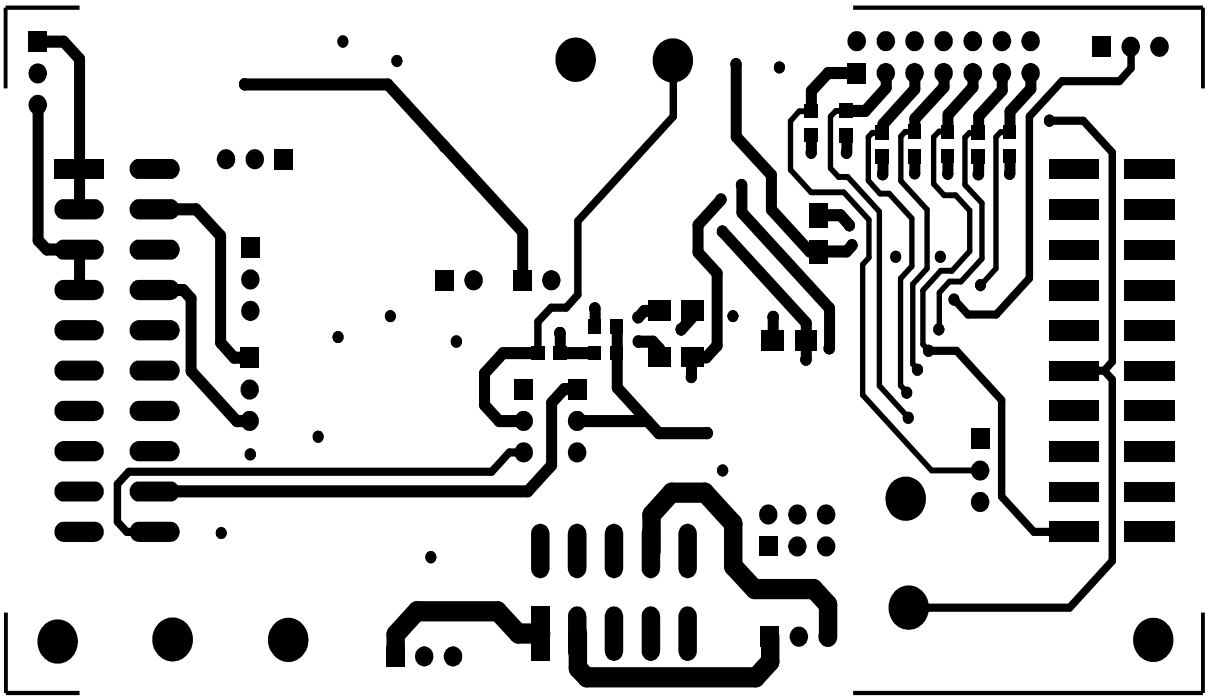


Figure 6. Layer 4 (Bottom Signal Plane)

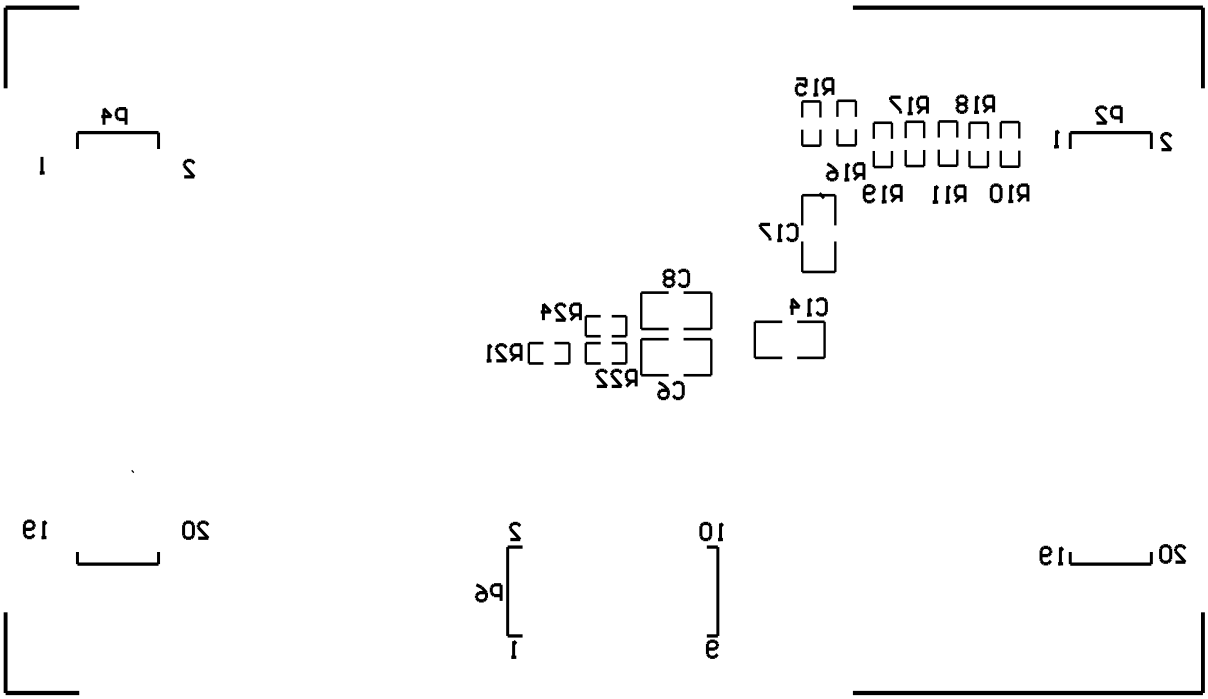


Figure 7. Bottom Silkscreen

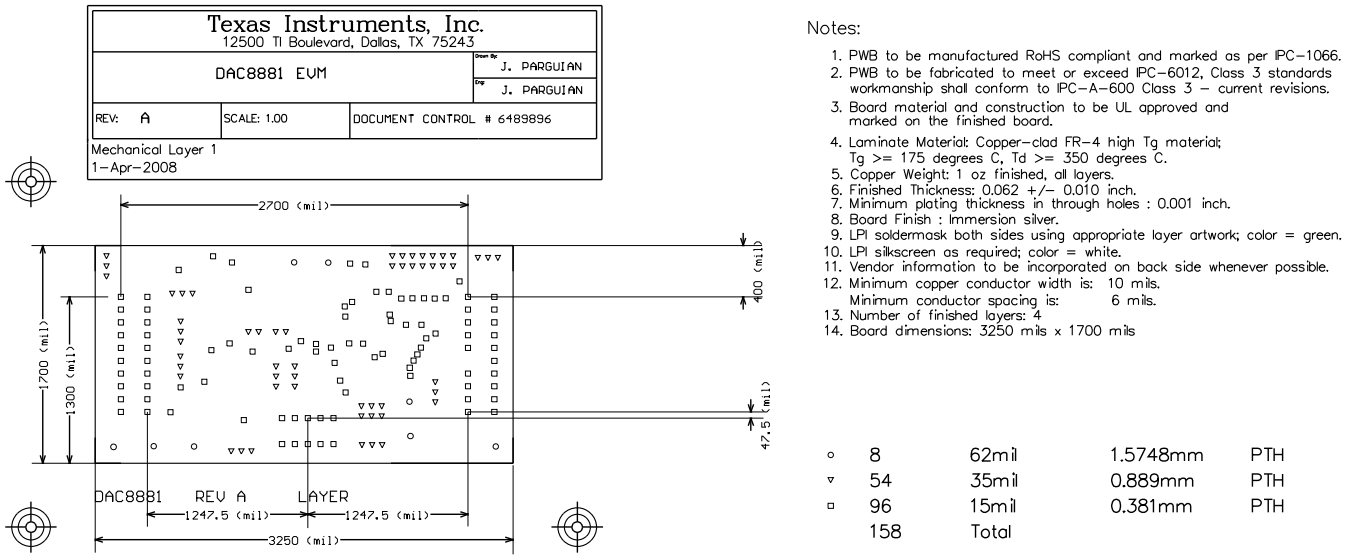


Figure 8. Drill Drawing

2.2 EVM Performance

The EVM performance test is performed using a high density DAC bench test board, an Agilent 3458A digital multimeter, and a PC running LabVIEW software. The EVM board is tested for all codes of 65535, and the device under test (DUT) is allowed to settle for 1ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL.

Figure 9 shows the INL and DNL characteristic plots.

Figure 9. INL and DNL Characteristic Plots

2.3 Bill of Materials

Table 1. Parts List

Item	Qty.	Designators	Description	Manufacturer	Mfg. Part Number
1	1	N/A	Printed wiring board	Texas Instruments	6489896
2	3	C8 C12 C14	1000 pF, 0805, ceramic cap, COG, 50V, 5%	TDK	C2012C0G1H102J
3	3	C5 C11 C16	10 µF, 1210, ceramic cap, X7R, 16V	TDK	C3225B63X7R1C106Z
4	7	C1 C2 C3 C4 C7 C15 C17	0.1 µF, 0805, ceramic cap, X7R, 50V, 10%	TDK	C2012X7R1H104K
5	2	C9 C10	1 µF, 0805, ceramic cap, X7R, 16V, 10%	TDK	C3216X7R1C105K
6	2	C6 C13	2200 pF, 0805 ceramic cap, COG, 50V, 5%	TDK	C2012C0G1H222J
7	1	J1	7 × 2 × 2mm terminal strip	Samtec	TMM-107-01-T-D
8	1	J3	3 × 2 × 2mm terminal strip	Samtec	TMM-103-01-T-D

Table 1. Parts List (continued)

Item	Qty.	Designators	Description	Manufacturer	Mfg. Part Number
9	2	J2 J4 (Top Side)(1)	10 pin, dual row, TH header (20 pos.)	Samtec	TSM-110-01-T-DV-P
10	1	J6 (Top Side)(1)	5 pin, dual row, TH header (10 pos.)	Samtec	TSM-105-01-T-DV-P
11	2	P2 P4 (Bottom Side)(1)	10 pin, dual row, TH header (20 pos.)	Samtec	SSW-110-22-F-D-VS-K
12	1	P6 (Bottom Side)(1)	5 pin, dual row, TH header (10 pos.)	Samtec	SSW-105-22-F-D-VS-K
13	1	R13	Resistor, 100 Ω, 0603, 1/4 W	Yageo America	9C06031A1000JLHFT
14	6	R1 R2 R3 R4 R8 R20	Resistor, 0 Ω, 0603	Yageo America	9C06031A0R00JLHFT
15	2	R23 R26	Resistor, 49.9 Ω 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF49R9V
16	2	R21 R24	Resistor, 2 kΩ, 0603,	Yageo America	9C06031A2001JLHFT
17	1	R9	Resistor, 20 kΩ, 32X4W	Bourns	3214W-1-203E
18	10	R6 R10 R11 R12 R14 R15 R16 R17 R18 R19	Resistor, 10 kΩ, 0603	Yageo America	9C06031A1002JLHFT
19	1	R22	Resistor, 95.3 Ω, 0603 SMD	Panasonic	ERJ-3EKF95R3V
20	8	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8	Test point turret	Mill-Max	2348-2-00-01-00-00-07-0
21	1	U1	16-bit, buffered voltage output DAC	Texas Instruments	DAC8881SRGET
22	1	U2	High precision op-amp	Texas Instruments	OPA211AIDR
23	1	U3	5V precision voltage reference	Texas Instruments	REF5050AID
24	1	U4	High precision dual op-amp	Texas Instruments	OPA2277UA
25	1	U5	High precision, op-amp	Texas Instruments	OPA277UA
26	10	W1 W2 W4 W5 W6 W7 W8 W9 W10 W11	3 pin mini header	Samtec	TMMH-103-01-T-T
27	2	W3 W12	2 pin mini header	Samtec	TMMH-102-01-T-T
28	10	Shunt	2mm shunt – black	Samtec	2SN-BK-G
29	0	R5 R7 R25(2)	DNP	–	–
30	1	Shunt	0.100 shunt – black	Samtec	SNT-100-BK-T

(1) P2, P4, and P6 parts are not shown in the schematic diagram. All P designated parts are installed on the bottom side of the PC board opposite the J designated counterpart. Example, J2 is installed on the top side while P2 is installed on the bottom side opposite of J2.
(2) Do **NOT** install the following: R5, R7, and R25.

3 EVM Operation

This chapter describes in detail the operation of the EVM to provide guidance to the user in evaluating the on-board DAC and how to interface the EVM to a specific host processor.

Refer to the DAC8881 data sheet, (SBAS422) for information about its serial interface and other related topics.

The EVM board is factory tested and configured to operate in the unipolar output mode.

3.1 Factory Default Settings

The EVM board is set to its default configuration from the factory to operate in unipolar +5V mode of operation as described in Table 2. Figure 10 shows the default jumper configuration as described in Table 2 for the DAC8881.

Table 2. Factory Default Jumper Settings

Reference	Jumper Position	Function
W1	1-2	The +5VA is used for AV_{DD} and DV_{DD} to power the analog and digital supplies of the DAC8881.
W2	1-2	Routes V_{OUT} of the DAC8881 to J4-2 for analog output monitoring.
W3	OPEN	Disconnects $V_{REF}H$ from the inverting input of U2 for other output mode of configuration.
W4	2-3	Connects the $V_{REF}L$ pin of the DAC8881 to ground.

Table 2. Factory Default Jumper Settings (continued)

Reference	Jumper Position	Function
W5	1-2	Negative supply rail of the output op-amp, U2, is powered by V_{SS} for bipolar operation.
W6	2-3	$\overline{FS}$ signal from J2-7 is routed to drive the $\overline{CS}$ signal of the DAC8881.
W7	OPEN	Leave this jumper open since R1 is installed. This is the default mode of the EVM from the factory.
W8	1-2	Routes the on-board +5V voltage reference, $V_{REF}H$ for the DAC.
W9	1-2	Routes V_{OUT} and R_{FB} from J4-2 and J4-4 (if they are shunted) to the non-inverting input of U2 op-amp.
W10	OPEN	$\overline{LDAC}$ signal of the DAC8881 is tied to ground for synchronous update of the DAC8881 output.
W11	1-2	Routes V_{CC} to power the analog supply of the U3 reference device.
W12	OPEN	Disconnects the inverting input of U2 from R12 gain resistor for other output mode of configuration.
J1	1-2	$\overline{LDAC}$ signal of the DAC8881 is tied to ground for synchronous DAC update operation.
J2	1-2	The V_{OUT} pin of the DAC8881 is connected to the noninverting input of the op-amp, U2.
J3	5-6	IOV_{DD} of the DAC8881 is powered with +3.3VD.
J4	1-2	The V_{OUT} pin of the DAC8881 is connected to the noninverting input of the op-amp, U2.

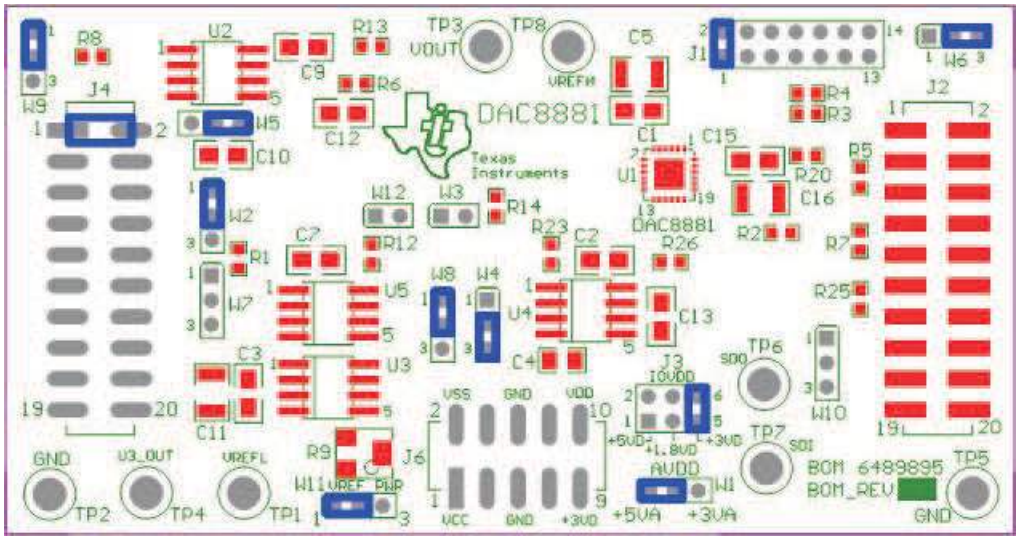


Figure 10. DAC8881 EVM Default Jumper Configuration

3.2 Host Processor Interface

The host processor basically drives the DAC, so the DACs proper operation depends on the successful configuration between the host processor and the EVM board. In addition, properly written code is also required to operate the DAC.

A custom cable can be made specifically for the user selected host interface platform. The EVM interfaces to the host processor through the J2 header connector for the serial control signals and the serial data input.

An interface adapter card is also available for a specific TI DSP starter kit as well as other interface platforms designed by the Precision Analog Applications group of Texas Instruments, as mentioned in chapter 1 of this manual. Using the interface card alleviates the tedious task of building a customized cable and allows easy configuration of a simple evaluation system.

The DAC8881 interfaces with any host processor capable of handling SPI protocols or a popular TI DSP. For more information regarding the DAC8881 data interface, refer to the data sheet (SBAS422).

3.3 Digital Control Interface

The DAC8881 supports the standard high-speed SPI™ serial interface to communicate with microprocessors or DSP devices. The EVM incorporates pass-through connectors to accommodate the digital control interface to the DAC8881 device via the J2 (top side) and P2 (bottom side) header/socket connectors. The signals of these pass-through connectors are listed in Table 3.

Table 3. Digital Control Interface Signal Mapping for J2/P2 Header/Socket Connectors

Pin Number	Signal	Function
J2.1/P2.1	$\overline{CS}$	Primary synchronization and device enable input for the DAC8881. Host microcontroller STE signal for SPI interface.
J2.3/P2.3	SCLK	Serial interface clock.
J2.5/P2.5	CLKR	Unused.
J2.7/P2.7	$\overline{FS}$	Secondary synchronization and device enable input for the DAC8881. Host microcontroller STE signal for SPI interface or $\overline{FS}$ signal from DSP host system.
J2.9/P2.9	FSR	Unused.
J2.11	SDO	Serial data output.
P2.11	SDI	Serial data input.
J2.13/P2.13	DR	Unused.
J2.15/P2.15	$\overline{LDAC1}$	GPIO signal to control $\overline{LDAC}$ for DAC output latch update.
J2.17/P2.17	$\overline{LDAC2}$	Alternate GPIO signal to control $\overline{LDAC}$ for DAC output latch update.
J2.19/P2.19	$\overline{RST}$	GPIO signal to control $\overline{RST}$ for DAC reset function.
J2.2/P2.2	PDN	GPIO signal to control PDN for hardware powerdown.
J2.4/P2.4 J2.10/P2.10 J2.18/P2.18	GND	Signal ground.
J2.6/P2.6 J2.8/P2.8 J2.12/P2.12 J2.14/P2.14 J2.16/P2.16 J2.20/P2.20	GPIOs	Unused.

3.3.1 $\overline{CS}$ or $\overline{FS}$ Signal

The $\overline{CS}$ and $\overline{FS}$ signals of the EVM are interchangeable and the signal used depends on the host controller that is selected to communicate with the DAC8881EVM. Either signal can be chosen to drive the DAC8881 chip select ($\overline{CS}$) pin. The basic function of the $\overline{CS}$ and $\overline{FS}$ signals is to drive the $\overline{CS}$ pin of the DAC8881 to enable the device communication port and to synchronize the data input into the device immediately following its high-to-low transition. This signal must be held low while the host processor is accessing the DAC. The low-to-high transition of this signal transfers the contents of the serial shift register to the DAC input register.

3.3.2 SCLK Signal

The SCLK signal is the clock necessary to load the serial data input into the DAC serial shift register. The serial clock rate can operate at speeds up to 50MHz. The 16-bit data is shifted out of the bus master synchronously on the falling edge of SCLK and latched on the rising edge of SCLK into the DAC serial shift register. The most significant bit (MSB) is the first bit that is output to the DAC. After 16-bits are transferred or 16 SCLK cycles are generated, the bus master takes the $\overline{CS}$ signal high immediately. If the $\overline{CS}$ signal is held low and more than 16 SCLK cycles are applied, the last SCLK cycle is considered the location of the least significant bit (LSB) of the 16-bit word that is loaded into the DAC serial shift register. Hence, the user must know the data word alignment with respect to SCLK or else the data input can become corrupted. If this happens, simply reload the DAC latch with the new 16-bit word.

3.3.3 SDI Signal

The SDI signal is the serial data input that is loaded into the DAC serial shift register with respect to SCLK.

3.3.4 $\overline{\text{LDAC}}$ Signal

The $\overline{\text{LDAC}}$ signal is the control input signal necessary to load the DAC register with the contents of the input register. This signal is active low and can be triggered synchronously or asynchronously.

3.3.5 $\overline{\text{RST}}$ Signal

The $\overline{\text{RST}}$ signal is the control input necessary to reset the device to a known state determined by the state of the RSTSEL pin when the $\overline{\text{RST}}$ pin is asserted. If RSTSEL is tied to DGND, the DAC latch is cleared (0V) and V_{OUT} is minimum scale (i.e., $V_{REF}L$). If RSTSEL is tied to V_{DD}, the DAC latch is set to mid-scale and V_{OUT} is equal to ($V_{REF}H$ – $V_{REF}L$)/2. This pin is active low.

3.3.6 PDN Signal

The PDN signal is the control input provided for the hardware power-down function of the device. This signal is active high, so when the PDN pin is driven high, the device goes into power-down mode, which reduces its power consumption. The DAC8881 voltage output pin is connected to ground through an internal 10kΩ resistor while in power-down mode.

3.4 Analog Output

The DAC8881 voltage output is buffered internally and offers a force and sense output configuration to allow the loop around the output amplifier to be closed as close to the load as possible. The EVM closes this loop by default with R1 installed. So if there is a need to close the loop at the load, R1 must be removed and jumpers W2 and W7 used to connect V_{OUT} and R_{FB} to the connector J4. The selected pins of the J4 connector, as dictated by the jumper positions of the W2 and W7 jumpers, can then be connected to the load to close the loop.

The EVM includes an external operational amplifier, U2, as an option for other output signal conditioning circuitry for the DAC output. Although the buffered output of the DAC8881 can be monitored through J4 pin 2, the optional external buffer output (if the DAC output is connected to it) can be monitored through the TP3 test point.

The external op-amp, U2, is set to the unity gain configuration by default to maintain the DAC8881 unipolar output mode of operation. But it can be modified by simple jumper settings to achieve other modes of operation. The following sections describe the different configurations of the output amplifier, U2.

3.4.1 Bipolar Output Operation

Using the external $V_{REF}H$ to offset the DAC output and extend the range of operation to achieve a bipolar mode of operation is possible by configuring the output op-amp, U2, properly. This configuration is described in Table 4.

Table 4. Bipolar Output Operation Jumper Settings

Reference	Jumper Setting	Function
W9	1-2	Connects DAC output ($V_{OUT}1$) to the non-inverting input of the output op-amp, U2.
	2-3	Connects DAC output ($V_{OUT}2$) to the non-inverting input of the output op-amp, U2.
W3	CLOSE	Connects $V_{REF}H$ to the inverting input of the op-amp, U2.
W5	1-2	Supplies power (V_{SS}) to the negative rail of the op-amp, U2, for a wider range of operation.
W12	OPEN	Disconnects negative input of the op-amp from the gain resistor, R12.

3.4.2 Output Gain of Two Operation

The jumper settings in Table 5 configure the EVM to operate with an output gain of two.

Table 5. Gain of Two Output Jumper Settings

Reference	Jumper Setting	Function
W9	1-2	Connects DAC output ($V_{OUT}1$) to the non-inverting input of the output op-amp, U2.
	2-3	Connects DAC output ($V_{OUT}2$) to the non-inverting input of the output op-amp, U2.
W3	OPEN	Disconnects $V_{REF}H$ to the inverting input of the op-amp, U2.
W5	1-2	Supplies power (V_{SS}) to the negative rail of the op-amp, U2, for a wider range of operation.
W12	CLOSE	Connects the negative input of the op-amp, U2, to the gain resistor, R12.

3.4.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive loads. However, all op-amps under certain conditions may become unstable depending on the op-amp configuration, gain, and load value. These are just few factors that can affect op-amp stability performance and should be considered during implementation.

In unity gain, the OPA627 op-amp, U2, performs very well with very large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive even more capacitance and by adding a load resistor even improves the capacitive load drive capability.

Table 6 shows the jumper setting configuration for a capacitive load drive.

Table 6. Capacitive Load Drive Output Jumper Settings

Reference	Jumper Setting	Function
W9	1-2	Connects DAC output ($V_{OUT}1$) to the non-inverting input of the output op-amp, U2.
	2-3	Connects DAC output ($V_{OUT}2$) to the non-inverting input of the output op-amp, U2.
W3	OPEN	Disconnects $V_{REF}H$ to the inverting input of the op-amp, U2.
W5	1-2	Supplies power (V_{SS}) to the negative rail of the op-amp, U2, for a wider range of operation.
W12	CLOSE	Connects the negative input of the op-amp, U2, to the gain resistor, R12.

3.5 Jumper Settings

Table 7 shows the function of each specific jumper setting of the EVM.

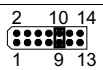
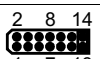
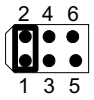
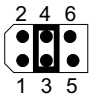
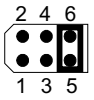
Table 7. Jumper Setting Functions

Reference	Jumper Setting	Function
W1		Routes +5VA for AV_{DD} and DV_{DD} to power the analog and digital supplies of the DAC8881.
		Routes +3.3VA for AV_{DD} and DV_{DD} to power the analog and digital supplies of the DAC8881.
W2		Routes V_{OUT} to J4-2.
		Routes V_{OUT} to J4-6.

Table 7. Jumper Setting Functions (continued)

Reference	Jumper Setting	Function
W3		Connects $V_{REF}H$ to the inverting input of U2 for the DAC8881 bipolar mode of operation.
		Disconnects $V_{REF}H$ from the inverting input of U2 to allow another output mode of configuration.
W4		Routes the reference voltage from J4 pin 18 for the $V_{REF}L$ pin of the DAC8881
		Connects the $V_{REF}L$ pin of the DAC8881 to ground.
W5		Negative supply rail of the output op-amp, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output op-amp, U2, is tied to AGND for unipolar operation.
W6		$\overline{CS}$ signal from J2-1 is routed to drive the $\overline{CS}$ signal of the DAC8881.
		$\overline{FS}$ signal from J2-7 is routed to drive the $\overline{CS}$ signal of the DAC8881.
W7		Routes the reference feedback, R_{FB}, pin of the DAC8881 to J4 pin 4 to provide the option to close the output op-amp, U2, loop as close as possible to the load.
		Leave this jumper open if R1 is installed. This is the default mode of the EVM from the factory.
		Routes the reference feedback, R_{FB}, pin of the DAC8881 to J4 pin 8 to provide the option to close the output op-amp, U2, loop as close as possible to the load.
W8		Routes the on-board +5V voltage reference, $V_{REF}H$, for the DAC.
		Disconnects the on-board or external positive voltage reference, $V_{REF}H$, for the DAC via U5A or J1 pin 20. Allows user reference voltage to connect via TP1.
		Routes the external positive voltage reference, $V_{REF}H$, for the DAC via J1 pin 20.
W9		Routes V_{OUT} and R_{FB} from J4-2 and J4-4 to the non-inverting input of the U2 op-amp.
		Routes V_{OUT} and R_{FB} from J4-6 and J4-8 to the non-inverting input of the U2 op-amp.
W10		$\overline{LDAC1}$ signal from J2-15 is routed to drive the $\overline{LDAC}$ signal of the DAC8881.
		The $\overline{LDAC}$ signal of the DAC8881 is tied to ground for synchronous update of the DAC8881 output.
		$\overline{LDAC2}$ signal from J2-17 is routed to drive the $\overline{LDAC}$ signal of the DAC8881.
W11		Routes V_{CC} to power the analog supply of the U3 reference device.
		Routes +5VA to power the analog supply of the U3 reference device.

Table 7. Jumper Setting Functions (continued)

Reference	Jumper Setting	Function
W12		Connects the inverting input of U2 to the R12 gain resistor for DAC8881 2x gain of operation.
		Disconnects the inverting input of U2 from the R12 gain resistor to allow another output mode of configuration.
J1		If jumper is installed on pins 1 and 2, the $\overline{\text{LDAC}}$ signal of the DAC8881 is tied to ground for synchronous DAC update operation.
		If jumper is installed on pins 3 and 4, the RSTSEL pin of the DAC8881 is tied to ground so the DAC output is at 0V upon power up or a reset to the device is issued.
		If jumper is installed on pins 5 and 6, the GAIN pin of the DAC8881 is tied to IOV_{DD} so that the DAC output is set with a gain of two output.
		If jumper is installed on pins 7 and 8, the USB/$\overline{\text{BTC}}$ pin of the DAC8881 is tied to ground so that the DAC input data format is set for twos complement format.
		If jumper is installed on pins 9 and 10, the $\overline{\text{RST}}$ pin of the DAC8881 is tied to ground so that the DAC is forced into hardware reset mode.
		If jumper is installed on pins 11 and 12, the PDN pin of the DAC8881 is tied to IOV_{DD} so that the DAC is forced into power-down status.
		If jumper is installed on pins 13 and 14, the SDOSEL pin of the DAC8881 is tied to ground so that the DAC device can be operated in daisy-chain mode.
J3		DAC8881 IOV_{DD} is powered with +5VD.
		DAC8881 IOV_{DD} is powered with +1.8VD.
		DAC8881 IOV_{DD} is powered with +3.3VD.
Legend:		Indicates the corresponding pins that are shorted or closed.

3.6 Schematics

The DAC8881 evaluation module schematic appears on the following page.

4 Using the DAC8881EVM with DXP

The DAC8881EVM is compatible with the DAC eXerciser Program (DXP) from Texas Instruments. DXP is a tool that can generate the necessary control signals required to output various signals and waveforms from the DAC8881EVM. The DAC8881EVM-PDK kit combines the DAC8881EVM board with the DSP based modular motherboard MMB0. The kit includes the DXP software for evaluation using any available USB port on a Windows XP based computer.

DXP is a program for controlling the digital input signals such as the clock, LDAC, /CS and SDI. Wave tables are built into the DSP software to allow Sine, Ramp, Triangle, and Square wave signals to be generated by the DAC8881. Straight DC outputs can also be obtained.

The DAC8881EVM-PDK is controlled by loading a DAC EVM configuration into the MMB0. For complete information about installing and configuring DXP, see the *DXP User's Guide* (SBAU146), available for download from the TI web site.

Revision History		
REV	ECN Number	Approved
1	First Proto Release	JLP
A	Production Release	JLP

Do not populate
R5, R7, & R25

J2 Serial Header
J1
P2 Serial Header Bottom
U1 DAC8881
U2 OPA627AU OPA211
U3 REF02AU(8) REF5045ID
U4A U4B OPA2277UA
U5 OPA277
J4 OUTPUT HEADER
J6
J3

EDGE Numbers:

DAC8881EVM BOM = 6489895
DAC8881EVM PWB = 6489896
DAC8881EVM DDB (BLOCK) = 6489897
DAC8881EVM PCA = 6489898
DAC8881EVM KIT (BLOCK) = 6489899

VCC = +15V Analog
AVDD = +2.7V to +5.5V Analog
VSS = 0V to -15V Analog

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title:	DAC8881 EVM		
DOCUMENTCONTROL #	6489897	REV:	A
Engineer: J. PARGUIAN			
Drawn By: J. PARGUIAN			
FILE: DAC8881 Rev A.Sch	DATE: 1-Apr-2008	SIZE:	SHEET: 1 OF: 1

This section covers the specific operation of the DAC8881EVM-PDK. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the DAC8881EVM.

4.1 Hardware

The hardware consists of two main components, the first is the DAC8881EVM itself and the other is a modular motherboard called the MMB0. The MMB0 board houses a TMS320VC5507 DSP which controls the DAC8881 serial interface.

The hardware needs to be configured such that the DAC8881EVM is plugged onto the MMB0 aligning female connectors P4, P2 and P6 (bottom side of the DAC8881EVM) with male connectors J4, J7 and J5 on the MMB0. Please exercise caution when assembling the boards as it is possible to misalign the connectors. DO NOT connect the MMB0 to your PC before installing the DXP software as described in the DXP User's Guide! Installing the software will ensure the necessary drivers are properly loaded to run the hardware.

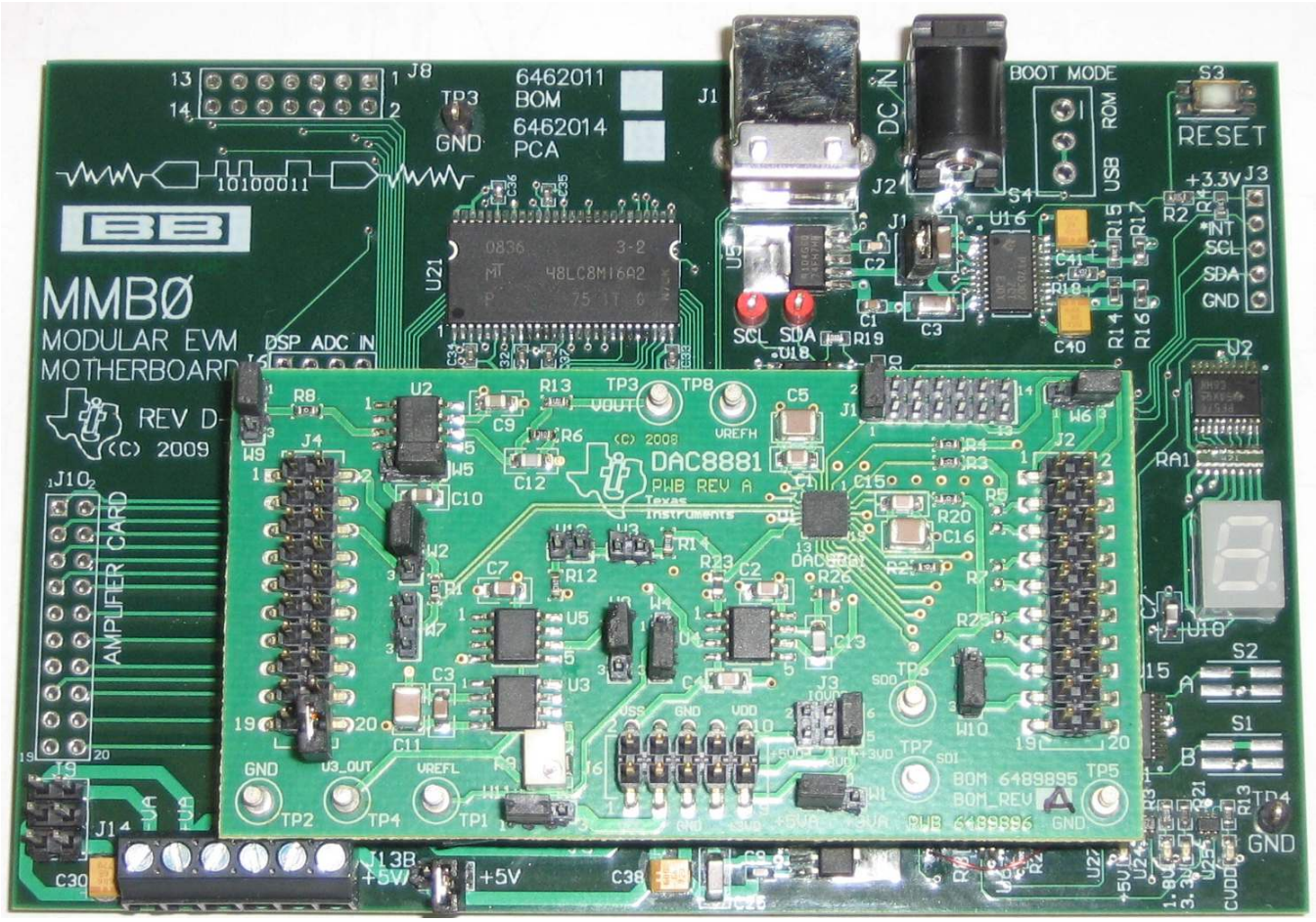


Figure 11. MMB0 with DAC8881EVM Installed

4.2 MMB0 Power Supplies

Several power connections are required for the hardware to work properly. For the MMB0, the supplied 6V AC/DC converter is all that is necessary. Please ensure J12 on the MMB0 board is closed before connecting the AC/DC adapter to the DC In connector of the MMB0. This supply will provide all power to the digital portion of the DAC8881EVM as well as all necessary power for the DSP. Analog power for the DAC8881EVM must be supplied externally via J14 – a 6 position screw terminal mounted in the lower left corner of the MMB0 board.

CAUTION

When using external power supplies applied to J14 on the MMB0, please ensure all shorting blocks from J13 are completely removed. Permanent damage to the MMB0 may occur otherwise.

From left to right, the J14 screw terminal connections are –VA, +VA, +5VA, –5VA, +5VD and GND. The DAC8881 board has power requirements as described in section 1.2 of this manual. The analog power for Vss (–VA) and Vcc (+VA) as well as +5VA may be applied directly to the screw terminals at J14 on the MMB0 (referenced to the GND terminal).

Connect the MMB0 power supply to DC IN connector (J2) on the MMB0. Connect all other analog supplies as necessary to J14 on the MMB0.

4.3 Software – Running DXP

Install DXP on a laptop or personal computer running Windows XP as per the detailed instruction in the DXP Users Guide (TI Document SBAU146). Run the DXP program by clicking on the DXP icon on your desktop, or by browsing to your installation directory.

Before you can generate signals with DXP, a DAC EVM configuration file must be loaded. To load a configuration file, select the desired DAC from the configuration list under the DAC menu. Choose the DAC configuration file for the DAC8881 EVM as shown in Figure 12.

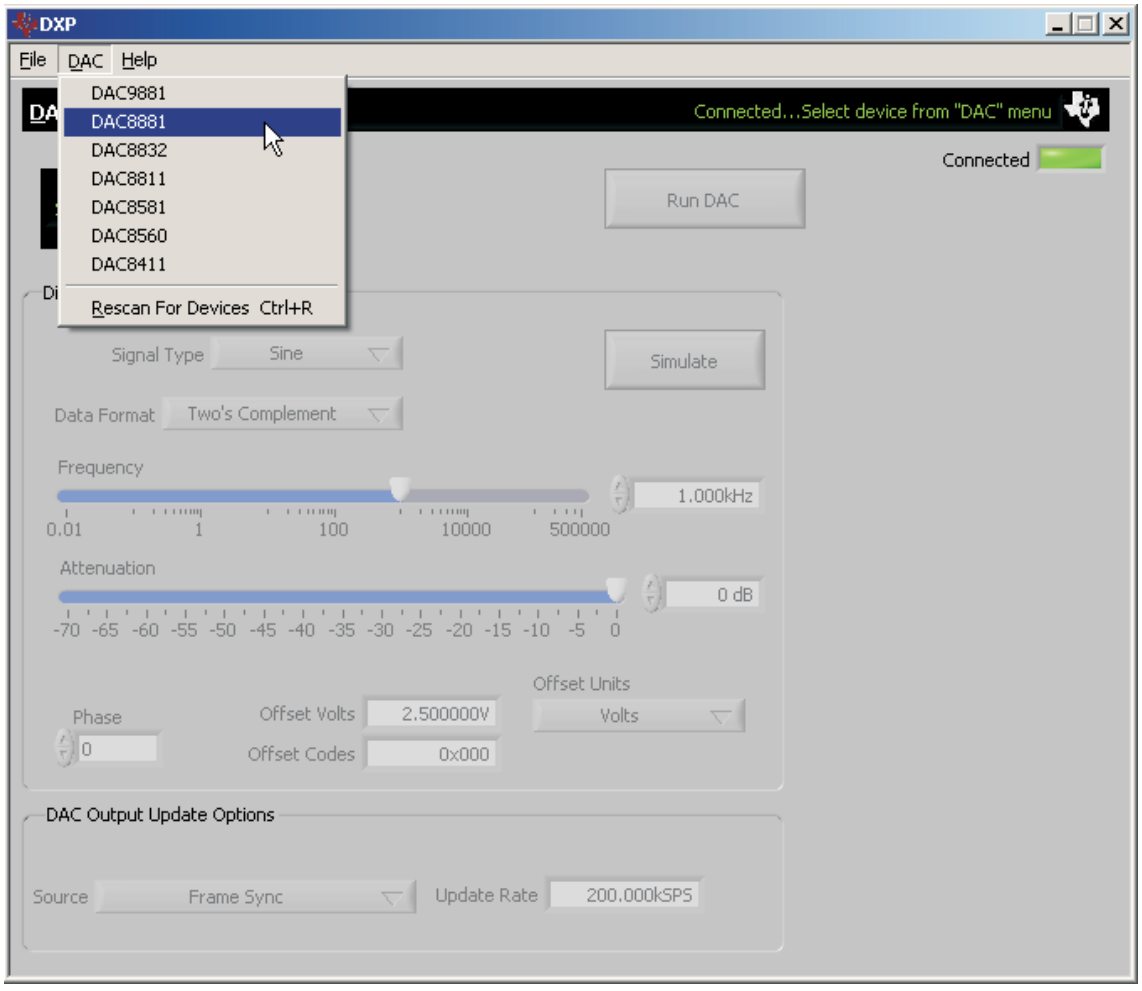


Figure 12. Loading the DAC8881EVM INI file

The DXP software defaults to output a 1 kHz sine wave from the DAC, other waveform options include Square, Saw tooth, Triangle and DC output options as described in the DXP Users Guide. GPIO options are available on the DAC8881EVM which will activate either the RESET or Power down functions of the DAC8881. These are shown below in the right side of the screen labeled GPIO-controlled DAC Functions and described in Table 8.

Table 8. DXP GPIO Controlled DAC Functions

Function	Detailed Description
Reset	Pressing the reset button will cause the button to turn ACTIVE and places logic low on pin 17 of the DAC8881. To use this function, please ensure no jumpers are placed on J1 pins 9-10. When the RST pin is low, the device is in hardware reset mode, and the input register and DAC latch are set to the value defined by the RSTSEL pin (refer to the DAC8881EVM Schematic; J1, pins 3-4). Pressing reset a second time returns the RST function to its inactive state. The device is in normal operating mode, and the input register and DAC output will maintain the reset value until new data are written.
Power Down	Pressing the Power-down button will cause the button to turn ACTIVE and places logic high on pin 18 of the DAC8881. To use this function, please ensure no jumpers are placed on J1 pins 11–12.

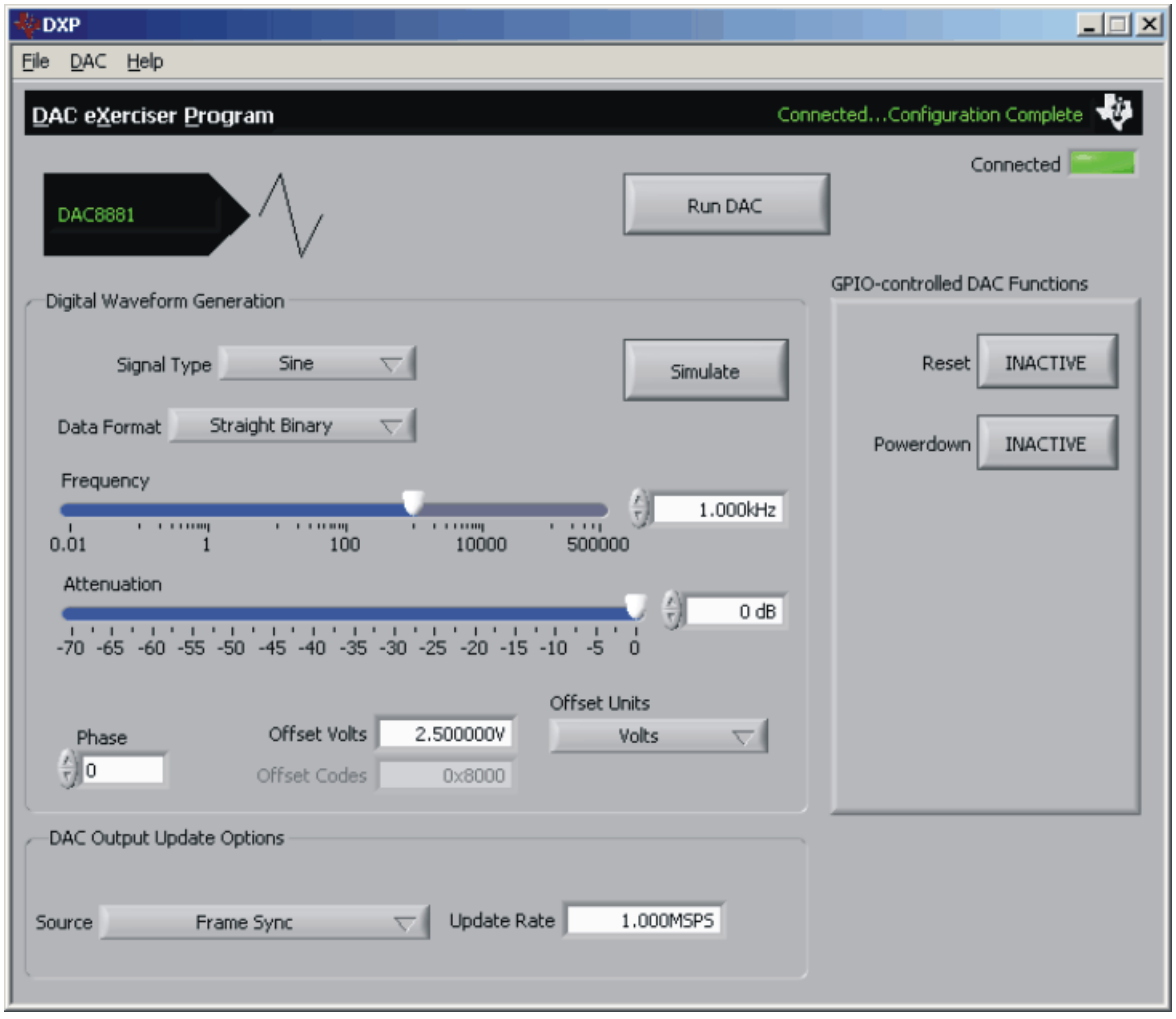


Figure 13. DAC8881 – Frequency/Amplitude and GPIO Control Options

4.4 DAC Output Update Options

The DXP software also allows the user to choose several DAC output update options. These are shown in Figure 14.

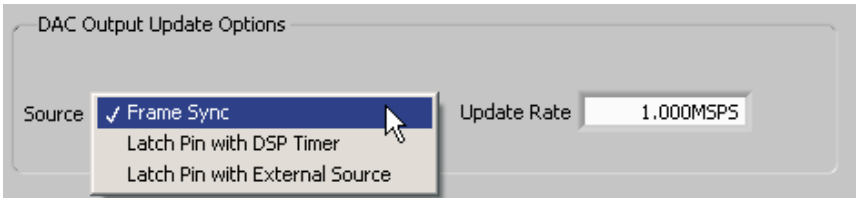


Figure 14. DAC Output Update Options

Details on these options are shown in Table 9.

Table 9. Output Update Features

Options	Detailed Description
Frame Sync	The DXP software defaults to Frame Sync. In this mode, the LDAC pin is held low and the DAC latch is transparent. The DAC output changes to the corresponding level simultaneously when the DAC latch is updated. Place a shunt jumper on J1 covering pins 1-2. W10 should be open.
Latch with DSP Timer	Jumper W10 on the EVM controls LDAC selection. In this configuration, a timer function on the MMB0 applies a pulse to the LDAC pin and the output of the DAC8881 is updated synchronously with the falling edge of the applied pulse. Remove the shunt jumper from J1 pins 1-2 and place it on W10 pins 2-3 to use this feature.
Latch with External Timer	Jumper W10, when moved to pins 1-2, routes the LDAC input to pin 15 of J2. This feature allows the user to apply an LDAC input from an external source. In this mode, J2 pin 15 provides an interrupt to the DSP on the MMB0 which transfers data from the serial interface to the DAC8881. The LDAC input requirements must be in accordance with the Timing Characteristics and voltage level inputs found in the device datasheet.
Update Rate	User Input – enter the desired DAC update rate, 1MSPS is the default.

4.5 Data Input Format

The data input format can be configured for either straight binary or binary two's compliment as shown in Figure 15.

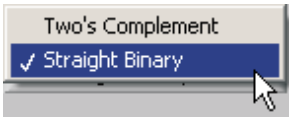


Figure 15. Data Format Options

Options	Detailed Description
Two's Complement	To provide the DAC8881 with two's complement data, the user must install a jumper on J1 pins 7-8. This grounds the USB/BTC input pin of the DAC8881.
Straight Binary	Default state of both DXP and the EVM. In this mode, straight binary data is supplied through the DXP software to the DAC8881. Ensure there is not jumper loaded at J1 pins 7-8 to use this feature.

5 Information

5.1 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center (PIC) at (972) 644–5580. When ordering, identify this manual by its title and literature number. Updated documents also can be obtained through the TI Web site at www.ti.com.

Data Sheets:	Literature Number:
DAC8881	SBAS422
REF02	SBVS003
REF5050	SBOS410
REF5045	SBOS410
OPA211	SBVS058
OPA627	SBOS165
OPA277	SBOS079
OPA2277	SBOS079
OPA227	SBOS110

5.2 Questions About This or Other Data Converter EVMs?

If you have questions about this or other Texas Instruments data converter evaluation modules, send an e-mail to the Data Converter Application Team at dataconvapps@list.ti.com. Include in the subject heading the product with which you have questions or concerns.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2.7 V to 5 V and the output voltage range of -5 V to +5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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