# NCV8612

# Ultra-Low Iq Automotive System Power Supply IC Power Saving Triple-Output Linear Regulator

The NCV8612 is a multiple output linear regulator IC's with an Automatic Switchover (ASO) input voltage selector. The ASO circuit selects between three different input voltage sources to reduce power dissipation and to maintain the output voltage level across varying battery line voltages associated with an automotive environment.

The NCV8612 is specifically designed to address automotive radio systems and instrument cluster power supply requirements. The NCV8612 can be used in combination with the 4−Output Controller/Regulator IC, NCV885x, to form a complete automotive radio or instrument cluster power solution. The NCV8612 is intended to supply power to various "always on" loads such as the CAN transceivers and microcontrollers (core, memory and IO). The NCV8612 has three output voltages, a reset / delay circuit, and a host of control features suitable for the automotive radio and instrument cluster systems.

### Features

- Operating Range 7.0 V to 18.0 V (45 V Load Dump Tolerant)
- Output Voltage Tolerance, All Rails, ±2%
- < 50 μA Quiescent Current
- Independent Input for LDO3 Linear Regulator
- High Voltage Ignition Buffer
- Automatic Switchover Input Voltage Selector
- Independent Input Voltage Monitor with a High Input Voltage and Low Input Voltage (Brown−out) Indicators
- Thermal Warning Indicator with Thermal Shutdown
- Single Reset with Externally Adjustable Delay for the 5 V Rail
- Push−Pull Outputs for Logic Level Control Signals
- All Ceramic Solution for Reduced Leakage Current at the Output
- Enable Input
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- This is a Pb−Free Device

### Applications

- Automotive Radio
- Instrument Cluster

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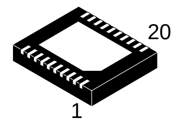



**DFN20**
**MN SUFFIX**
**CASE 505AB**

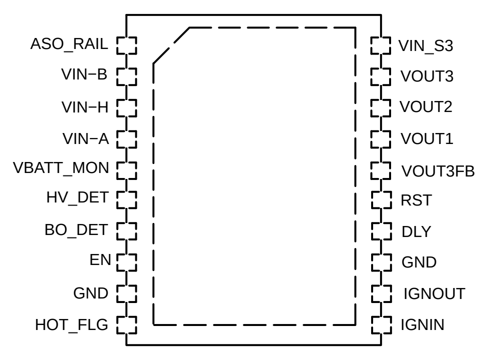
**MARKING DIAGRAM**

NCV8612
AWLYYWW▪
▪

| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

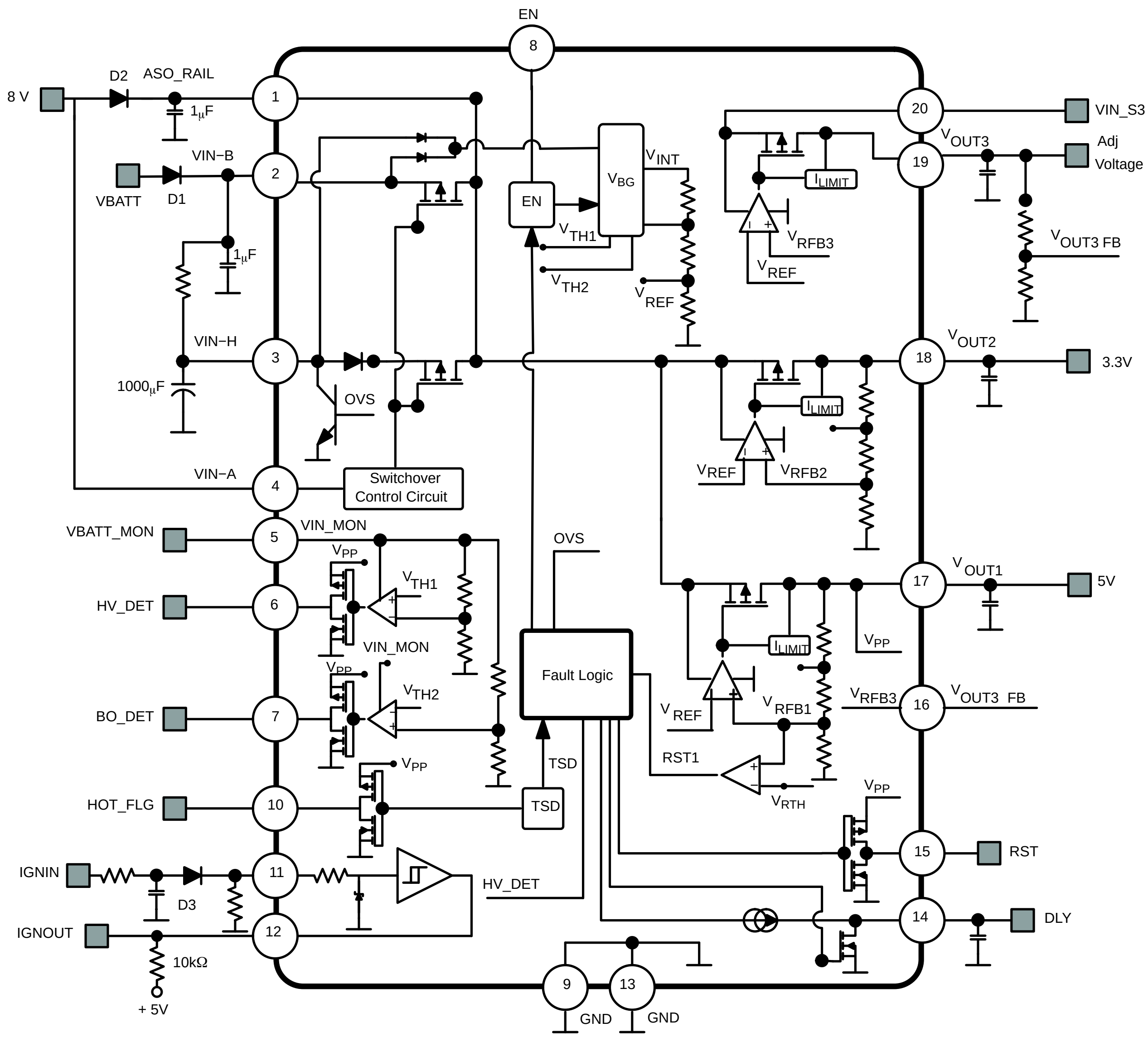
**PIN CONNECTIONS**




**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCV8612MNR2G | DFN20 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.




| Components | Value | Manufacturer |
| --- | --- | --- |
| D1 | MBRS2H100T3G | ON Semiconductor |
| D2 | MBR0502T1 | ON Semiconductor |
| D3 | MMDL914T1 | ON Semiconductor |

**Figure 1. Typical Circuit with the Internal Schematic**

### PIN FUNCTION DESCRIPTIONS

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | ASO_RAIL | Output/Input of the automatic switchover (ASO) circuitry. Place a 1 uF ceramic capacitor on this pin to provide local bypassing to the LDO linear regulator pass devices. |
| 2 | VIN−B | Primary power supply input. Connect battery to this pin through a blocking diode. |
| 3 | VIN−H | Holdup power supply rail. Connect a storage capacitor to this pin to provide a temporary backup rail during loss of battery supply. A bleed resistor (typically 1 kΩ) is needed from VIN−B to this pin in order to trickle charge this capacitor. |
| 4 | VIN−A | Voltage monitor which determines whether the 8 V supply is able to power the outputs. If the 8 V supply is present, the FET’s connected to VIN−B and VIN−H will be turned off, and the 8 V supply will be providing power to the outputs. If the 8 V supply is not present, the FET’s on VIN−B and VIN−H will be left on, and the greater of those voltages will be driving the outputs. |
| 5 | VBATT_MON | VBATT monitor pin. To operate overvoltage shutdown, HV_DET and BO_DET, connect this pin to ASO_RAIL or battery. To eliminate overvoltage shutdown, HV_DET and BO_DET, tie this pin to ground. |
| 6 | HV_DET | High−voltage detect output. When VBATT_MON surpasses 19 V, this pin will be driven to ground. During normal operation, this pin is held at $V_{PP}$. |
| 7 | BO_DET | Brown out indicator output. When VBATT_MON and VIN−A falls below 7.5 V, this pin will be driven to ground. During normal operation, this pin is held at $V_{PP}$. |
| 8 | EN | Enable pin for the LDO linear regulators. Logic high on this pin will enable the LDO linear regulators. Driving this pin to ground will place the IC in a low power shutdown state. |
| 9 | GND | Ground. Reference point for internal signals. Internally connected to pin 13. Ground is *not* connected to the exposed pad of the DFN20 package. |
| 10 | HOT_FLG | Thermal warning indicator. This pin provides an early warning signal of an impending thermal shutdown. |
| 11 | IGNIN | Ignition buffer input |
| 12 | IGOUT | Ignition buffer logic output |
| 13 | GND | Ground. Reference point for internal signals. Internally connected to pin 9. Ground is *not* connected to the exposed pad of the DFN20 package. |
| 14 | DLY | Delay pin. Connect a capacitor to this pin to set the delay time. |
| 15 | RST | Reset pin. Monitors $V_{OUT1}$. |
| 16 | $V_{OUT3}$ FB | Voltage Adjust Input; use an external voltage divider to set the output voltage |
| 17 | $V_{OUT1}$ | 5 V output. Voltage is internally set. |
| 18 | $V_{OUT2}$ | 3.3 V output. Voltage is internally set. |
| 19 | $V_{OUT3}$ | Adjustable voltage output. This voltage is set through an external resistor divider. |
| 20 | VIN_S3 | Supply rail for the standby linear regulator VOUT3. Tie this pin to ASO_RAIL or a separate supply rail. |
| EP | − | Exposed Pad of DFN device. This pad serves as the main path for thermal spreading. The Exposed Pad is **not** connected to IC ground. |

### MAXIMUM RATINGS (Voltages are with respects to GND unless noted otherwise)

| Rating | Symbol | Max | Min | Unit |
|---|---|---|---|---|
| Maximum DC Voltage | VIN−B, VIN−A, ASO_RAIL, VBATT_MON, VIN_S3, EN, IGNIN | 40 | −0.3 | V |
| Peak Transient | VIN−B, VIN−A, ASO_RAIL, VBATT_MON, VIN_S3, EN, IGNIN | 45 | −0.3 | V |
| Maximum DC Voltage | VIN−H | 24 | −0.3 | V |
| Maximum DC Voltage | IGNOUT, $V_{PP}$, HV_DET, BO_DET, HOT_FLG, RST, DLY, $V_{OUT1}$, $V_{OUT2}$ | 7 | −0.3 | V |
| Maximum DC Voltage | $V_{OUT3}$ | 10 | −0.3 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL INFORMATION

| Rating | Symbol | Min | Unit |
|---|---|---|---|
| Thermal Characteristic (Note 1) | $R_{\theta JA}$ | 40 | °C/W |
| Operating Junction Temperature Range | $T_J$ | −40 to 150 | °C |
| Maximum Storage Temperature Range | $T_{STG}$ | −55 to +150 | °C |
| Moisture Sensitivity Level | MSL | 1 | |

1. Values based on measurement of NCV8612 assembled on 2−layer 1−oz Cu thickness PCB with Copper Area of more than 645 $mm^2$ with several thermal vias for improved thermal performance. Refer to CIRCUIT DESCRIPTION section for safe operating area.

### ATTRIBUTES

| Rating | Symbol | Min | Unit |
|---|---|---|---|
| ESD Capability, Human Body Model (Note 2) | $ESD_{HB}$ | 2 | kV |
| ESD Capability, Machine Model (Note 2) | $ESD_{MM}$ | 200 | V |
| ESD Capability, Charged Device Model (Note 2) | $ESD_{CDM}$ | 1 | kV |
| IGNIN ESD Capability, Human Body Model (Note 2) | $ESD_{HB}$_IGNIN | 3 | kV |
| IGNIN ESD Capability, Machine Model (Note 2) | $ESD_{MM}$_IGNIN | 200 | V |
| IGNIN ESD Capability (Note 3) | ESD_IGNIN | 10 | kV |

2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model (HBM) tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model (MM) tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD Charged Device Model (CDM) tested per EIA/JES D22/C101, Field Induced Charge Model
3. Device tested with external 10 kΩ series resistance and 1 nF storage capacitor.

### SUPPLY VOLTAGES AND SYSTEM SPECIFICATION ELECTRICAL CHARACTERISTICS

(7 V < ASO_RAIL < 18 V, VIN−H = VIN−B ≥ ASO_RAIL, $V_{PP}$ = 5 V, VIN_S3 tied to ASO_RAIL, VBATT_MON = 0 V, EN = 5 V, IGNIN = 0 V, $I_{SYS}$ = 3 mA (Note 6)) Minimum/Maximum values are valid for the temperature range −40°C ≤ $T_J$ ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY RAILS** | | | | | | |
| Quiescent Current (Notes 4 and 6) | $i_q$ | $T_J$ = 25°C, $I_{SYS}$ = 70 μA, VIN−A = VIN_S3 = 0 V, VIN−B = 13.2 V | | 34 | 50 | μA |
| Shutdown Current (Note 5) | $i_{SHDN}$ | $T_J$ = 25°C, EN = 0 V, VIN−B = 13.2 V | | | 0.5 | μA |
| Minimum Operating Voltage (VIN−H, VIN−B) | | | 4.5 | | | V |
| **THERMAL MONITORING** | | | | | | |
| Thermal Warning (HOT_FLG) Temperature | $T_{WARN}$ | | 140 | 150 | 160 | °C |
| $T_{WARN}$ Hysteresis | | | 10 | | 20 | °C |
| Thermal Shutdown | | | 160 | 170 | 180 | °C |
| Thermal Shutdown Hysteresis | | | 10 | | 20 | °C |
| Delta Junction Temperature (TSD − $T_{WARN}$) | | | 10 | 20 | 30 | °C |
| HOT_FLG Voltage Low | | $T_J$ < $T_{WARN}$, 10 kΩ Pullup to 5 V | | | 0.4 | V |
| HOT_FLG Voltage High | | $T_J$ > $T_{WARN}$, 10 kΩ Pulldown to GND | $V_{OUT1}$ − 0.5 | | | V |
| **AUTO SWITCHOVER** | | | | | | |
| VIN−A Quiescent Current | | | | 24 | | μA |
| VIN−A to VIN−B Risetime | | $T_J$ = 25°C, $C_{ASO\_RAIL}$ = 1 μF, $I_{SYS}$ = 400 mA | | 200 | | μsec |
| VIN−B to VIN−A Falltime | | $T_J$ = 25 °C, $C_{ASO\_RAIL}$ = 1 μF, $I_{SYS}$ = 400 mA | | 100 | | μsec |
| VIN−A Operating Threshold | | VIN−A Rising | 7.2 | 7.5 | 7.75 | V |

**SUPPLY VOLTAGES AND SYSTEM SPECIFICATION ELECTRICAL CHARACTERISTICS** (continued)
(7 V < ASO_RAIL < 18 V, VIN−H = VIN−B ≥ ASO_RAIL, $V_{PP}$ = 5 V, VIN_S3 tied to ASO_RAIL, VBATT_MON = 0 V, EN = 5 V, IGNIN = 0 V, $I_{SYS}$ = 3 mA (Note 6)) Minimum/Maximum values are valid for the temperature range −40°C ≤ $T_J$ ≤ 150°C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **AUTO SWITCHOVER** | | | | | | |
| VIN−A Operating Hysteresis | | VIN−A Falling | 100 | 175 | 250 | mV |
| Max VIN−B to $V_{ASO\_RAIL}$ Voltage Drop | | $I_{SYS}$ = 400 mA, VIN−B = 7 V | | | 1.5 | V |
| Max VIN−H to $V_{ASO\_RAIL}$ Voltage Drop | | $I_{SYS}$ = 400 mA, VIN−H = 7.5 V | | | 2.0 | V |
| **RESET (RST Pin)** | | | | | | |
| RESET Threshold | | % of $V_{OUT1}$ | 90 | 93 | 96 | % |
| Hysteresis | | % of $V_{OUT1}$ | | | 2.5 | % |
| Reset Voltage High | | 10 kΩ Pulldown to GND | $V_{OUT1}$ − 0.5 | | | V |
| Reset Voltage Low | | 10 kΩ Pullup to 5 V | | | 0.4 | V |
| **DELAY (DLY Pin)** | | | | | | |
| Charge Current | | | 2.4 | 5 | 7 | μA |
| Delay Trip Point Voltage | | | | 2.0 | | V |
| **ENABLE (EN pin)** | | | | | | |
| Bias current (Into Pin) | | $T_J$ = 25°C, EN = 5 V | | 1.6 | 5.0 | μA |
| Logic High | | | 2.0 | | | V |
| Logic Low | | | | | 0.8 | V |
| **IGNITION BUFFER** | | | | | | |
| Schmitt Trigger Rising Threshold | | | 2.75 | 3.25 | 3.75 | V |
| Schmitt Trigger Falling Threshold | | | 0.8 | 1.0 | 1.2 | V |
| IGNOUT Voltage Low | | IGNIN = 5 V, 10 kΩ Pullup to 5 V | | | 0.4 | V |
| IGNOUT Leakage Current | | $T_J$ = 25°C, IGNOUT = 5 V | | 0.1 | 0.5 | μA |
| **VBATT MONITOR** | | | | | | |
| VBATT_MON Quiescent Current | | $T_J$ = 25°C, VBATT_MON = 13.2 V | | 3 | 5 | μA |
| VBATT_MON Shutdown Current | | $T_J$ = 25°C, EN = 0 V, VBATT_MON = 13.2 V | | | 0.5 | μA |
| VBATT_MON Minimum Operating Voltage | | Threshold where BO_DET and HV_DET signals become valid | 1.0 | 2.0 | 2.5 | V |
| VBATT_MON Hysteresis | | | | 0.25 | | V |
| HV_DET Voltage High | | 10 kΩ Pulldown to GND VBATT_MON Tied to ASO_RAIL | $V_{OUT1}$ − 0.5 | | | V |
| HV_DET Voltage Low | | 10 kΩ Pullup to 5 V VBATT_MON Tied to ASO_RAIL | | | 0.4 | V |
| HV_DET Threshold | | VBATT_MON Rising | 18 | | 20 | V |
| HV_DET Hysteresis | | VBATT_MON Falling | 0.2 | 0.35 | 0.5 | V |
| BO_DET Voltage High | | 10 kΩ Pulldown to GND VBATT_MON Tied to ASO_RAIL | $V_{OUT1}$ − 0.5 | | | V |
| BO_DET Voltage Low | | 10 kΩ Pullup to 5 V VBATT_MON Tied to ASO_RAIL | | | 0.4 | V |
| BO_DET Threshold | | VBATT_MON Falling | 7 | 7.5 | 8 | V |
| BO_DET Hysteresis | | VBATT_MON Rising | 0.2 | 0.35 | 0.5 | V |

4. $i_q$ is equal to $I_{VIN-B} + I_{VIN-H} - I_{SYS}$
5. $I_{SHDN}$ is equal to $I_{VIN-B} + I_{VIN-H}$
6. $I_{SYS}$ is equal to $I_{OUT1} + I_{OUT2} + I_{OUT3}$

**ELECTRICAL CHARACTERISTICS**
(7 V < ASO_RAIL < 18 V, VIN−H = VIN−B ≥ ASO_RAIL, $V_{PP}$ = 5 V, VIN_S3 tied to ASO_RAIL, VBATT_MON = 0 V, EN = 5 V, IGNIN = 0 V, $I_{SYS}$ = 3 mA (Note 6)) Min/Max values are valid for the temperature range −40°C ≤ $T_J$ ≤ 150 °C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LOW DROP−OUT LINEAR REGULATOR 1 (LDO1) SPECIFICATION** | | | | | | |
| Output Voltage | | $I_{OUT1}$ = 0 mA to 120 mA, 7 V < ASO_RAIL < 18 V | 4.9 | 5 | 5.1 | V |
| Dropout (ASO_RAIL − $V_{OUT1}$) | $V_{DR1}$ | $I_{OUT1}$ = 120 mA (Note 7) | | | 500 | mV |
| Load Regulation | | $I_{OUT1}$ = 0 mA to 120 mA, VIN_B = 13.2 V | | 0 | 75 | μV/mA |
| Line Regulation | | $I_{OUT1}$ = 1 mA, 7 V < ASO_RAIL < 18 V | | 0 | 2 | mV/V |
| Output Current Limit | | | 180 | | | mA |
| Output Load Capacitance Range | Co | Output Capacitance for Stability | 1.0 | | 100 | μF |
| Output Load Capacitance ESR Range (Notes 8 and 9) | ESRCo | Cap ESR for Stability | 0.01 | | 13 | Ω |
| $\Delta V_{OUT1}$ (ASO Low to High Transient) | | $T_J$ = 25 °C , $I_{OUT1}$ = 100 mA, $I_{SYS}$ = 400 mA, $C_{ASO\_RAIL}$ = 1 μF, $ESR_{Co}$ = 0.01 Ω, Co = 10 μF, VIN−A falling | | 70 | 100 | ± mV |
| $\Delta V_{OUT1}$ (ASO high to Low Transient) | | $T_J$ = 25 °C , $I_{OUT1}$ = 100 mA, $I_{SYS}$ = 400 mA, $C_{ASO\_RAIL}$ = 1 μF, $ESR_{Co}$ = 0.01 Ω, Co = 10 μF, VIN−A rising | | 70 | 100 | ± mV |
| Power Supply Ripple Rejection (Note 8) | PSRR | VIN_B = 13.2 V, 0.5 $V_{PP}$, 100 Hz | | 60 | | dB |
| Startup Overshoot | | $I_{OUT1}$ = 0 mA to 100 mA | | | 3 | % |
| **LOW DROP−OUT LINEAR REGULATOR 2 (LDO2) SPECIFICATION** | | | | | | |
| Output Voltage | | $I_{OUT2}$ = 0 mA to 80 mA, 7 V < ASO_RAIL < 18 V | 3.234 | 3.3 | 3.366 | V |
| Dropout (ASO_RAIL − $V_{OUT2}$) | $V_{DR2}$ | $I_{OUT2}$ = 80 mA (Note 7) | | | 1.0 | V |
| Load Regulation | | $I_{OUT2}$ = 0 mA to 80 mA, VIN_B = 13.2 V | | 0 | 66 | μV/mA |
| Line Regulation | | $I_{OUT2}$ = 1 mA, 7 V < ASO_RAIL < 18 V | | 0 | 1.2 | mV/V |
| Output Current Limit | | | 120 | | | mA |
| Output Load Capacitance Range | Co | Output Capacitance for Stability | 1.0 | | 100 | μF |
| Output Load Capacitance ESR Range (Notes 8 and 9) | ESRCo | Maximum Cap ESR for stability | 0.01 | | 10 | Ω |
| $\Delta V_{OUT2}$ (ASO Low to High Transient) | | $T_J$ = 25 °C , $I_{OUT2}$ = 80 mA, $I_{SYS}$ = 400 mA, $C_{ASO\_RAIL}$ = 1 μF, $ESR_{Co}$ = 0.01 Ω, Co = 22 μF, VIN−A falling | | 30 | 66 | ± mV |
| $\Delta V_{OUT2}$ (ASO high to Low Transient) | | $T_J$ = 25 °C , $I_{OUT2}$ = 80 mA, $I_{SYS}$ = 400 mA, $C_{ASO\_RAIL}$ = 1 μF, $ESR_{Co}$ = 0.01 Ω, Co = 22 μF, VIN−A rising | | 30 | 66 | ± mV |
| Power Supply Ripple Rejection (Note 8) | PSRR | VIN_B = 13.2 V, 0.5 $V_{PP}$, 100 Hz | | 60 | | dB |
| Startup Overshoot | | $I_{OUT2}$ = 0 mA to 80 mA | | | 3 | % |
| **LOW DROP−OUT LINEAR REGULATOR 3 (LDO3) SPECIFICATION** | | | | | | |
| Output Voltage | $V_{OUT3}$ | $I_{OUT3}$ = 0 mA to 400 mA, $V_{OUT3}$ + $V_{DR3}$ ≤ VIN_S3 ≤ 18 V | −2% | − | +2% | V |
| Dropout (VIN_S3 − $V_{OUT3}$) | $V_{DR3}$ | $I_{OUT3}$ = 400 mA , $V_{OUT3}$ = 5 V (Notes 7 and 10) | | | 2.5 | V |
| Output Current Limit | | | 500 | | | mA |
| Load Regulation | | $I_{OUT3}$ = 0 mA to 400 mA, VIN_B = 13.2 V | | 0 | 75 | μV/mA |
| Line Regulation | | $I_{OUT3}$ = 1 mA, $V_{REF}$ ≤ VIN_S3 ≤ 18 V | | 0 | 654 | μV /V |
| Output Load Capacitance Range | Co | Output Capacitance for Stability | 1.0 | | 100 | μF |

**ELECTRICAL CHARACTERISTICS** (continued)
(7 V < ASO_RAIL < 18 V, VIN−H = VIN−B ≥ ASO_RAIL, $V_{PP}$ = 5 V, VIN_S3 tied to ASO_RAIL, VBATT_MON = 0 V, EN = 5 V, IGNIN = 0 V, $I_{SYS}$ = 3 mA (Note 6)) Min/Max values are valid for the temperature range −40°C ≤ $T_J$ ≤ 150 °C unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LOW DROP−OUT LINEAR REGULATOR 3 (LDO3) SPECIFICATION** | | | | | | |
| Output Load Capacitance ESR Range (Notes 8 and 9) | ESRCo | Maximum Capacitance ESR for stability | 0.01 | | 12 | Ω |
| $\Delta V_{OUT3}$ (ASO Low to High Transient) | | $T_J$ = 25 °C , $I_{OUT3}$ = 400 mA, $I_{SYS}$ = 400 mA, $C_{ASO\_RAIL}$ = 1 μF, $ESR_{Co}$ = 0.01 Ω, Co = 47 μF, VIN−A falling | | 15 | 36 | ± mV |
| $\Delta V_{OUT3}$ (ASO high to Low Transient) | | $T_J$ = 25 °C , $I_{OUT3}$ = 400 mA, $I_{SYS}$ = 400 mA, $C_{ASO\_RAIL}$ = 1 μF, $ESR_{Co}$ = 0.01 Ω, Co = 47 μF, VIN−A rising | | 15 | 36 | ± mV |
| Power Supply Ripple Rejection (Note 8) | PSRR | VIN_B = 13.2 V, 0.5 $V_{PP}$, 100 Hz | | 60 | | dB |
| Startup Overshoot | | $I_{OUT3}$ = 0 mA to 400 mA | | | 3 | % |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Dropout voltage is measured when the output voltage has dropped 100 mV relative to the nominal value obtained with ASO_RAIL = VIN_S3 = 13.2 V.
8. Not tested in production. Limits are guaranteed by design.
9. Refer to CIRCUIT DESCRIPTION Section for Stability Consideration
10. For other voltage versions refer to Typical Performance Characteristics Section.

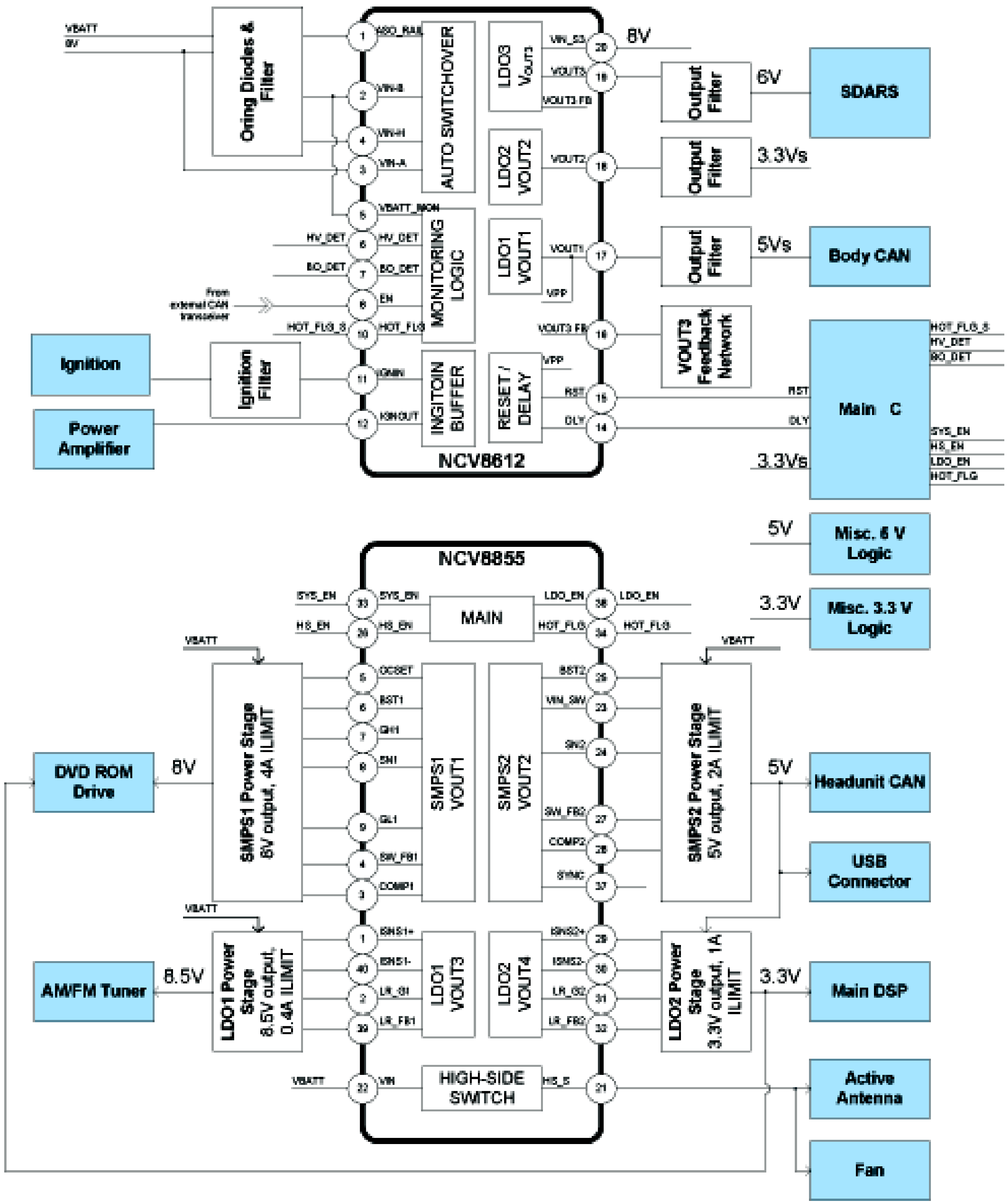


Figure 2. Automotive Radio System Block Diagram Example NCV8612 with NCV8855

## CIRCUIT DESCRIPTION

### Auto Switchover Circuitry

The auto switchover circuit is designed to insure continuous operation of the device, automatically switching the input voltage from the ASO_RAIL input, to the VIN−B input, to the VIN−H input depending on conditions. The primary input voltage pin is ASO_RAIL, which is driven from the 8 V supply. When this voltage is present it will drive the output voltages. Regardless of whether the 8 V supply is available, the reference and core functions of the device will be driven by the higher of VIN−B and VIN−H. The switchover control circuitry will be powered solely by the 8 V supply, via VIN−A.

When the 8 V supply is not present, the gates of the 2 P−FET switches will be pulled to ground, turning the switches on. In this condition, the VIN−B and VIN−H voltages will be diode or'ed, with the higher voltage powering the chip. The VIN−H voltage will be one diode lower than the VIN−B voltage, thereby forcing the VIN−B voltage to be dominant supply.

In the event that both the 8 V supply and the VIN−B supply are not present, the VIN−H supply will be powering the device. The VIN−H supply is then fed from a recommended 1000 μF cap. The duration of VIN−H supply is dependent on output current. It is intended as protection against temporary loss of battery conditions.

In the event of a double battery, or prolonged high voltage condition on the battery line, a bleed transistor has been included on the VIN−H line. With the large hold−up cap on VIN−H, the voltage on that pin has the potential to remain in an elevated position for an extended period of time. The main result of this condition would be an Overvoltage Shutdown of the device. In order to avoid this condition, a transistor that is connected to the Overvoltage Shutdown signal is tied to the VIN−H line. This transistor will become active in a high voltage event, allowing the hold−up cap to discharge the excess voltage in a timely manner.

In the Block Diagram, Figure 1, $C_{ASO\_RAIL}$ is listed as a 1 μF capacitor. It is required for proper operation of the device that $C_{ASO\_RAIL}$ is no larger than 1 μF.

During a switchover event, a timer in the output stages prepares the regulator in anticipation of change in input voltage. The event results in a hitch in the output waveforms, as can be seen in Figure 3.

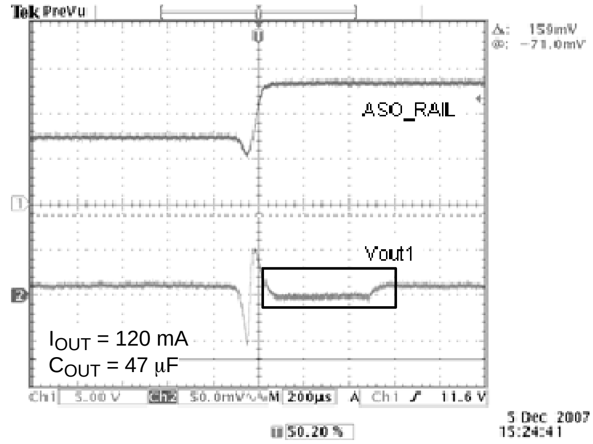



**Figure 3. $V_{OUTX}$ Response to ASO Switchover Event**

### VIN−B/VIN−H Minimum Operating Voltage

The internal reference and core functions are powered by either the VIN−B or VIN−H supply. The higher of the two voltages will dominate and power the reference. This provides quick circuit response on start−up, as well as a stable reference voltage. Since the VIN−B voltage will come up much more quickly than the VIN−H voltage, initially, the VIN−B voltage will be running the reference. In the case of any transient drops on VIN−B, the VIN−H supply, with its large hold−up capacitor, will then be the dominant voltage, and will be powering the reference.

For proper operation of the device, VIN−B or VIN−H must be at least 4.5 V. Below that voltage the reference will not operate properly, leading to incorrect functioning by the device. VIN−B or VIN−H must be greater than 4.5 V regardless of the voltage on the VIN−A pin.

### Enable Function

The NCV8612 is equipped with an Enable input. By keeping the Enable voltage below 0.8 V, the three outputs will be held low. By increasing the Enable pin voltage above 2.0 V, the three outputs will be enabled to their regulated output voltage.

### Internal Soft−Start

The NCV8612 is equipped with an internal soft−start function. This function is included to limit inrush currents and overshoot of output voltages. The soft−start function applies to all 3 regulators.

The soft−start function kicks in for start up, start up via enable, start up after thermal shutdown, and startup after an over voltage condition.

LDO3 is not subject to soft−start under all conditions. The LDO3 output is not affected by overvoltage shutdown, and therefore is not effected by the soft−start function upon the device's return from an over voltage condition. Also, when VIN_S3 is connected to an independent supply and the supply is made available after the soft−start function, LDO3 will not have an independent soft−start.

### LDO1 Regulator

The LDO1 error amplifier compares the reference voltage to a sample of the output voltage ($V_{OUT1}$) and drives the gate of an internal PFET. The reference is a bandgap design to give it a temperature−stable output.

### LDO2 Regulator

The LDO2 error amplifier compares the reference voltage to a sample of the output voltage ($V_{OUT2}$) and drives the gate of an internal PFET. The reference is a bandgap design to give it a temperature−stable output.

### LDO3 Regulator

The LDO3 error amplifier compares the reference voltage to a sample of the output voltage ($V_{OUT3}$) and drives the gate of an internal PFET. The reference is a bandgap design to give it a temperature−stable output

LDO3 is an adjustable voltage output. The adjustable voltage option requires an external resistor divider feedback network. LDO3 can be adjusted up to 10 V. The internal reference voltage is 0.996 V. To determine the proper feedback resistors, the following formula can be used:

$V_{OUT3} = V_{OUT3}FB\ [(R1+R2)/R2]$

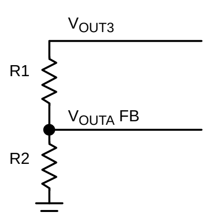



**Figure 4. Feedback Network**

### Stability Considerations

The output or compensation capacitors, $C_{OUTX}$ help determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor values and type should be based on cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for each output capacitor $C_{OUTX}$ shown in Figures 22 − 27 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at the following values:

$C_{OUT1} \geq 47\ \mu F$, $ESR \leq 10\ \Omega$
$C_{OUT2} \geq 47\ \mu F$, $ESR \leq 10\ \Omega$
$C_{OUT3} \geq 47\ \mu F$, $ESR \leq 10\ \Omega$

Actual limits are shown in graphs in the Typical Performance Characteristics section.

### Thermal

As power in the NCV8612 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8612 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications.

The maximum dissipation the NCV8612 can handle is given by:

$P_{D(max)} = (T_{J(max)} - T_A)/R_{thJA}$

See Figure 20 for $R_{thJA}$ versus PCB Area.

$R_{thJA}$ could be further decreased by using Multilayer PCB and/or if Air Flow is taken into account.

### IGNOUT Circuitry

The IGNOUT pin is an open drain output Schmitt Trigger, externally pulled up to 5 V via a 10 kΩ resistor. The IGNOUT pin can be used to monitor the ignition signal of the vehicle, and send a signal to mute an audio amplifier during engine crank. The IGNIN pin is ESD protected, and can handle peak transients up to 45 V. An external diode is recommended to protect against negative voltage spikes.

The IGNOUT circuitry requires the device to be enabled for proper operation.

### $V_{PP}$ Function

The reset and warning circuits utilize a push−pull output stage. The high signal is provided by $V_{PP}$. $V_{PP}$ is tied internally to LDO1. Under this setup, and any setup where LDO's 1−3 are tied to $V_{PP}$, loss of the $V_{PP}$ signal can occur if the pull up voltage is reduced due to over current, thermal shutdown, or overvoltage conditions.

### Reset Outputs

The Reset Output is used as the power on indicator to the Microcontroller. The NCV8612 Reset circuitry monitors the output on LDO1.

This signal indicates when the output voltage is suitable for reliable operation. It pulls low when the output is not considered to be suitable. The Reset circuitry utilizes a push pull output stage, with $V_{PP}$ as the high signal. In the event of the part shutting down via Battery voltage or Enable, the Reset output will be pulled to ground.

The input and output conditions that control the Reset Output and the relative timing are illustrated in Figure 5, Reset Timing. Output voltage regulation must be maintained for the delay time before the reset output signals a valid condition. The delay for the reset output is defined as the amount of time it takes the timing capacitor on the delay pin to charge from a residual voltage of 0 V to the Delay timing threshold voltage $V_D$ of 2 V. The charging current for this is $I_D$ of 5 μA. By using typical IC parameters with a 10 nF capacitor on the Delay Pin, the following time delay is derived:

$t_{RD} = C_D * V_{DU} / I_D$

$t_{RD}$ = 10 nF * (2 V)/ (5 μA) = 4 ms

Other time delays can be obtained by changing the $C_D$ capacitor value. The Delay Time can be reduced by decreasing the capacitance of $C_D$. Using the formula above, delay can be reduced as desired. Leaving the Delay Pin open is not desirable as it can result in unwanted signals being coupled onto the pin.

### VBATT_MON and Warning Flags

The NCV8612 is equipped with High Voltage Detection, Brown Out Detection, and High Temperature Detection circuitry. The Overvoltage Shutdown, High Voltage, and Brown Out Detection circuitry are all run off the VBATT_MON input. If this functionality is not desired, grounding of the VBATT_MON pin will turn off the functions.

The HV_DET and BO_DET signals are in a high impedance state until the VBATT_MON circuitry reaches it minimum operating voltage, typically 1.0 V to 2.5 V. At that point the BO_DET signal will be held low, while the HV_DET signal will go high. The BO_DET signal will go high once the VBATT_MON signal reaches the Brown Out Threshold, typically 7 V to 8 V. The BO_DET signal will stay high until the VBATT_MON voltage drops below the Brown Out Threshold. The HV_DET signal will stay high until the VBATT_MON voltage rises above the HV_DET threshold, typically 18 V to 20 V. The HV_DET signal will reassert high once the HV_DET signal crosses the HV_DET threshold going low.

The NCV8612 is also equipped with a Hot Flag pin which indicates when the junction temperature is approaching thermal shutdown. The Hot Flag signal will remain high as long as the junction temperature is below the Hot flag threshold, typically 140°C to 160°C. This pin is intended as a warning that the junction temperature is approaching the Thermal Shutdown threshold, which is typically 160°C to 180°C. The Hot Flag signal will remain low until the junction temperature drops below the Hot Flag threshold.

The Hot_Flag circuitry does not run off the VBATT_MON Pin, and can not be disabled by grounding VBATT_MON.

Each of the three warning circuits utilizes a push−pull output stage. The high signal is provided by $V_{PP}$. $V_{PP}$ is internally tied to $V_{OUT1}$

### Overvoltage Shutdown

The NCV8612 is equipped with overvoltage shutdown (OVS) functionality. The OVS is designed to turn on when the VBATT_MON signal crosses 19 V. If the VBATT_MON pin is tied to ground, the OVS functionality will be disabled.

When OVS is triggered, LDO1 and LDO2 will both be shut down. LDO3 is run off a separate input voltage line, VIN_S3, and will not shutdown in this condition. Once the OVS condition has passed, LDO1 and LDO2 will both turn back on.

The VIN−H line is equipped with a bleed transistor to prevent a continued OVS condition on the chip once the high battery condition has subsided. This transistor is needed to discharge the high voltage from the VIN−H hold−up capacitor. This transistor will only turn on when an OVS is detected on−chip, and will turn off as soon as the OVS condition is no longer detected by the chip.

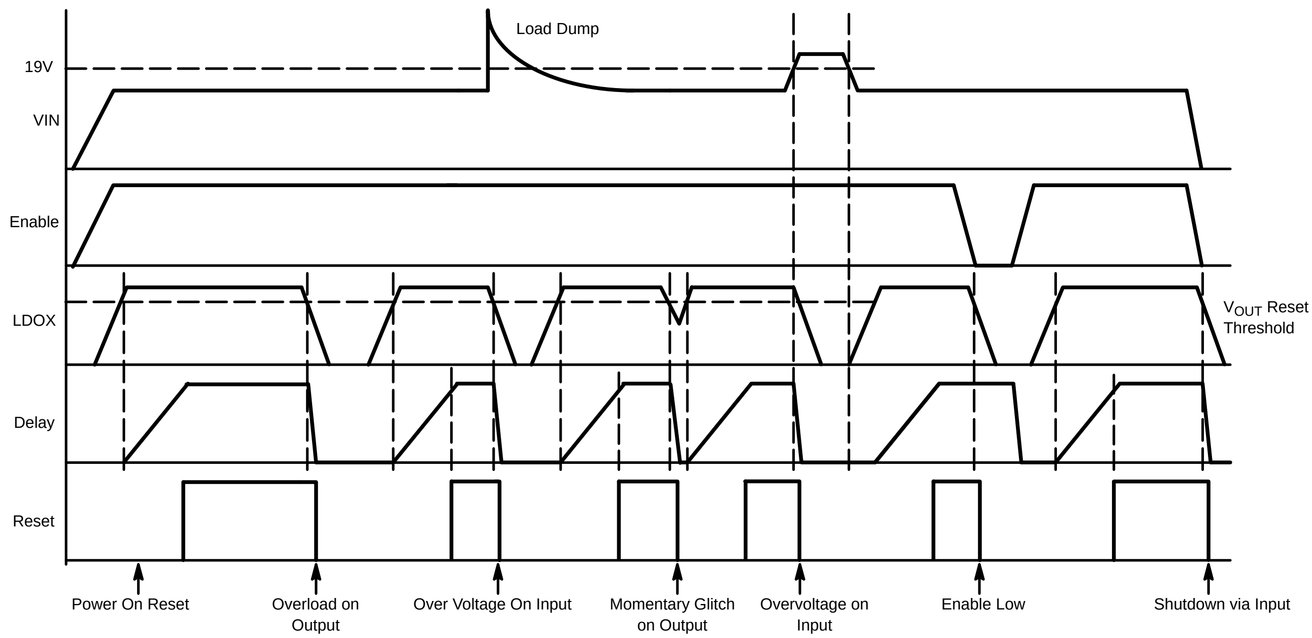



**Figure 5. NCV8612 Reset Timing Diagram**

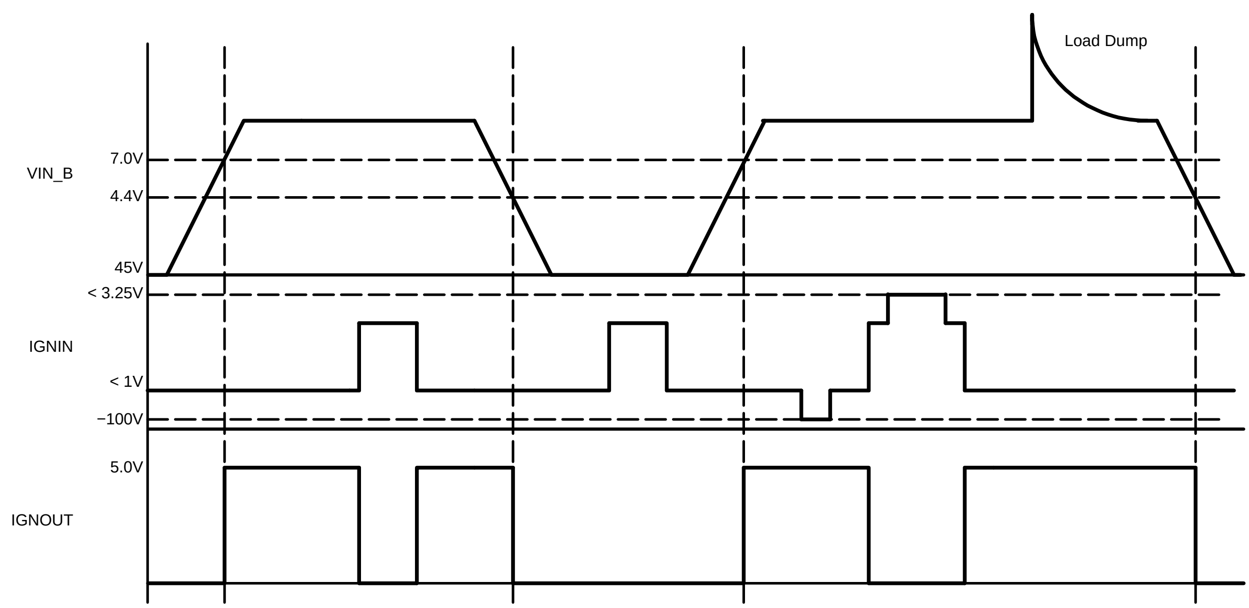



**Figure 6. IGNOUT Timing Diagram**

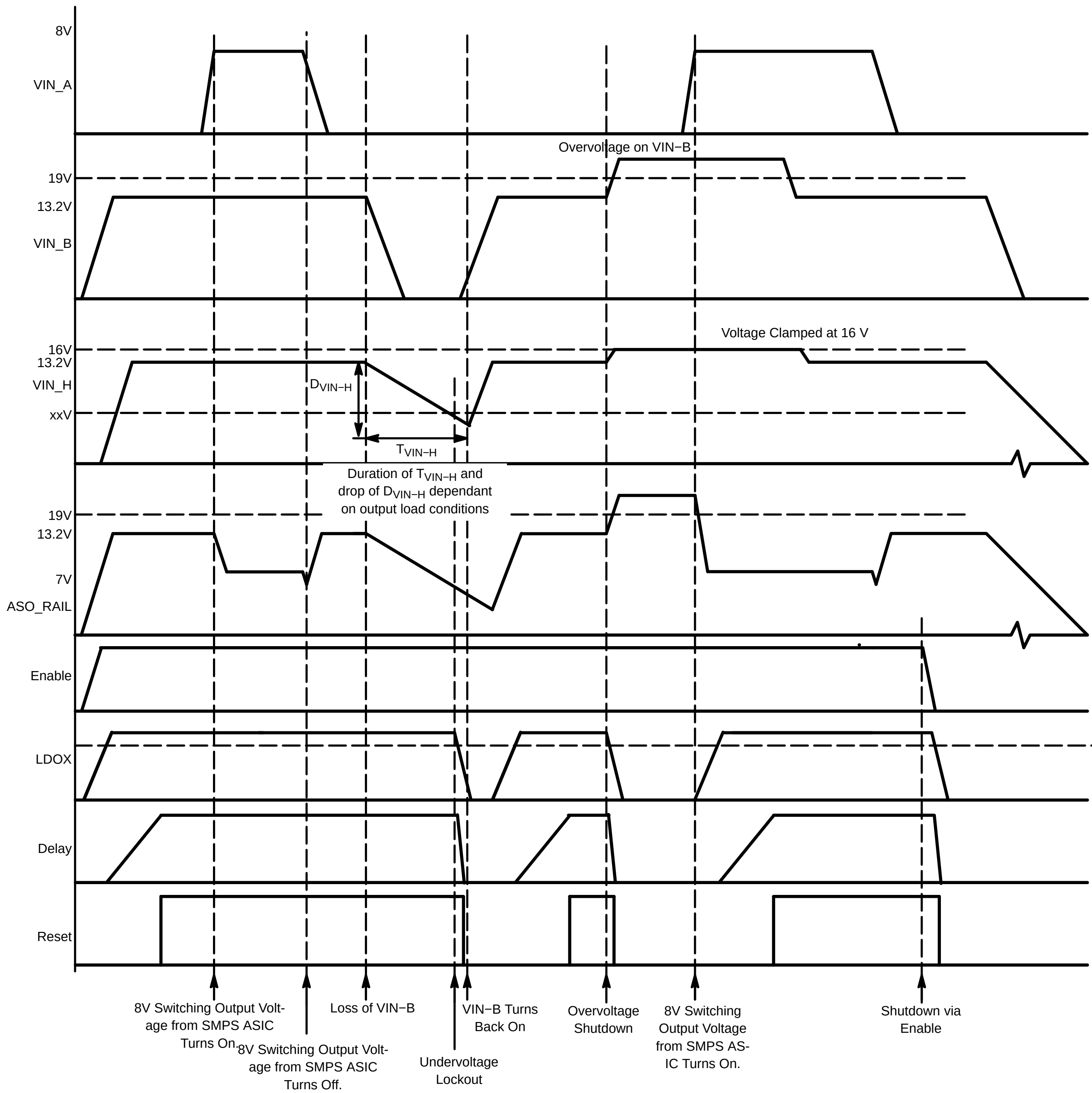



**Figure 7. Auto Switchover Circuit Timing Diagram VBATTMON Connected to ASO_RAIL**

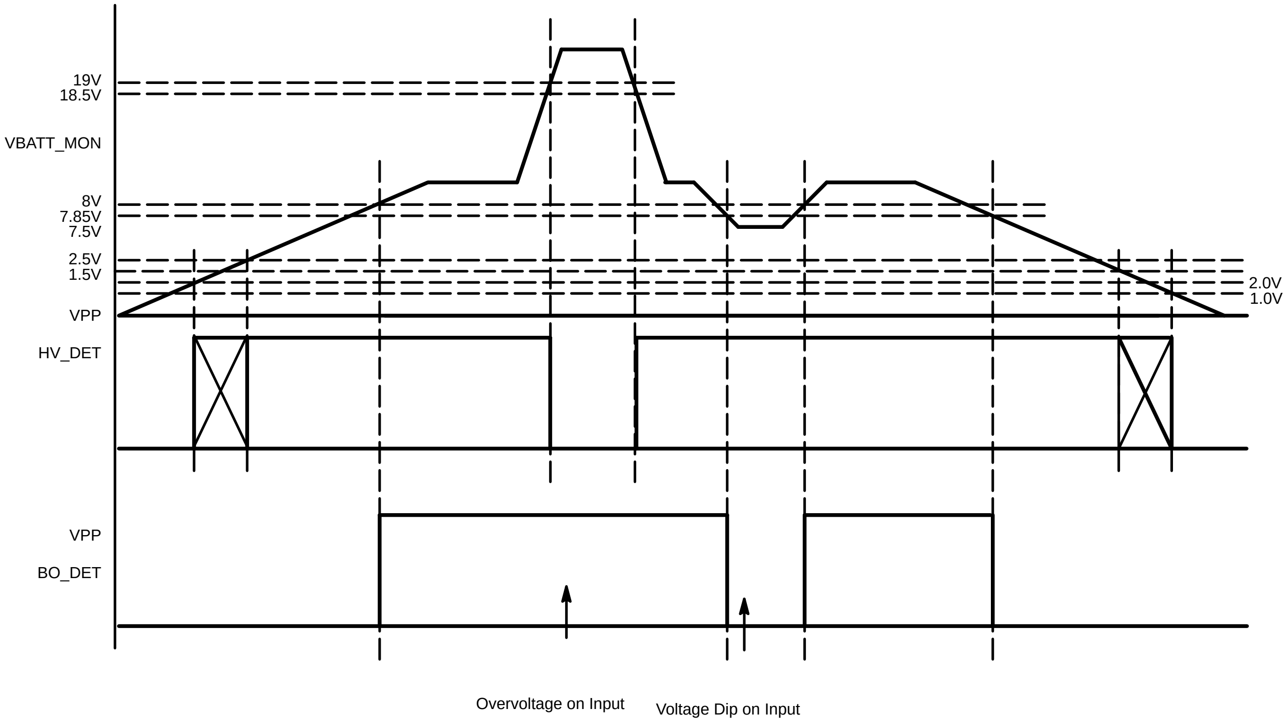



**Figure 8. Warning Circuitry Timing Diagram**

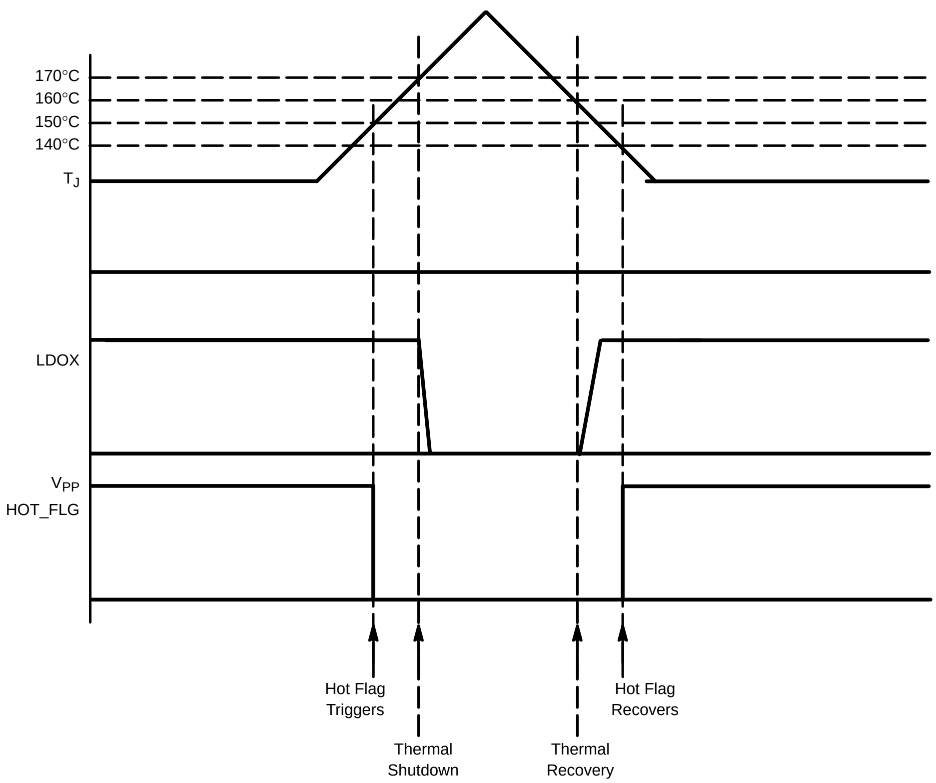



**Figure 9. Thermal Shutdown Timing Diagram**

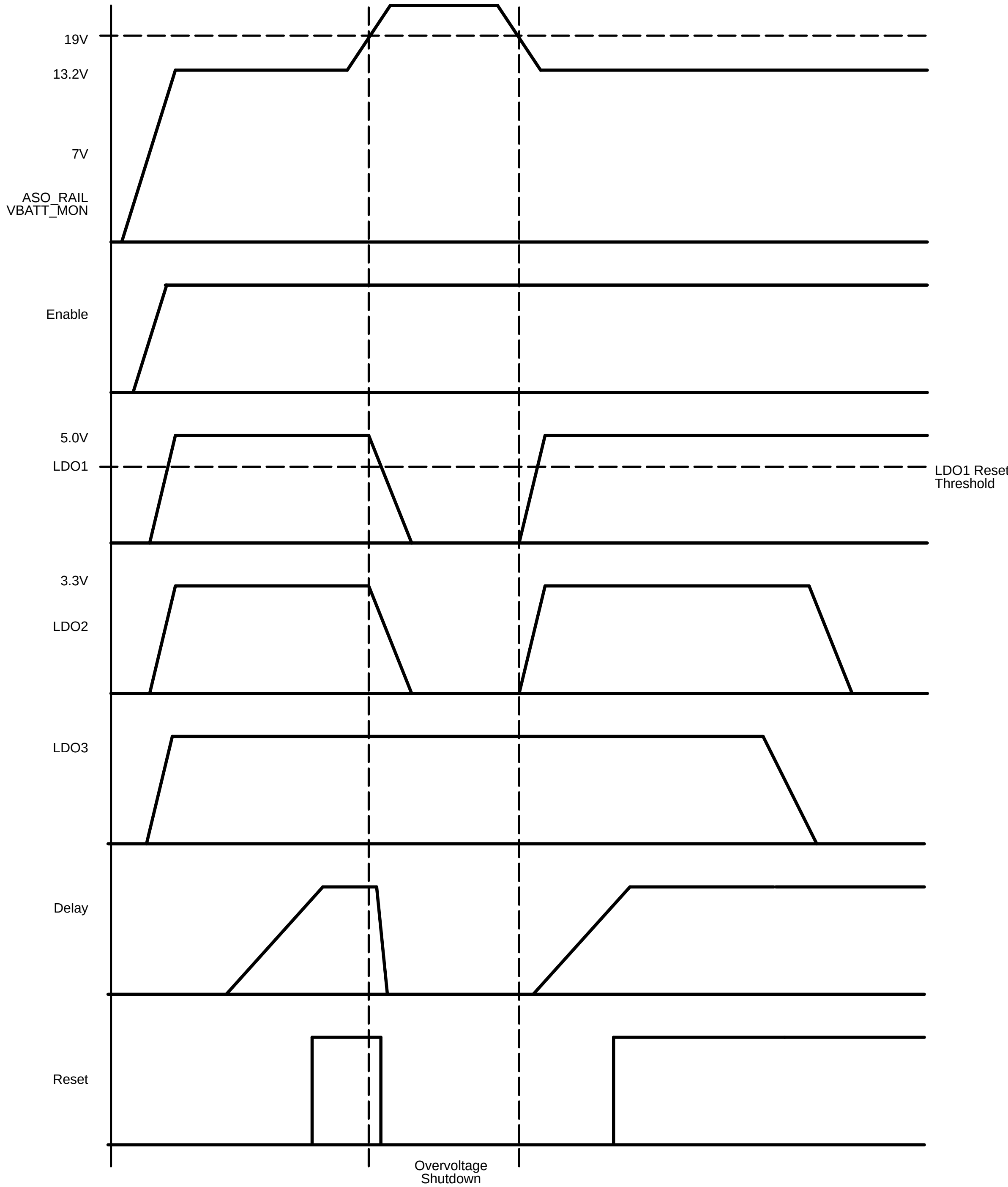



**Figure 10. NCV8612 Regulator Output Timing Diagram– VIN_S3 Tied to ASO_RAIL**

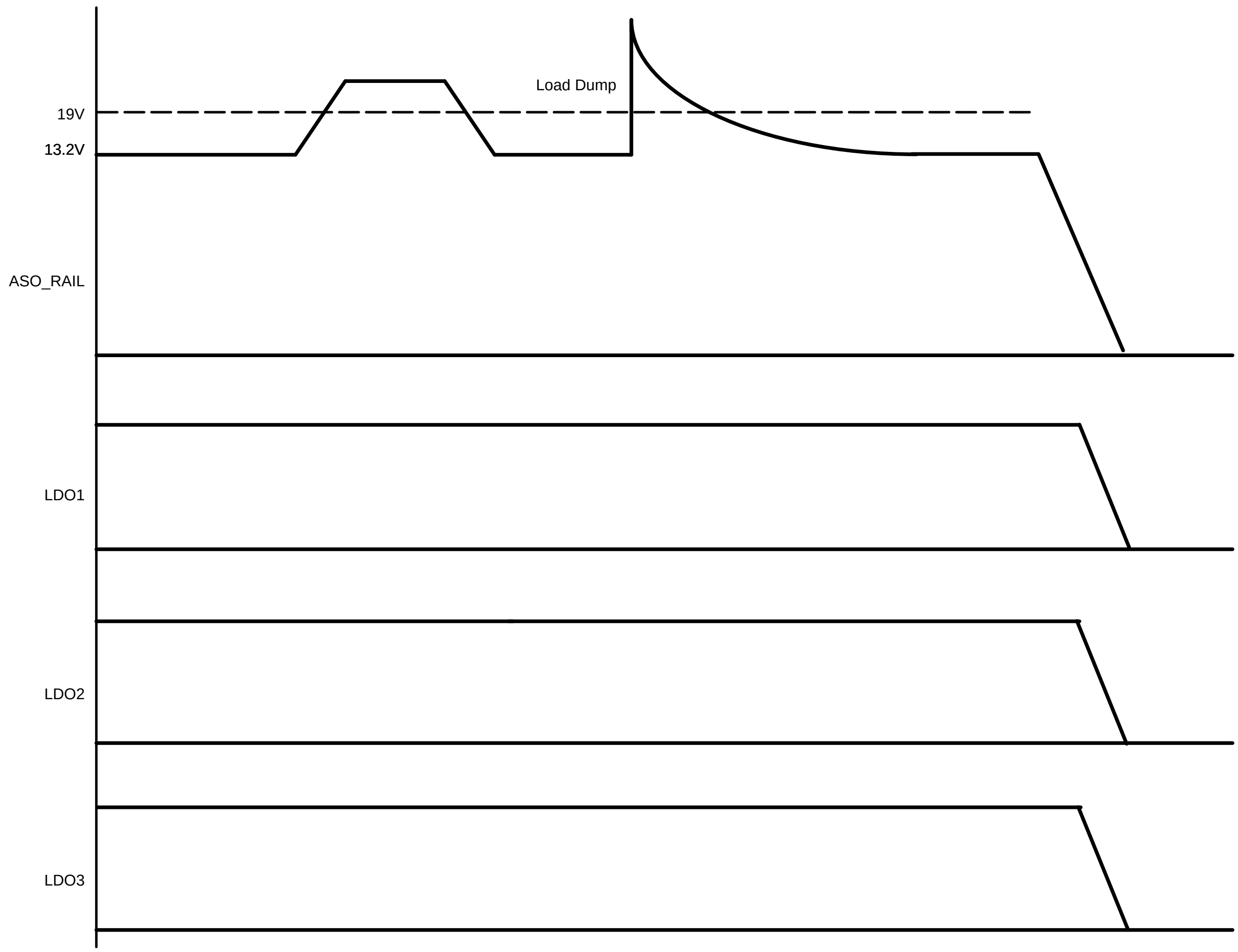



**Figure 11. NCV8612 Regulator Output Timing Diagram− VBATT_MON Grounded**

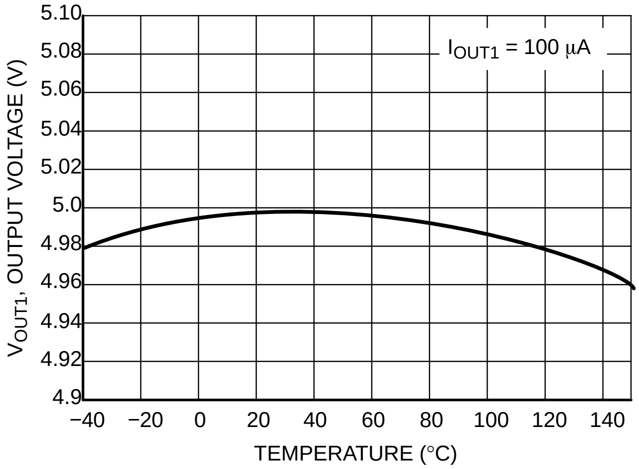



**Figure 12. Output Voltage LDO1 vs Temperature**

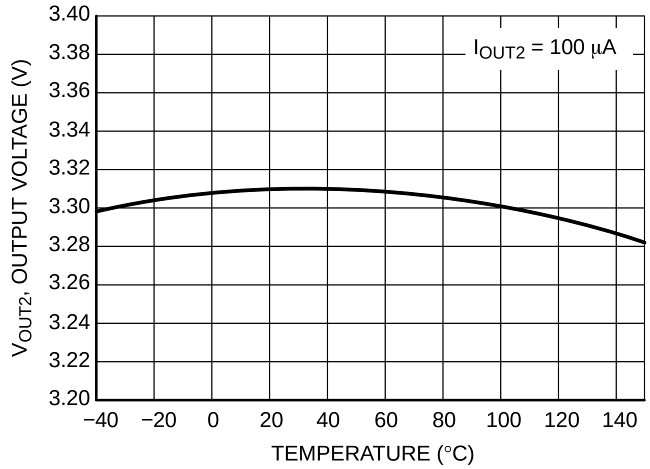



**Figure 13. Output Voltage LDO2 vs Temperature**

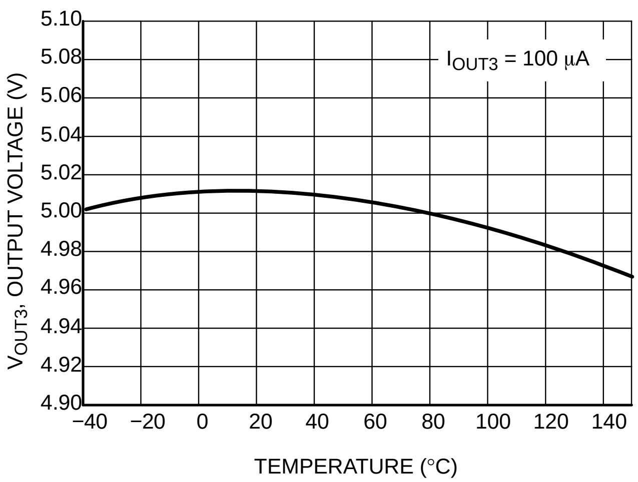



**Figure 14. Output Voltage LDO3 vs Temperature**

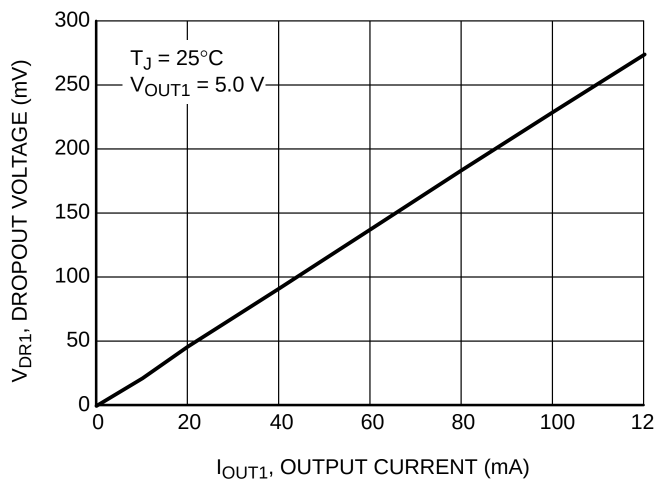



**Figure 15. Dropout LDO1 vs Output Current**

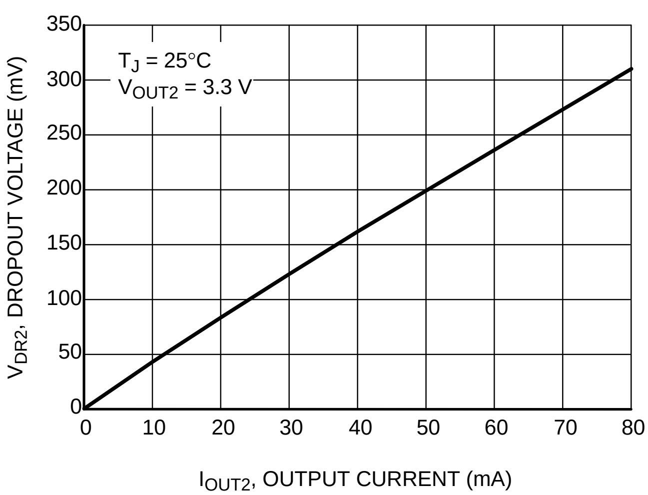



**Figure 16. Dropout LDO2 vs Output Current**

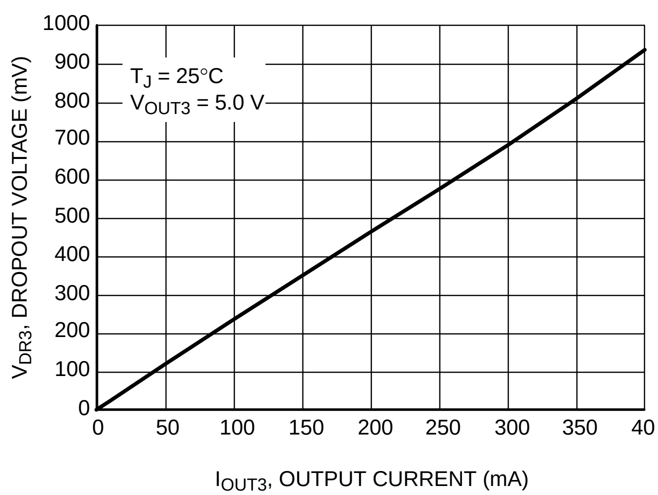



**Figure 17. Dropout LDO3 vs Output Current**

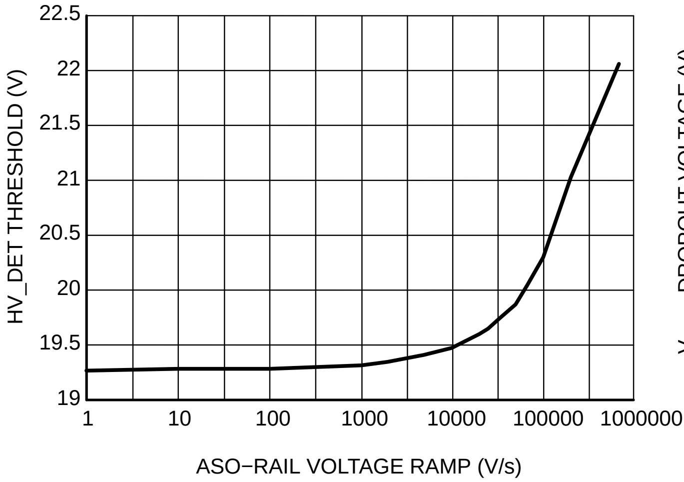



**Figure 18. HV−DET Threshold vs. dV/dt**

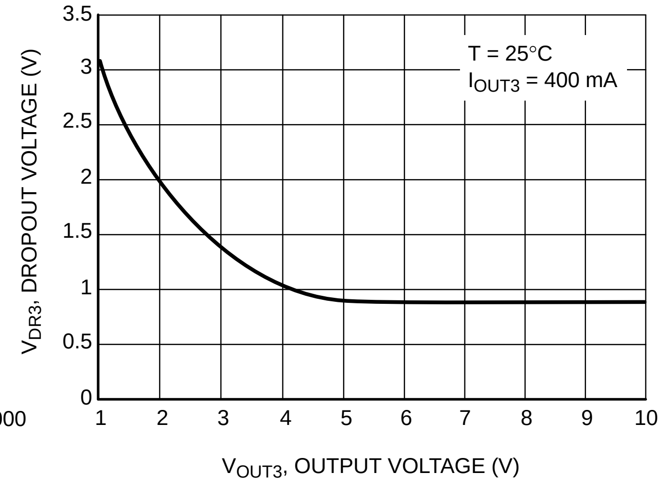



**Figure 19. LDO3 Dropout Voltage vs. Output Voltage**

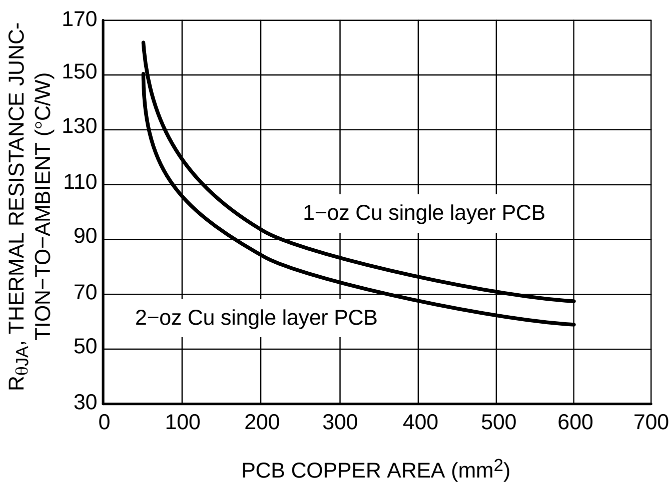



**Figure 20. $R_{\theta JA}$ vs. Copper Area**

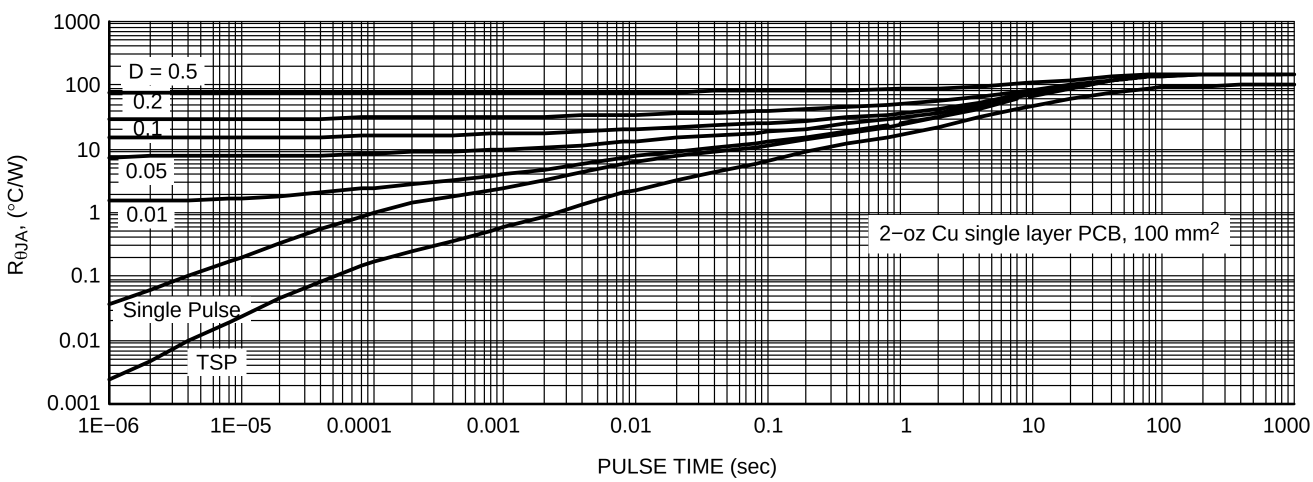



**Figure 21. $R_{\theta JA}$ vs. Duty Cycle**

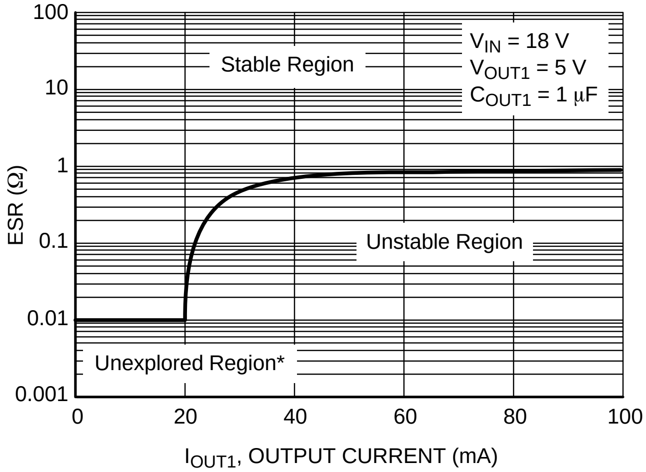



**Figure 22. $C_{OUT1}$ ESR Stability Region − 1 μF**

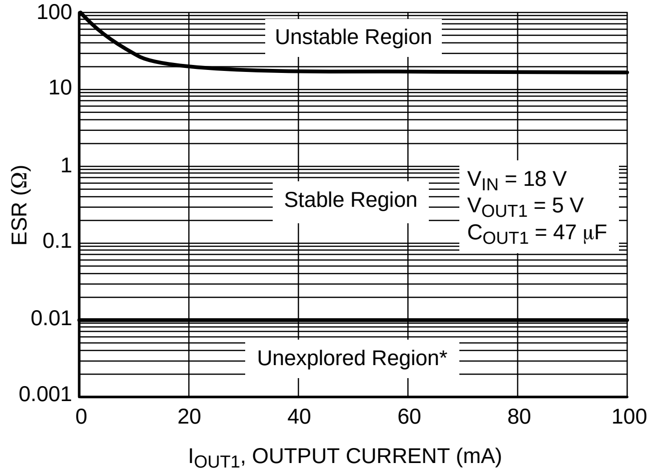



**Figure 23. $C_{OUT1}$ ESR Stability Region − 47 μF**

*The min specified ESR is based on Murata's capacitor GRM31CR60J476ME19 used in measurement. The true min ESR limit might be lower than shown.

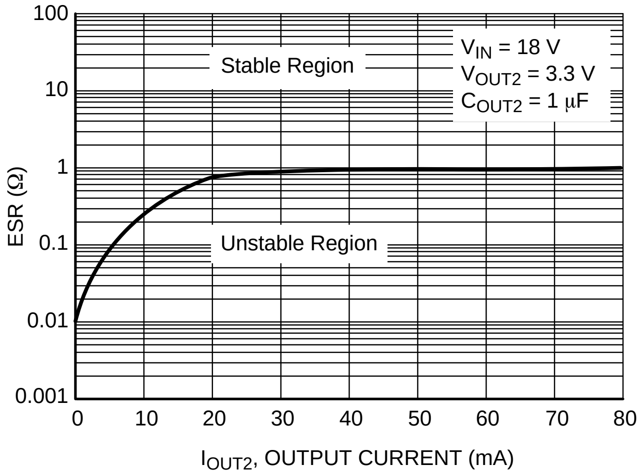



**Figure 24. $C_{OUT2}$ ESR Stability Region − 1 μF**

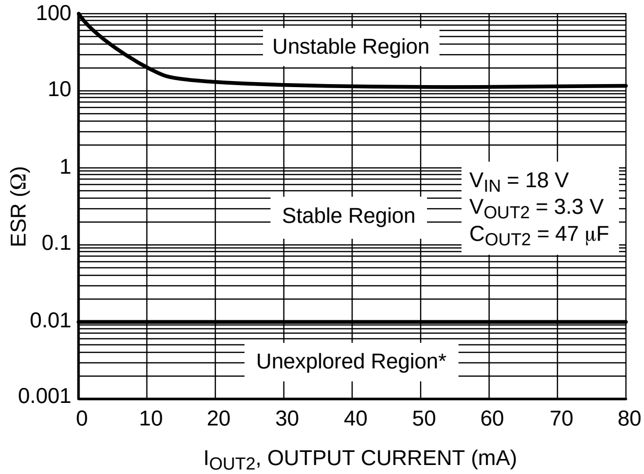



**Figure 25. $C_{OUT2}$ ESR Stability Region − 47 μF**

*The min specified ESR is based on Murata's capacitor GRM31CR60J476ME19 used in measurement. The true min ESR limit might be lower than shown.

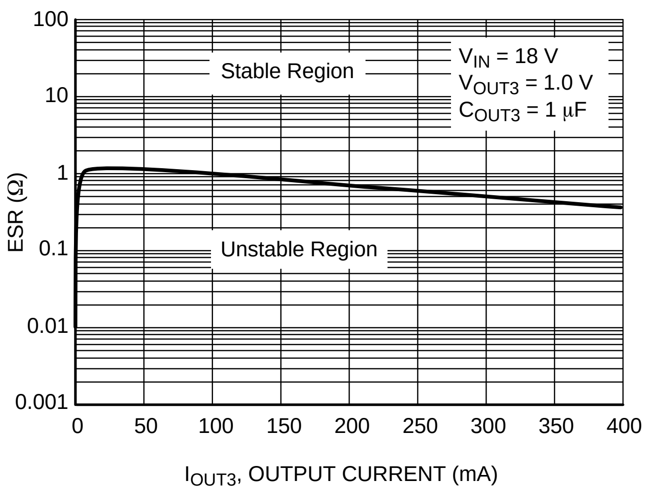



**Figure 26. $C_{OUT3}$ ESR Stability Region − 1 μF**

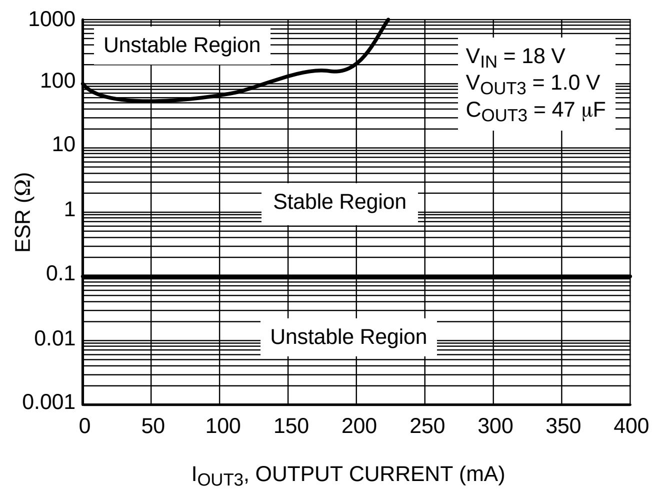



**Figure 27. $C_{OUT3}$ ESR Stability Region − 47 μF**

*The min specified ESR is based on Murata's capacitor GRM31CR60J476ME19 used in measurement. The true min ESR limit might be lower than shown.

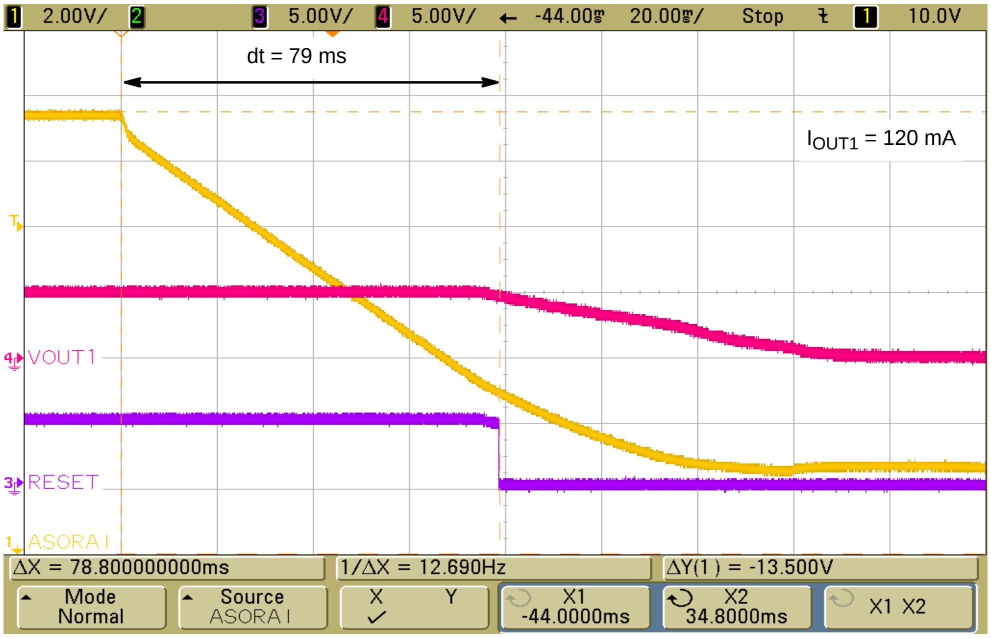



Figure 28. Output Response of LDO1 to Loss of Vin−B

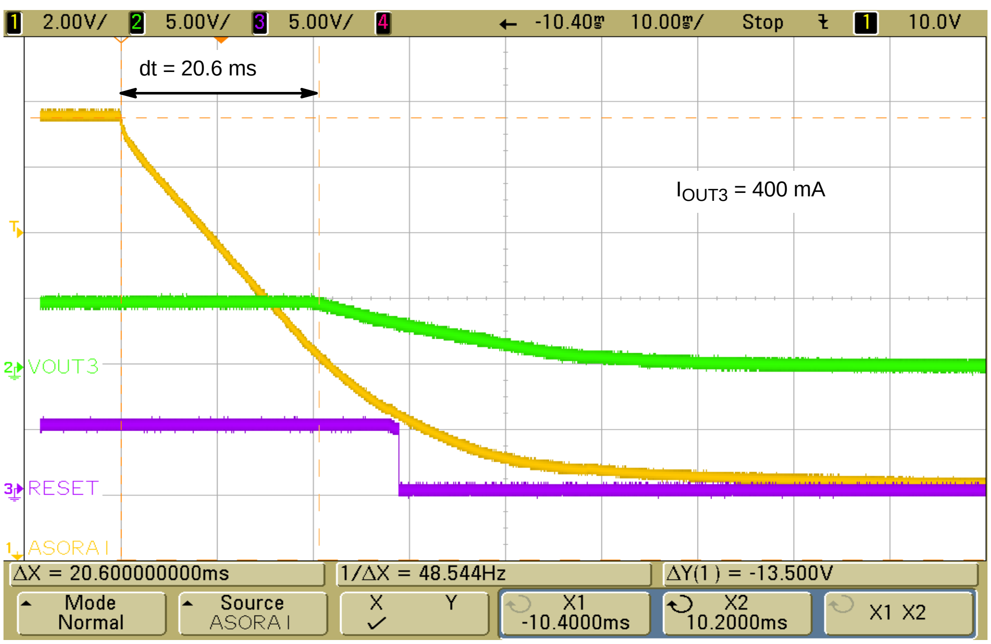



Figure 29. Output Response of LDO3 to Loss of Vin−B


Figure 30. Output Response of LDO2 to Loss of Vin−B


Figure 31. HV−DET Response to High Voltage − VBAT−MON tied to ASO−RAIL


**Figure 32. HV−DET Response to High Voltage − VBAT−MON Left Open**


**Figure 33. BO−DET Response to LOW Voltage − VBAT−MON tied to ASO−RAIL**

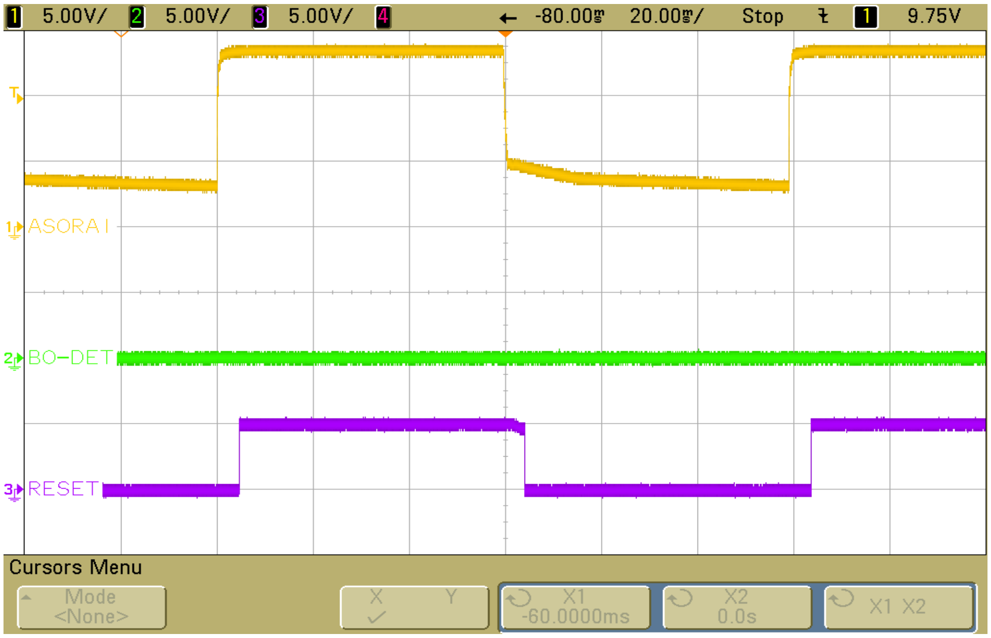



Figure 34. BO−DET Response to LOW Voltage − VBAT−MON Left Open

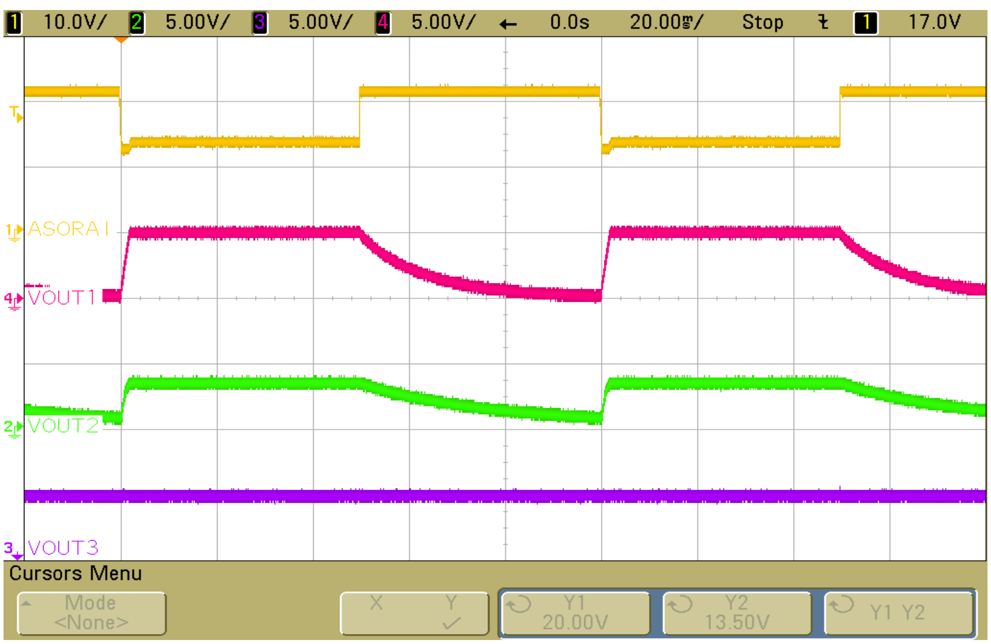



Figure 35. Output Response to OVS − VBAT−MON tied to ASO−RAIL


**Figure 36. Output Response to OVS − VBAT−MON Left Open**

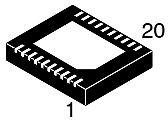
**ORDERING INFORMATION**

| Device | Conditions | Package | Shipping |
|---|---|---|---|
| NCV8612MNR2G | Enable with LDO1 Reset monitor, Adjustable LDO3 | 20 Lead DFN, 5x6 (Pb−Free) | 2500 / Tape & Reel |

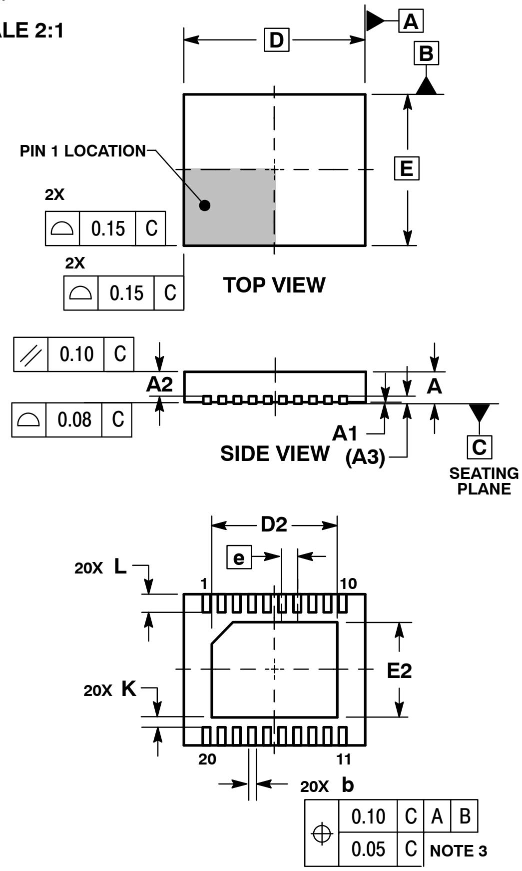
ON Semiconductor®

**DFN20, 6x5, 0.5P**
CASE 505AB
ISSUE C

DATE 23 MAY 2012



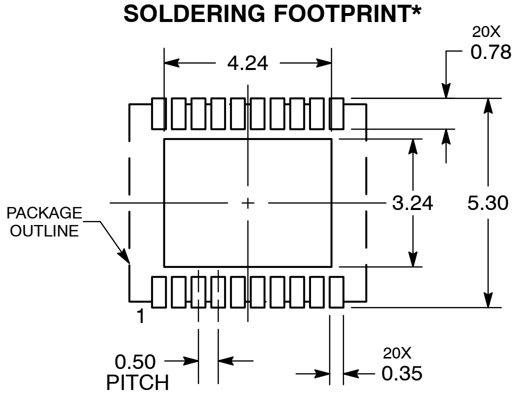

**SCALE 2:1**




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A2 | 0.65 | 0.75 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 6.00 BSC | |
| D2 | 3.98 | 4.28 |
| E | 5.00 BSC | |
| E2 | 2.98 | 3.28 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.50 | 0.60 |

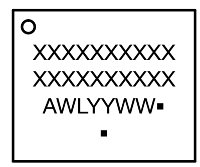
**RECOMMENDED SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| DOCUMENT NUMBER: | 98AON13117D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
|---|---|---|
| DESCRIPTION: | 20 PIN DFN, 6X5 MM, 0.5 MM PITCH | PAGE 1 OF 1 |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
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**ONLINE SUPPORT:** www.onsemi.com/support
**For additional information, please contact your local Sales Representative at**
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