



## eZ80Acclaim! Flash Microcontrollers

# eZ80F92/F93 Product Brief

PB010306-0803

### Product Block Diagram\*

eZ80F92 MCU			
128KB+256B Flash	8KB SRAM	24-Bit GPIO	
Infrared Encoder/ Decoder	2 UART	I <sup>2</sup> C	SPI
6 PRT	WDT	Real-Time Clock	
4 CS + WSG	JTAG	ZDI	

\*eZ80F92 shown. eZ80F93 features 64KB Flash, 4KB SRAM.

### Features

The eZ80F92 microcontroller is a member of ZiLOG's eZ80Acclaim! product family, which offers Flash versions of ZiLOG's eZ80<sup>®</sup> processor core. An additional controller, the eZ80F93, is intrinsically the same device, but offers smaller memory sizes. The eZ80F92 and eZ80F93 devices offer the following features:

- High-performance, pipelined eZ80F92 with single-cycle instruction fetch
  - eZ80F92—128KB on-chip Flash program memory and an extra 256 bytes configuration Flash memory; 8 KB on-chip high-speed SRAM
  - eZ80F93—64KB on-chip Flash program memory and an extra 256 bytes configuration Flash memory, 4 KB on-chip high-speed SRAM
- 24 General-Purpose I/O pins
- IrDA<sup>™</sup>-compatible Infrared Encoder/Decoder
- 2 UARTs with independent baud rate generators and providing up to 9 bits of data transmission
- I<sup>2</sup>C with independent clock rate generator
- SPI with independent clock rate generator
- Six 16-bit Counter/Timers with prescalers and direct input/output drive capability
- Watch-Dog Timer
- Real-time clock with on-chip 32KHz oscillator, selectable 50/60Hz input, and separate V<sub>DD</sub> pin for battery backup
- Glueless external memory interface with 4 Chip Selects, independent WAIT state generators, and external  $\overline{\text{WAIT}}$  input pin; supports eZ80<sup>®</sup>, Z80, Intel, and Motorola bus-compatible peripherals
- JTAG Debug Interface (also supports ZiLOG Debug Interface)
- Interrupt controller supports internal and external maskable interrupts as well as a non-maskable interrupt input
- New DMA-like eZ80<sup>®</sup> instructions
- Power management features including SLEEP/HALT modes and peripheral power-down controls
- 100-pin LQFP package, pin-compatible with the eZ80L92 microprocessor
- 3.0–3.6V supply voltage with 5V tolerant inputs
- Operating Temperature Ranges:
  - Standard: 0°C to +70°C
  - Extended: –40°C to +105°C
- 20MHz versions:
  - eZ80F92AZ020SC
  - eZ80F92AZ020EC
  - eZ80F93AZ020SC
  - eZ80F93AZ020EC

## General Description

The eZ80F92 and eZ80F93 microcontrollers are power-efficient, optimized, pipeline-architecture microcontrollers operating at 20MHz. They are new devices in a line of eZ80<sup>®</sup>-based standard products with integrated Flash memory, and are targeted toward industrial, communication, security, automation, and embedded Internet applications.

### eZ80<sup>®</sup> CPU Core

The eZ80Acclaim! is a Flash version of ZiLOG's eZ80<sup>®</sup> processor core, which can operate in Z80-compatible (64KB) mode or full 24-bit (16MB) addressing mode. Considering both the increased clock speed and processor efficiency, the eZ80<sup>®</sup>'s processing power rivals the performance of 16-bit microcontrollers. The eZ80<sup>®</sup> improves on the world-famous Z80 architecture. Like the Z80, it features dual bank registers for fast context switching.

## Peripherals Description

### On-Chip Memory

The eZ80F92 and eZ80F93 microcontrollers offer integrated Flash program memory. A separate page of 256 bytes Flash memory is available for general device configuration data.

- eZ80F92: 128KB Flash
- eZ80F93: 64KB Flash
- Single power supply operation
- Page erase feature: 1024 bytes/page
- Fast page erase and byte program operation
- 60ns maximum access time
- Endurance: 20,000 write cycles (typical)
- Data retention: greater than 100 years @ room temperature

In addition, high-speed relocatable SRAM is available for general application use.

- eZ80F92: 8KB SRAM
- eZ80F93: 4KB SRAM

### General-Purpose Input/Output

There are 24 bits of General Purpose Input or Output (GPIO) pins. All GPIO pins are individually programmable and support the following I/O modes: input, output, open-drain, open-source, level-triggered interrupts (High or Low), edge-triggered interrupts (High or Low), dual-edge-triggered interrupts, and alternate function.

### Infrared Encoder/Decoder

- Supports IrDA<sup>™</sup> SIR format
- Operates seamlessly with the on-chip UART
- Interfaces with IrDA<sup>™</sup>-compliant transceivers
- Supports transmit/receive to 115.2kbps

### Universal Asynchronous Receiver/Transmitter

Each of the two Universal Asynchronous Receiver/Transmitter (UART) devices contains control registers and a Baud Rate Generator (BRG).

- The Baud Rate Generator produces a lower-frequency bit clock from the system clock. All standard baud rates up to 115kbps and some rates higher than 115kbps are supported.
- The UART module implements all of the logic required to support asynchronous communications, hardware flow control, and 9-bit character format. The module also contains separate 16-byte-deep transmit and receive FIFOs.

### Inter-Integrated Circuit

The Inter-Integrated Circuit (I<sup>2</sup>C) device contains control registers and its own clock rate generator. The I<sup>2</sup>C operates in four modes: Master Transmit

or Master Receive, Slave Transmit or Slave Receive.

## Serial Peripheral Interface

The Serial Peripheral Interface (SPI) device contains control registers and its own clock rate generator. The SPI is a synchronous interface allowing several SPI-type devices to be interconnected. The SPI may be configured as either a master or a slave.

## Programmable Reload Timers

The eZ80F92 features six Programmable Reloadable Counter Timers (PRT). Each timer is a 16-bit down counter and offers a 4-bit clock prescaler with four selectable taps for  $CLK \div 4$ ,  $CLK \div 16$ ,  $CLK \div 64$ , and  $CLK \div 256$ . The timers' two modes of operation are single-pass and continuous count mode. Four timers can be driven through a GPIO input pin for external event count. Two other timers have the ability to drive general-purpose output pins.

## Watch-Dog Timer

The Watch-Dog Timer (WDT) features four programmable time-out periods:  $2^{18}$ ,  $2^{22}$ ,  $2^{25}$ , or  $2^{27}$  system clock cycles. It can operate from either the main system clock or the on-chip 32KHz oscillator (from RTC). Time-out action of the WDT is user programmable via hardware reset or nonmaskable interrupt to the eZ80F92. The source of action taken after a WDT time-out is indicated by a WDT status bit.

## Real-Time Clock

The real-time clock (RTC) allows counting of seconds, minutes, hours, days-of-the-week, day-of-the-month, month, year, and century. Alarms and interrupts can be set for seconds, minutes, hours, and day-of-the-week. The real-time clock input can be taken from the on-chip 32 KHz oscillator or from a 50/60Hz input. The real-time clock operates from an isolated  $V_{DD}$  pin to allow constant operation from a battery.

## Block Transfer Instructions

Four new block transfer instructions with expanded repeat capability are added to the eZ80F92. These provide performance similar to hardware DMAs.

## Chip Select/Wait State Generator and WAIT Pin

There are four chip selects for external devices. Each chip select may be programmed for either memory or I/O space. Each memory chip select can be individually programmed on a 64 KB boundary. The I/O chip selects can choose a 256-byte section of I/O space. The WAIT input pin facilitates interface with slow peripherals. The chip selects support eZ80<sup>®</sup>, Z80-, Intel-, and Motorola-style buses.

## JTAG Debug Interface

The IEEE1149.1-compatible JTAG debug interface supports all of the ZDI functions plus the following features: software break points, 64-word trace buffer, complex break points using address and data masks, and cascadable triggers.

## ZiLOG Debug Interface

The ZiLOG Debug Interface (ZDI) incorporates most of the functions of an In-Circuit Emulator on-chip. ZDI allows the user to single step code, change registers, edit programs, and view status of internal registers.

## Power Management

Several power management features are supported on the eZ80F92. Peripheral power-down registers allow independent clock gating of on-chip peripherals under software control while operating under normal conditions. The eZ80F92 can write to these control registers to disable the clock from driving any one of the peripherals when they are inactive.

In addition, execution of the HALT instruction suspends eZ80F92 operation and eliminates clock power associated with the eZ80F92 core. Normal

operation can be restored via external and peripheral interrupts or HW reset.

Execution of a SLP (Sleep) instruction provides the lowest power consumption. In SLEEP mode, only the on-chip RTC 32KHz crystal oscillator remains active to drive the RTC and the WDT. All other peripherals, the system clock, and the primary oscillator are disabled. An RTC alarm, a WDT time-out or HW Reset can restart the device.

## Electrical Features Summary

- Power supply: 3.3V  $\pm$  300mV
- Standard temperature: 0°C to +70°C
- Extended temperature: -40°C to +105°C
- Supply current @ 20MHz: <30mA (typical)
- Supply current in HALT mode with peripherals powered down: <10mA (typical)
- Supply current in SLEEP mode: <50 $\mu$ A (typical)

## Support Tools

The following development tools are available to program and debug applications using the eZ80F92 devices:

- eZ80F92 and Ethernet compact evaluation modules
- eZ80<sup>®</sup> Development Platform
- ZiLOG Development Suite IDE (ZDS) including assembler, linker, debugger, and simulator
- ZiLOG ANSI C-Compiler
- eZ80F92 Development Kit including:
  - One eZ80F92 module
  - eZ80<sup>®</sup> Development Platform
  - ZPAKII emulator with ZDI
  - ZDSII, ANSI C-Compiler

## Pin Diagram

Figure 1 diagrams the pin configuration of the eZ80F92 100-pin LQFP device. Each of the eZ80F92 and eZ80F93 parts features the same pin-out.

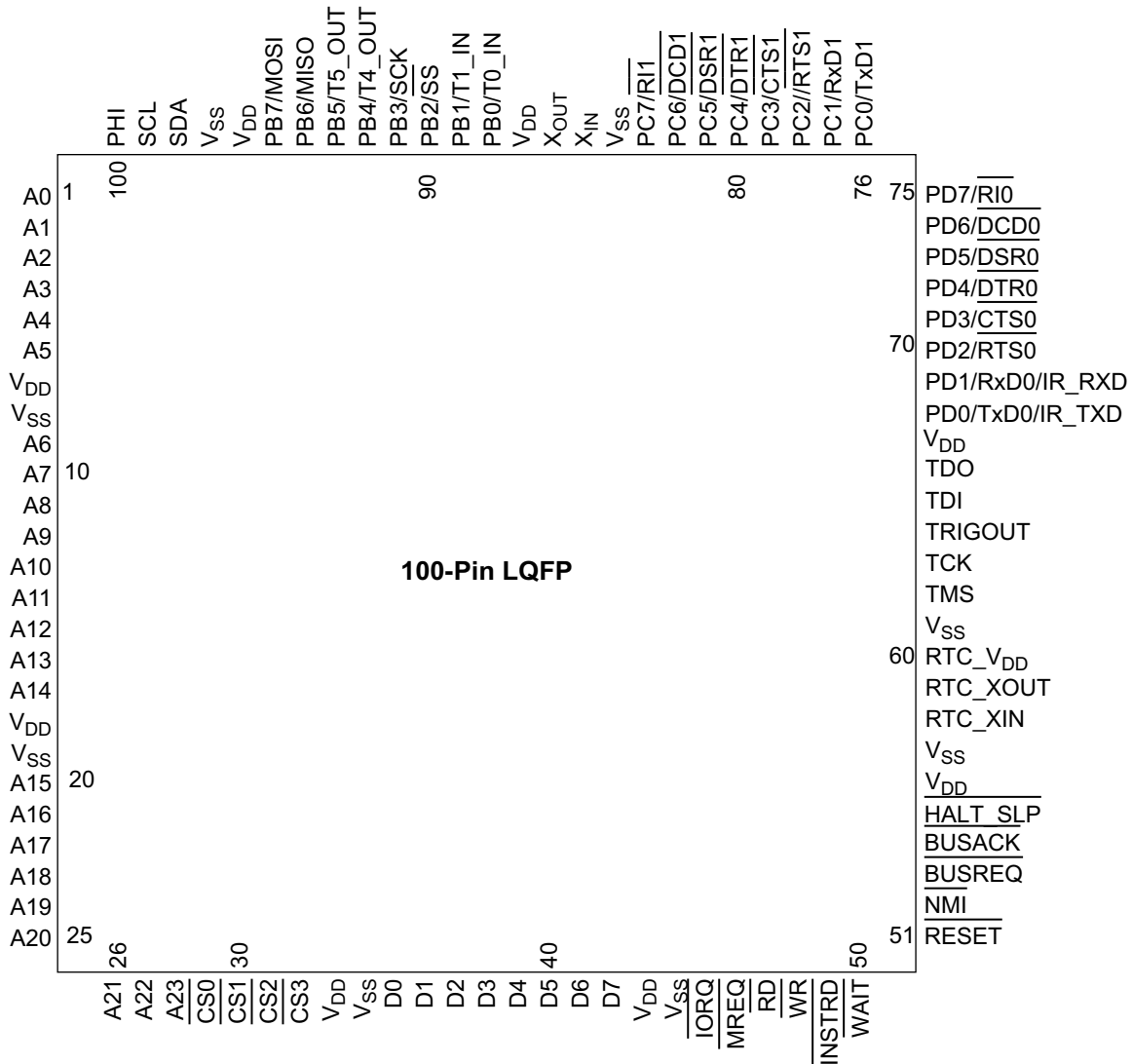
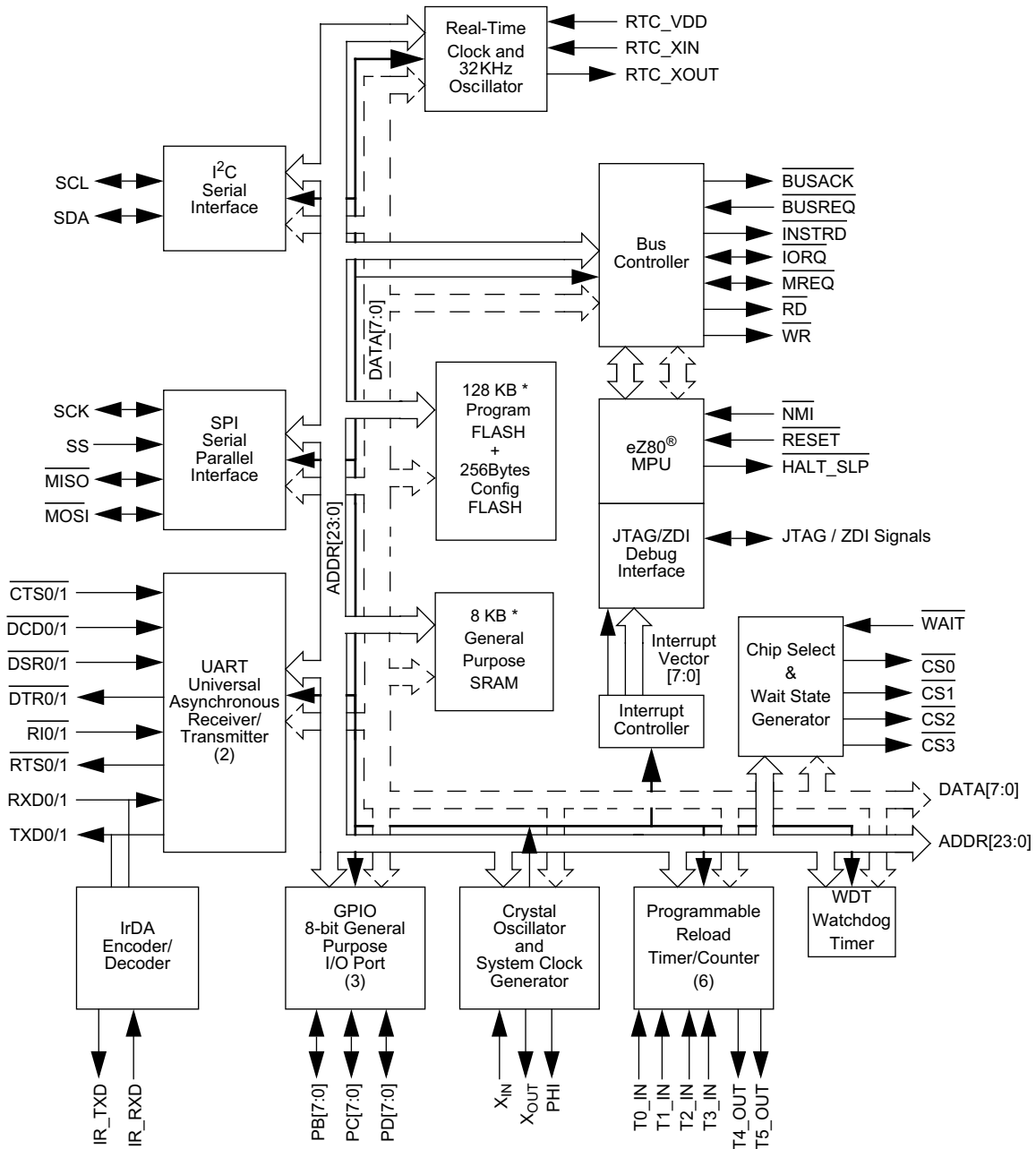


Figure 1. eZ80F92 100-Pin LQFP Pin Configuration

## Block Diagram

Figure 2 illustrates a block diagram of the eZ80F92 device.



\* Memory configuration for eZ80F92 shown. eZ80F93 features 64KB Flash and 4KB SRAM.

Figure 2. eZ80F92 Block Diagram

## Related Products

Other integrated devices of interest include:

eZ80190	50 MHz eZ80 <sup>®</sup> CPU, 8KB SRAM, 16x16 Multiply with 40-bit Accumulators, 32 bits GPIO, 6 Counter Timers with Prescalers, WDT, 4-channel CS+WSG, 2-Channel DMA, 2 UZI Channels, ZDI, On-Chip Oscillator.
eZ80L92	20MHz and 50MHz eZ80 <sup>®</sup> CPU, low-power modes, 24 bits GPIO, IrDA, 2 UART, I <sup>2</sup> C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4-channel CS, JTAG, ZDI.
eZ80F91	50MHz eZ80 <sup>®</sup> CPU, low-power modes, 256KB+512B Flash, 8KB SRAM, 32 bits GPIO, 10/100 EMAC, IrDA, 2 UART, I <sup>2</sup> C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4-channel CS+WSG, JTAG, ZDI, PLL.
Z80S180	Improved Z80 <sup>™</sup> CPU, 1MB MMU, 2 DMA, 2 16-bit PRTs, 2 UARTs, CSIO, up to 33MHz clock speed.
Z80181	Z8S180 CPU, SCC, CTC, 16-bit GPIO, up to 33MHz clock speed.
Z80182	Z8S180 CPU, 2 ESCC, 24-bit GPIO, 16550 Mimic interface, up to 33MHz clock speed.
Z84C00	Z80 <sup>™</sup> CPU (up to 20 MHz).
Z84C15	Z80 <sup>™</sup> CPU, 2 SIO, 4x8 CTC, 2 PIO, WDT, up to 16MHz clock speed.

## Ordering Information

PSI	Part	Description
eZ80F92AZ020SC	20MHz, Standard Temperature	eZ80F92, 128KB Flash, 8KB SRAM.
eZ80F92AZ020EC	20MHz, Extended Temperature	eZ80F92, 128KB Flash, 8KB SRAM.
eZ80F93AZ020SC	20MHz, Standard Temperature	eZ80F93, 64KB Flash, 4KB SRAM.
eZ80F93AZ020EC	20MHz, Extended Temperature	eZ80F93, 64KB Flash, 4KB SRAM.
eZ80F920200ZCO	eZ80F92 Development Kit	Complete eZ80Acclaim! Development Kit.



This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

**ZiLOG Worldwide Headquarters**

532 Race Street  
San Jose, CA 95126  
Telephone: 408.558.8500  
Fax: 408.558.8300  
[www.ZiLOG.com](http://www.ZiLOG.com)

**Document Disclaimer**

ZiLOG is a registered trademark of ZiLOG Inc. in the United States and in other countries. All other products and/or service names mentioned herein may be trademarks of the companies with which they are associated.

©2003 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZiLOG ALSO DOES NOT

ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Devices sold by ZiLOG, Inc. are covered by warranty and limitation of liability provisions appearing in the ZiLOG, Inc. Terms and Conditions of Sale. ZiLOG, Inc. makes no warranty of merchantability or fitness for any purpose Except with the express written approval of ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.