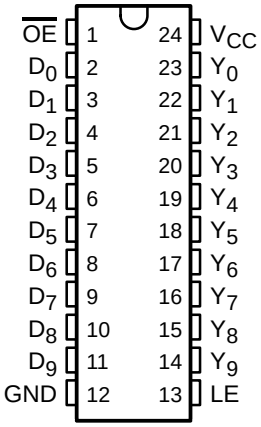
- **Function, Pinout, and Drive Compatible With FCT, F, and AM29841 Logic**
- **Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **High-Speed Parallel Latches**
- **Buffered Common Latch-Enable Input**
- **3-State Outputs**
- **CY54FCT841T**
  - **32-mA Output Sink Current**
  - **12-mA Output Source Current**
- **CY74FCT841T**
  - **64-mA Output Sink Current**
  - **32-mA Output Source Current**

CY54FCT841T . . . D PACKAGE
CY74FCT841T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



description

The ’FCT841T bus-interface latches are designed to eliminate additional packages required to buffer existing latches and provide additional data width for wider address/data paths or buses carrying parity. The ’FCT841T devices are buffered 10-bit-wide versions of the FCT373 function.

The ’FCT841T devices’ high-performance interface is designed for high-capacitance-load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D	I	Latch data inputs
LE	I	Latch-enable input. The latches are transparent when LE is high. Input data is latched on the high-to-low transition.
Y	O	3-state latch outputs
$\overline{OE}$	I	Output-enable control. When $\overline{OE}$ is low, the outputs are enabled. When $\overline{OE}$ is high, the outputs are in the high-impedance (off) state.

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.5	CY74FCT841CTQCT	FCT841C
	SOIC – SO	Tube	5.5	CY74FCT841CTSOC	FCT841C
		Tape and reel	5.5	CY74FCT841CTSOCT	
	DIP – P	Tube	6.5	CY74FCT841BTPC	CY74FCT841BTPC
	SOIC – SO	Tube	9	CY74FCT841ATSOC	FCT841A
		Tape and reel	9	CY74FCT841ATSOCT	
–55°C to 125°C	CDIP – D	Tube	10	CY54FCT841ATDMB	

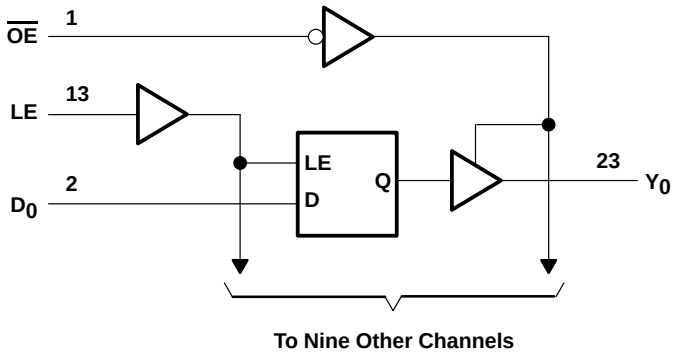
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	LE	D	O	Y	
H	X	X	X	Z	Z
H	H	L	L	Z	
H	H	H	H	Z	
H	L	X	NC	Z	Latched (Z)
L	H	L	L	L	Transparent
L	H	H	H	H	
L	L	X	NC	NC	Latched

H = High logic level, L = Low logic level, X = Don't care, NC = No change, Z = High-impedance state

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential . . . . . –0.5 V to 7 V
DC input voltage range . . . . . –0.5 V to 7 V
DC output voltage range . . . . . –0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . . 120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package . . . . . 67°C/W
(see Note 2): Q package . . . . . 61°C/W
(see Note 2): SO package . . . . . 46°C/W
Ambient temperature range with power applied, T_A . . . . . –65°C to 135°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		CY54FCT841T			CY74FCT841T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–32	mA
I_{OL}	Low-level output current			32			64	mA
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			CY54FCT841T			CY74FCT841T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{IN} = –18 mA			–0.7	–1.2				V
	V_{CC} = 4.75 V,	I_{IN} = –18 mA						–0.7	–1.2	
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –12 mA		2.4	3.3					V
	V_{CC} = 4.75 V	I_{OH} = –32 mA					2			
		I_{OH} = –15 mA					2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA			0.3	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA						0.3	0.55	
V_{hys}	All inputs				0.2			0.2		V
I_I	V_{CC} = 5.5 V,	V_{IN} = V_{CC}				5				µA
	V_{CC} = 5.25 V,	V_{IN} = V_{CC}							5	
I_{IH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V				±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V							±1	
I_{IL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V				±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V							±1	
I_{OZH}	V_{CC} = 5.5 V,	V_{OUT} = 2.7 V				10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V							10	
I_{OZL}	V_{CC} = 5.5 V,	V_{OUT} = 0.5 V				–10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V							–10	
I_{OS}‡	V_{CC} = 5.5 V,	V_{OUT} = 0 V		–60	–120	–225				mA
	V_{CC} = 5.25 V,	V_{OUT} = 0 V					–60	–120	–225	
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V				±1			±1	µA
I_{CC}	V_{CC} = 5.5 V,	V_{IN} ≤ 0.2 V,	V_{IN} ≥ V_{CC} – 0.2 V		0.1	0.2				mA
	V_{CC} = 5.25 V,	V_{IN} ≤ 0.2 V,	V_{IN} ≥ V_{CC} – 0.2 V					0.1	0.2	
ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open				0.5	2				mA
	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open							0.5	2	
I_{CCD}¶	V_{CC} = 5.5 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V				0.06	0.12				mA/ MHz
	V_{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V							0.06	0.12	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT841T			CY74FCT841T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_C#	V_{CC} = 5.5 V, Outputs open, $\overline{OE}$ = GND, LE = V_{CC}	One bit switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		0.7	1.4				mA
			V_{IN} = 3.4 V or GND		1	2.4				
		10 bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		1	3.2‖				
			V_{IN} = 3.4 V or GND		4.1	13.2‖				
	V_{CC} = 5.25 V, Outputs open, $\overline{OE}$ = GND, LE = V_{CC}	One bit switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					0.7	1.4	
			V_{IN} = 3.4 V or GND					1	2.4	
		10 bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					1	3.2‖	
			V_{IN} = 3.4 V or GND					4.1	13.2‖	
C_i					5	10		5	10	pF
C_o					9	12		9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current
I_{CC} = Power-supply current with CMOS input levels
ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_0 = Clock frequency for registered devices, otherwise zero
f_1 = Input signal frequency
N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY54FCT841AT		CY74FCT841AT		CY74FCT841BT		CY74FCT841CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5		4		4		4		ns
t_{su}	Setup time, data before LE↑	2.5		2.5		2.5		2.5		ns
t_h	Hold time, data after LE↑	3		2.5		2.5		2.5		ns

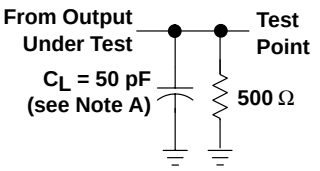
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY54FCT841AT		CY74FCT841AT		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	D	Y	C_L = 50 pF, R_L = 500 Ω	1.5	10	1.5	9	ns
t_{PHL}				1.5	10	1.5	9	
t_{PLH}	D	Y	C_L = 300 pF, R_L = 500 Ω	1.5	15	1.5	13	ns
t_{PHL}				1.5	15	1.5	13	
t_{PLH}	LE	Y	C_L = 50 pF, R_L = 500 Ω	1.5	13	1.5	12	ns
t_{PHL}				1.5	13	1.5	12	
t_{PLH}	LE	Y	C_L = 300 pF, R_L = 500 Ω	1.5	20	1.5	16	ns
t_{PHL}				1.5	20	1.5	16	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF, R_L = 500 Ω	1.5	13	1.5	11.5	ns
t_{PZL}				1.5	13	1.5	11.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 300 pF, R_L = 500 Ω	1.5	25	1.5	23	ns
t_{PZL}				1.5	25	1.5	23	
t_{PHZ}	$\overline{OE}$	Y	C_L = 5 pF, R_L = 500 Ω	1.5	9	1.5	7	ns
t_{PLZ}				1.5	9	1.5	7	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF, R_L = 500 Ω	1.5	10	1.5	8	ns
t_{PLZ}				1.5	10	1.5	8	

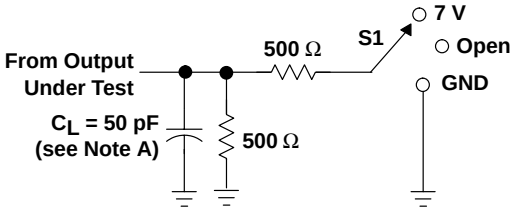
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT841BT		CY74FCT841CT		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	D	Y	C_L = 50 pF, R_L = 500 Ω	1.5	6.5	1.5	5.5	ns
t_{PHL}				1.5	6.5	1.5	5.5	
t_{PLH}	D	Y	C_L = 50 pF, R_L = 500 Ω	1.5	13	1.5	13	ns
t_{PHL}				1.5	13	1.5	13	
t_{PLH}	LE	Y	C_L = 50 pF, R_L = 500 Ω	1.5	8	1.5	6.4	ns
t_{PHL}				1.5	8	1.5	6.4	
t_{PLH}	LE	Y	C_L = 300 pF, R_L = 500 Ω	1.5	15.5	1.5	15	ns
t_{PHL}				1.5	15.5	1.5	15	
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF, R_L = 500 Ω	1.5	8	1.5	6.5	ns
t_{PZL}				1.5	8	1.5	6.5	
t_{PZH}	$\overline{OE}$	Y	C_L = 300 pF, R_L = 500 Ω	1.5	14	1.5	12	ns
t_{PZL}				1.5	14	1.5	12	
t_{PHZ}	$\overline{OE}$	Y	C_L = 5 pF, R_L = 500 Ω	1.5	6	1.5	5.7	ns
t_{PLZ}				1.5	6	1.5	5.7	
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF R_L = 500 Ω,	1.5	7	1.5	6	ns
t_{PLZ}				1.5	7	1.5	6	

PARAMETER MEASUREMENT INFORMATION

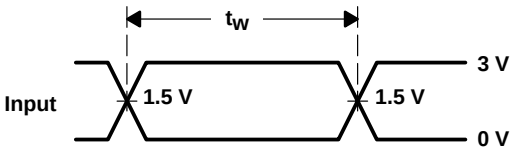


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

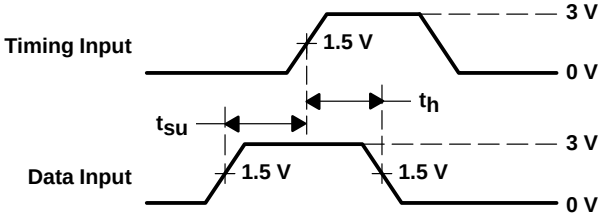


LOAD CIRCUIT FOR
3-STATE OUTPUTS

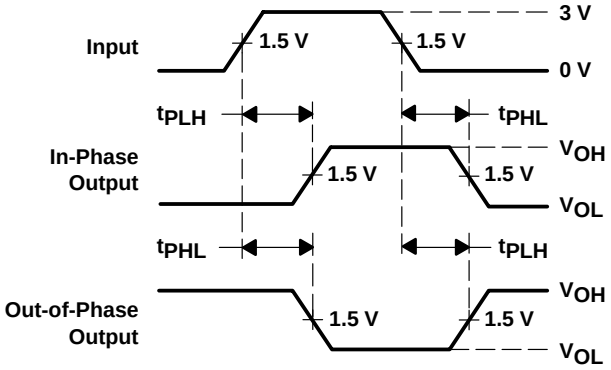
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



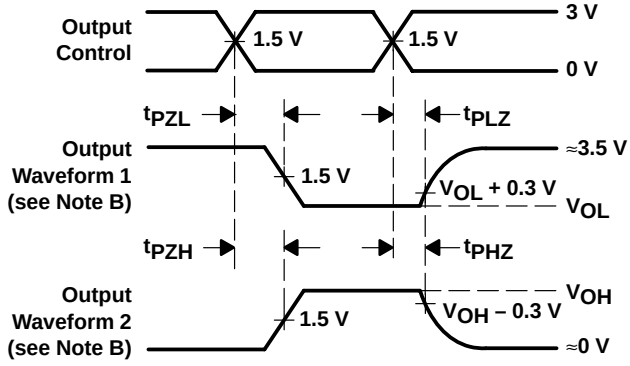
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY54FCT841ATDMB	ACTIVE	CDIP	JT	24	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CY54FCT841ATDMB	Samples
CY74FCT841ATSOC	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841A	Samples
CY74FCT841ATSOCT	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841A	Samples
CY74FCT841CTQCT	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT841C	Samples
CY74FCT841CTSOC	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841C	Samples
CY74FCT841CTSOCT	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT841C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

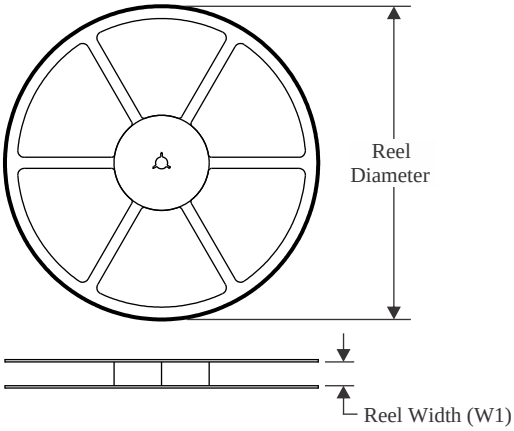
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

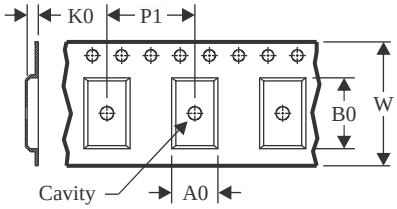
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

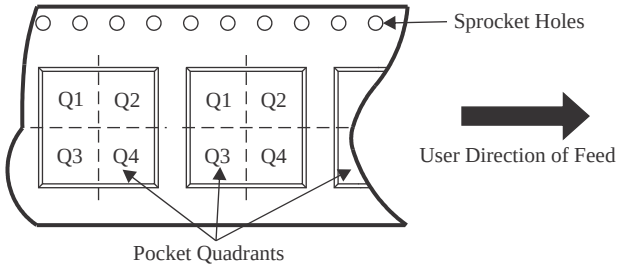


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

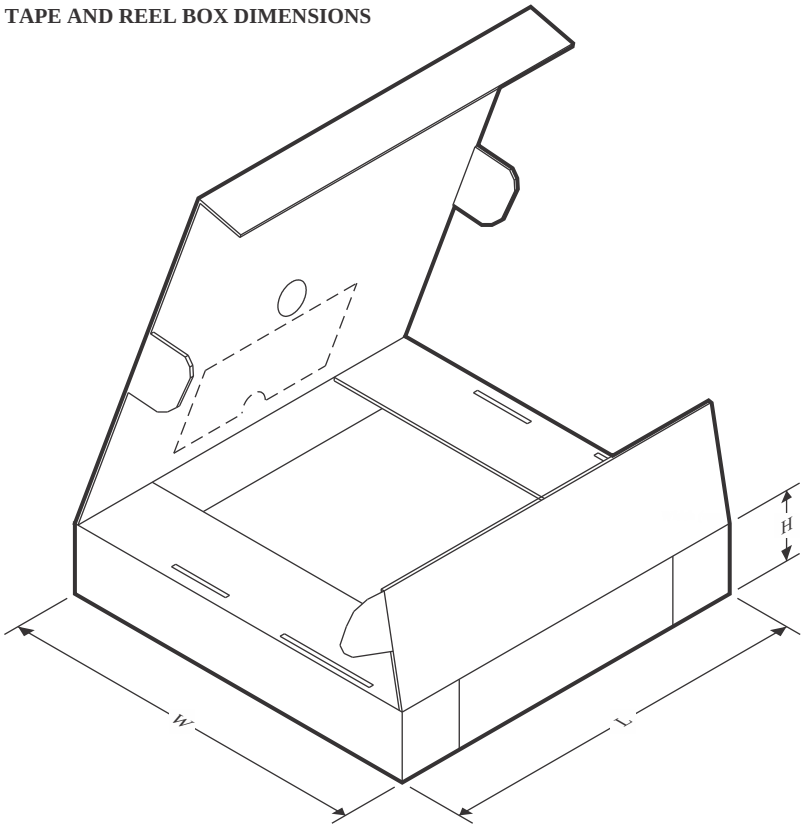
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT841ATSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT841CTQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT841CTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

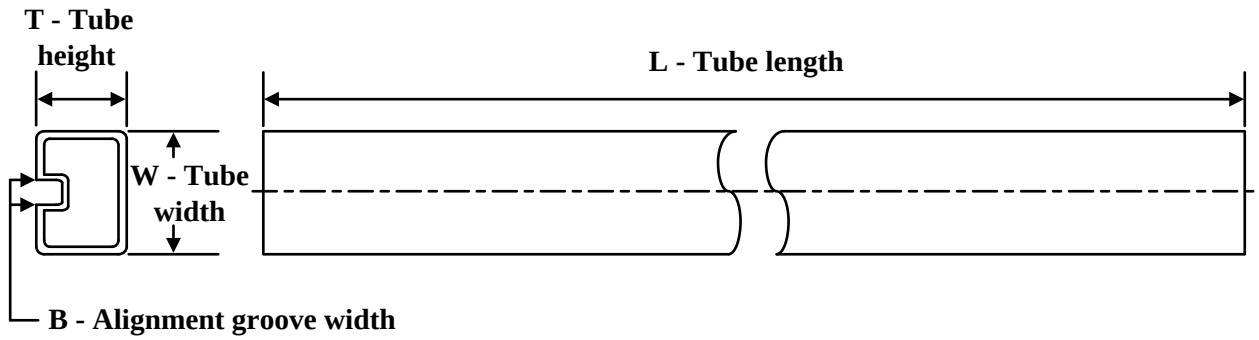
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT841ATSOCT	SOIC	DW	24	2000	350.0	350.0	43.0
CY74FCT841CTQCT	SSOP	DBQ	24	2500	356.0	356.0	35.0
CY74FCT841CTSOCT	SOIC	DW	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CY74FCT841ATSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT841CTSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265