TRC101

300-1000 MHz Transceiver

Complies with Directive 2002/95/EC (RoHS)

16-TSSOP package

Product Overview

TRC101 is a highly integrated single chip, zero-IF, multi-channel, low power RF transceiver. It is an ideal fit for low cost, high volume, two way short-range wireless applications for use in the unlicensed 300-1000 MHz frequency bands. All critical RF and baseband functions are completely integrated in the chip, thus minimizing external component count and simplifying and speeding design-ins. Use of a low cost, generic 10MHz crystal and a low-cost microcontroller is all that is needed to create a complete link. The TRC101 also incorporates different sleep modes to reduce overall current consumption and extend battery life. Its small size with low power consumption makes it ideal for various short range radio applications.

Key Features

- Modulation: FSK (Frequency Hopping Spread Spectrum capability)
- Frequency range: 300-1000 MHz
- High sensitivity: (-105 dBm)
- High data rate: Up to 256 kbps
- Low current consumption
  (RX current ~8.5mA)
- Wide operating supply voltage: 2.2 to 5.4V
- Low standby current (0.2uA)
- Integrated PLL, IF, Baseband Circuitry
- Automatic Frequency Adjust(TX/RX frequency alignment)
- Programmable Analog/Digital Baseband Filter
- Programmable Output RF Power
- Programmable Input LNA Gain
- Internal Valid Data Recognition
- Transmit/Receive FIFO
- Standard SPI Interface
- TTL/CMOS Compatible I/O pins
- Programmable CLK Output Freq
- Automatic Antenna tuning circuit
- Low cost, generic 10MHz Xtal reference
- Integrated, Programmable Low Battery Voltage Detector
- Programmable Wake-up Timer with programmable Duty Cycle
- Integrated Selectable Analog/Digital RSSI
- Integrated Crystal Oscillator
- External Processor Interrupt pin
- Programmable Crystal Load Capacitance
- Programmable Data Rate
- Integrated Clock & Data Recovery
- Programmable FSK Deviation Polarity
- External Wake-up Events
- Support for Multiple Channels
  - [315/433 Bands] 95 Channels (100kHz)
  - [868 Band] 190 Channels (100kHz)
  - [915 Band] 285 Channels (100kHz)
- Power-saving sleep mode
- Very few external components requirement
- Small size plastic package: 16-pin TSSOP
- Standard 13 inch reel, 2000 pieces.

Popular applications

- Active RFID tags
- Automated Meter reading
- Home & Industrial Automation
- Security systems
- Two way Remote keyless entry
- Automobile Immobilizers
- Sports & Performance monitoring
- Wireless Toys
- Medical equipment
- Low power two way telemetry systems
- Wireless mesh sensors
- Wireless modules

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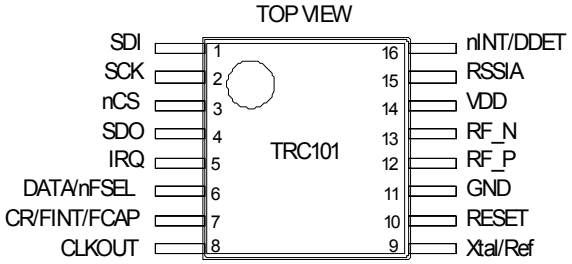
1. Pin Configuration



1.1 Pin Descriptions

Pin	Name	Description
1	**SDI**	**SPI Data In**
2	**SCK**	**SPI Data Clock**
3	**nCS**	**Chip Select Input** – Selects the chip for an SPI data transaction. The pin must be pulled 'low' for a 16-bit read or write function. See Figure 6 for timing specifications.
4	**SDO**	**SPI Data Out**
5	**nIRQ**	**Interrupt Request Output** - The receiver will generate an active low interrupt request for the microcontroller on the following events: · The TX register is ready to receive the next byte · The FIFO has received the preprogrammed amount of bits · Power-on reset · FIFO overflow/TX register underrun · Wake-up timer timeout · Negative pulse on the interrupt input pin nINT · Supply voltage below the preprogrammed value is detected
6	**Data/nFSel**	**Data In** – When the internal TX register is not used, this pin may be used to manually modulate data from an external host processor. If the internal TX register is enabled, this pin must be pulled "High". When using the internal Rx FIFO, this pin must be pulled "Low" to select the FIFO. This pin is used to select the internal registers when reading and writing. **Data Out** – When the internal FIFO is not used this pin is used in conjunction with pin 7 (Recovered Clock) to receive data. **FIFO Select** – When reading the FIFO, this pin selects the FIFO and the first bit appears on the next clock. Use this pin in conjunction with Pin 7.
7	**CR/FINT/FCAP**	**Recovered Clock Output** – When the digital filter is used (*Baseband Filter Register*, Bit [4]) and FIFO disabled (*Configuration Register,* Bit [6]), this pin provides the recovered clock from the incoming data. **FIFO INT** – When the internal FIFO is enabled (*Configuration Register,* Bit [6]), this pin acts as a FIFO Full interrupt indicating that the FIFO has filled to its pre-programmed limit (*FIFO Configuration Register*, Bit [7..4]). **External Data Filter Capacitor** – When the Analog filter is used (*Baseband Filter Register*, Bit [4]), this pin is the raw baseband data that may be used by a host processor for data recovery. The external capacitor forms a simple lowpass filter with an internal 10KOhm series resistor. The capacitor value may be chosen for a Max data rate up to 256kbps.
8	**ClkOut**	Optional host processor Clock Output
9	**Xtal/Ref**	**Xtal** - Connects to a 10MHz series crystal or an external oscillator reference. The circuit contains an integrated load capacitor (See *Configuration Register*) in order to minimize the external component count. The crystal is used as the reference for the PLL, which generates the local oscillator frequency. The accuracy requirements for production tolerance, temperature drift and aging can be determined from the maximum allowable local oscillator frequency error. Whenever a low frequency error is essential for the application, it is possible to "pull" the crystal to the accurate frequency by changing the load capacitor value. **Ext Ref** – An external reference, such as an oscillator, may be connected as a reference source. Connect through a .01uF capacitor.
10	**nRESET**	**Reset Output** with internal pull-up
11	**GND**	**System Ground**
12	**RF_P**	**RF Diff I/O**
13	**RF_N**	**RF Diff I/O**
14	**VDD**	**Supply Voltage**
15	**RSSIA**	**Analog RSSI Output –** The Analog RSSI can be used to determine the actual signal strength. The response and settling time depends on an external filter capacitor. Typically, a 1000pF capacitor will provide optimum response time for most applications.
16	**nINT/DDet**	**nINT** – This pin may be configured as an active low external interrupt to the chip. When a logic '0' is applied to this pin, it causes the nIRQ pin (5) to toggle, signaling an interrupt to an external processor. Reading the first four (4) bits of the status register tells the source of the interrupt. This pin may be used as a wake-up event from sleep. **Valid Data Detector Output**– This pin may be configured to indicate Valid Data when the synchronous

		pattern recognition circuit indicates potentially real incoming data.

2. Functional Description

The TRC101 is a low power, frequency agile, zero-IF, multi-channel FSK transceiver for use in the 315, 433, 868, and 916 MHz bands. All RF and baseband functions are completely integrated requiring only a single 10MHz crystal as a reference source and an external low-cost processor. Functions include:

- PLL synthesizer
- Power Amp
- LNA
- I/Q Mixers
- I/Q Demodulators
- Baseband Filters
- Baseband Amplifiers
- RSSI
- Low Battery Detector
- Wake-up Timer/Duty Cycle Mode
- Valid Data Detection/Data Quality

The TRC101 is ideal for Frequency Hopping Spread Spectrum (FHSS) applications requiring frequency agility to meet FCC requirements. Use of a low-cost microcontroller is all that is needed to create a complete data link. The TRC101 incorporates different sleep modes to reduce overall current consumption and extend battery life. It is ideal for applications operating from typical lithium coin cells.

2.1 TRC101 Typical Application Circuit

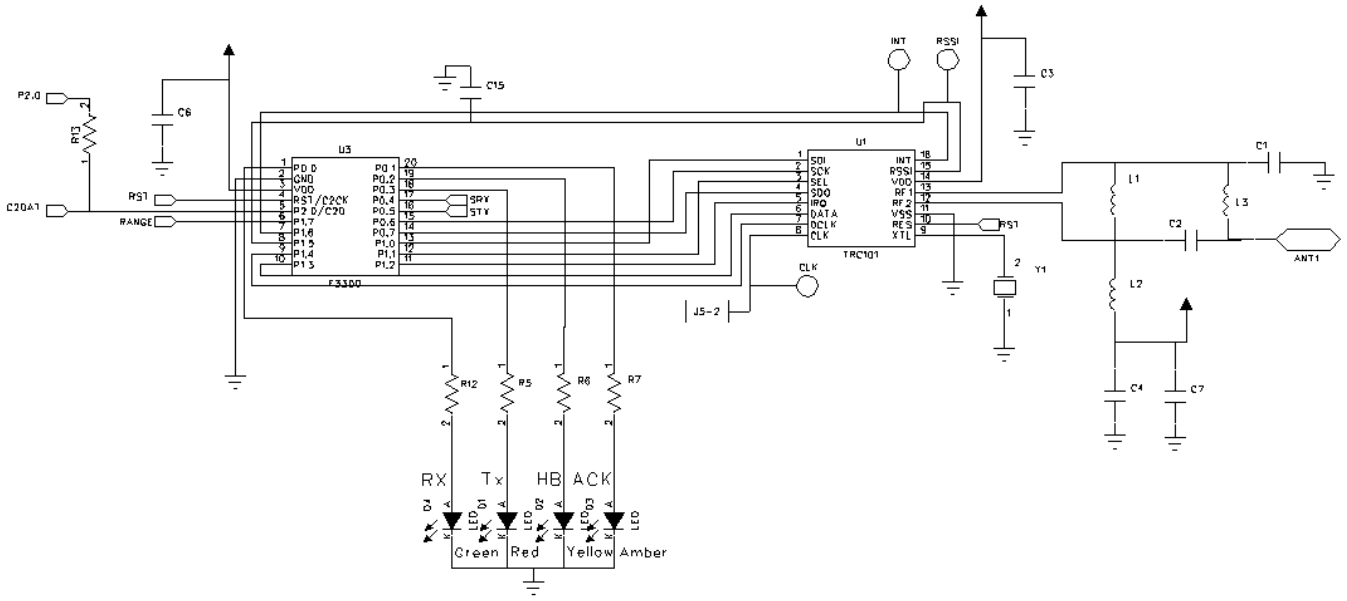


Figure 1. Typical Application Circuit

RF Transmitter Matching

The RF pins are high impedance and differential. The optimum differential load for the RF port at a given frequency band is shown in Table 1.

TABLE 1.

TRC101	Admittance	Impedance (Ohm)	L
315 MHz	1.5e-3 – j5.14e-3	52 + j179	98nH
433 MHz	1.4e-3 – j7.1e-3	27 + j136	52nH
868 MHz	2e-3 – j1.5e-2	8.7 + j66	12.5nH

916 MHz	2.2e-3 – j1.55e-2	9 + j63	11.2nH

These values are what the RF port pins want to "see" as an antenna load for maximum power transfer. Antennas ideally suited for this would be a Dipole, Folded Dipole, and Loop. For all transmit antenna applications a bias or "choke" inductor must be included since the RF outputs are open-collector type. The TRC101 may also drive a single ended 50 Ohm load, such as a monopole antenna, using the matching circuit as shown in Figure 1. Use of a balun would provide an optimum power transfer, but the matching circuit of Figure 1 has been optimized for use with discrete components, reducing the cost associated with use of a balun. The matching component values for a 50 Ohm load for each band are given in Table 2.

Table 2.

Ref Des	315	433	868	916
C1	6.8pF	5.1pF	2.7pF	2.7pF
C2	3.9pF	2.7pF	1.2pF	1.2pF
C4	.1uF	.1uF	.1uF	.1uF
C7	100pF	100pF	100pF	100pF
L1	56nH	33nH	8.2nH	8.2nH
L2	390nH	390nH	100nH	100nH
L3	68nH	47nH	22nH	22nH

Antenna Design Considerations

The TRC101 is designed to drive a differential output such as a Dipole antenna or a Loop. The loop antenna is ideally suited for applications where compact size is required. The dipole is typically not an attractive option for compact designs due to its inherent size at resonance and distance needed away from a ground plane to be an efficient antenna. A monopole antenna can be used with the addition of a balun or by using the matching circuit in Figure 1.

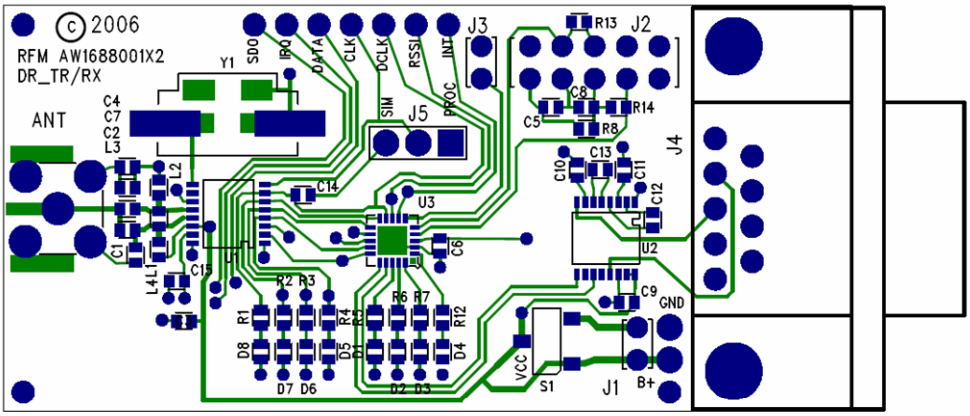
PCB Layout Considerations

Optimal PCB layout is very critical. For optimal transmit and receive performance, the trace lengths at the RF pins must be kept as short as possible. Using small, surface mount components, like 0402 or 0603, will yield the best performance as well as keep the RF port compact. Make all RF connections short and direct. A good rule of thumb to adhere to is add 1nH of series inductance for every 0.1" of trace length.

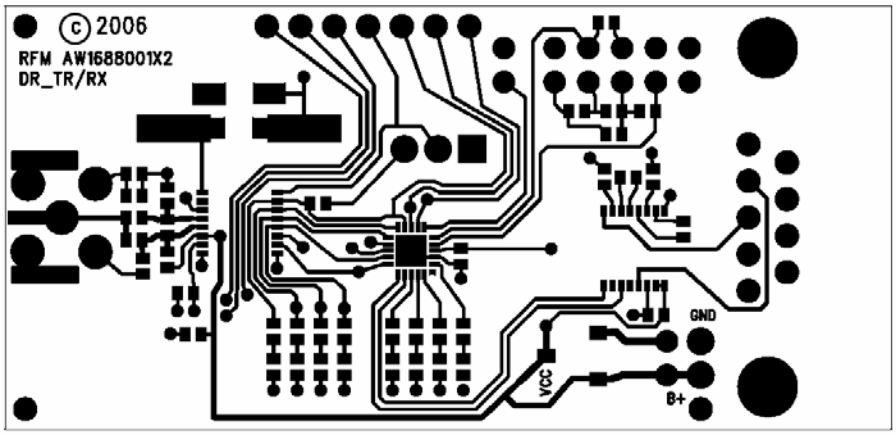
The crystal oscillator is also affected by additional trace length as it adds parasitic capacitance to the overall load of the crystal. To minimize this effect place the crystal as close as possible to the chip and make all connections short and direct. This will minimize the effects of "frequency pulling" that stray capacitance may introduce and allows the internal load capacitance of the chip to be more effective in properly loading the crystal oscillator circuit.

If using an external processor, the TRC101 provides an on-chip clock for that purpose. Even though this is an integrated function, long runs of the clock signal may radiate and cause interference. This can degrade receiver performance as well as add harmonics or unwanted modulation to the transmitter. Keep clock connections as short as possible and surround the clock trace with an adjacent ground plane pour where needed. This will help in reducing any radiation or crosstalk due to long runs of the clock signal.

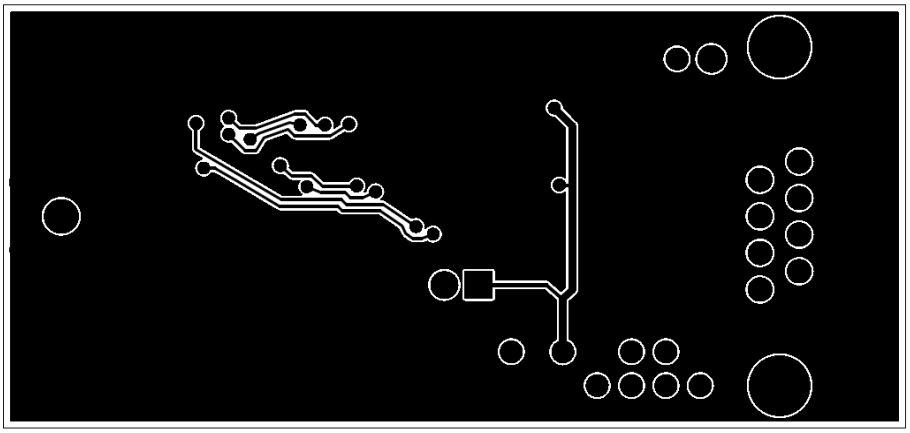
Good power supply bypassing is also essential. Large decoupling capacitors should be placed at the point where power is applied to the PCB. Smaller value decoupling capacitors should then be placed at each power point of the chip as well as bias nodes for the RF port. Poor bypassing lends itself to conducted interference which can cause noise and spurious signals to couple into the RF sections, significantly reducing performance.



Assembly View



Top Side



Bottom Side

3. TRC101 Functional Characteristics

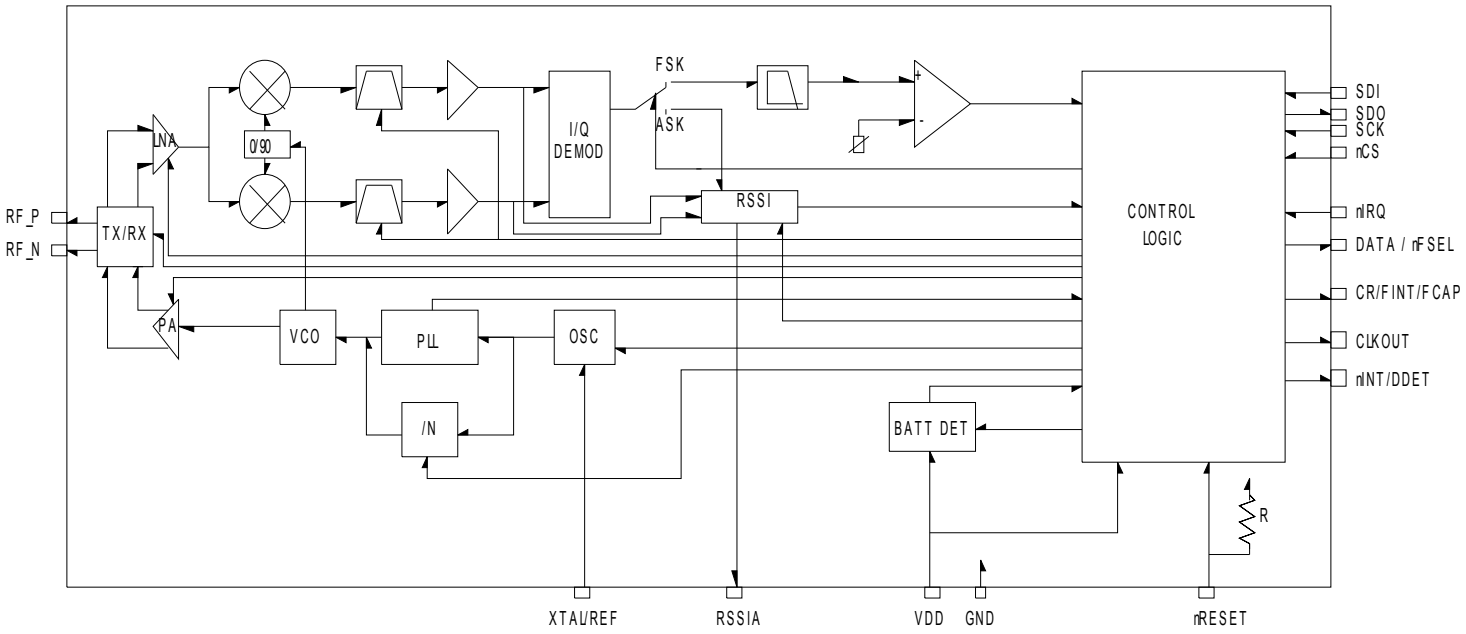


Figure 2. Functional Block Diagram

Input/Output Amplifier

The output power amplifier is an open-collector, differential output with programmable output power which can directly drive a loop or dipole antenna, and with proper matching may also drive a monopole antenna. Incorporated in the power amplifier is an automatic antenna tuning circuit to avoid manual tuning during production and to offset “hand effects”. Registers common to the Power Amplifier are:

- *Power Management Register*
- *Transmit Configuration Register*

The input LNA has selectable gain (0dB, -6dB, -14dB, -20dB) which may be useful in an environment with strong interferers. The LNA has a 250ΩOhm differential input impedance which requires a matching circuit when connected to 50 Ohm devices. Registers common to the LNA are:

- *Power Management Register*
- *Receiver Control Register*

Baseband Data and Filtering

The baseband receiver has several programmable options that optimize the data link for a wide range of applications. The programmable functions include:

- Receive bandwidth
- Receive data rate
- Baseband Analog Filter
- Baseband Digital Filter
- Clock Recovery (CR)
- Receive FIFO
- Data Quality Detector
- Valid Data Detector

The receive bandwidth is programmable from 67kHz to 400kHz to accommodate various FSK modulation deviations. If the deviation is known for a given transmitter, the best results are obtained with a bandwidth at least twice the transmitter FSK deviation.

The receive data rate is programmable from 337bps to 256kbps. An internal prescaler is used to give better resolution when setting up the receive data rate. The prescaler is optional and may be disabled through the *Data Rate Setup Register*.

The type of baseband filtering is selectable between an Analog filter and a Digital filter. The analog filter is a simple RC lowpass filter. An external capacitor may be chosen depending on the actual data rate. The chip has an integrated 10K Ohm resistor in series that makes the RC lowpass network. With the analog filter selected, a maximum data rate of 256kbps can be achieved. The digital filter is used with a clock frequency of 29X data rate. In this mode a clock recovery (CR) circuit is used to provide for a synchronized clock source to recover the data using an external processor. The CR has three modes of operation: fast, slow, and automatic, all configurable through the *Baseband Filter Register*. The CR circuit works by sampling the preamble on the incoming data. The preamble must contain a series of 1's and 0's in order for the CR circuit to properly extract the data timing. In slow mode the CR circuit requires more sampling (12 to 16 bits) and thus has a longer settling time before locking. In fast mode the CR circuit takes fewer samples (6 to 8 bits) before locking so settling time is not as long and timing accuracy is not critical. In automatic mode the CR circuit begins in fast mode to coarsely acquire the timing period with fewer samples and then changes to slow mode after locking. Further details of the CR and data rate clock are provided in the *Baseband Filter Register*. CR is only used with the digital filter and data rate clock. These are not used when configured for the analog filter.

Transmit Register

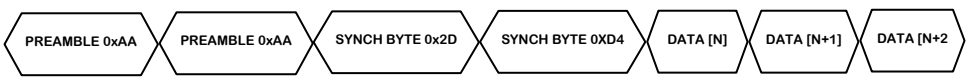
The transmit register is configured as two 8-bit shift registers connected in series to form a single 16-bit shift register. On POR the registers are filled with the value AAh. This can be used to generate a preamble before sending actual data, however, the value is not reloaded when the transmit register is re-enabled. When the transmitter is enabled through the *Power Management Register*, transmission begins immediately and the value in the transmit register begins to be sent out. If there is nothing written to the register then it will send out the default value AAh. The next data byte can be loaded via the SPI bus to the transmit register by monitoring the SDO pin for a logic '1' or waiting for an interrupt from the nIRQ pin. After data has been loaded to the transmit register the processor must wait for the next interrupt before disabling the transmitter or the rest of the data left in the register will be lost. Inserting a dummy byte of all 0's is recommended for the last byte of data loaded.

Receive FIFO

The receive FIFO is configured as one 16-bit register. The FIFO can be configured to generate an interrupt after a predefined number of bits have been received. This threshold is programmable from 1 to 16 bits (0..15). It is recommended to set the threshold to at least half the length of the register (8 bits) to insure the external host processor has time to set up before performing a FIFO read. The FIFO read clock (SCK) must be < $f_{XTAL}/4$ or <2.5 MHz for a 10 MHz reference xtal.

The receive FIFO may also be configured to fill only when valid data has been identified. The RXC101 has a synchronous pattern detector that watches incoming data for a particular pattern. When it sees this pattern it begins to store any data that follows. At the same time, if pin 16 is configured for Valid Data Indicator output (See *Receiver Control Register)*, this pin will go 'high' signaling valid data. This can be used to wake up or prepare a host processor for processing data. The internal synchronous pattern is set to 2DD4h and is not configurable.

The receive packet structure when using the synchronous pattern should be:



Any packet sent, whether using the synchronous pattern or not, should always start with a preamble sequence of alternating 1's and 0's, such as 1-0-1-0-1. This corresponds to sending a 0xAA or 0x55. The preamble may be one byte (Fast CR lock) or two bytes (Slow CR lock). The next two bytes should be the synchronous pattern. In this case, data storage begins immediately following the 2nd synch byte. All other following bytes are treated as data.

The FIFO can be read out through the SDO pin only by pulling the nFSEL pin (6) 'Low" which selects the FIFO for read and reading out data on the next SPI clock. The FINT pin (7) will stay active (logic '1') until the last bit has been read out, and it will then go 'low'. This pin may also be polled to watch for valid data. When the number of bits received in the FIFO match the pre-programmed limit, this pin will go active (logic '1') and stay active until the last bit is read out as above. An alternative method of reading the FIFO is through an SPI bus *Status Register* read. The drawback to this is that all interrupt and status bits must be read first before the FIFO bits appear on the bus. This could pose a problem for receiving large amounts of data. The best method is using the SDO pin and the associated FIFO function pins.

Automatic Frequency Adjustment (AFA)

The PLL has the capability to do fine adjustment of the carrier frequency automatically. In this way, the receiver can minimize the offset between transmit and receive frequency. This function may be enabled or disabled through the *Automatic Frequency Adjustment Register*. The range of offset can be programmed as well as the offset value calculated and added to the frequency control word within the PLL to incrementally change the carrier frequency. The chip can be programmed to automatically perform an adjustment or may be manually activated by a strobe signal. This function has the advantage of allowing:

- Low cost lower accuracy crystals to be used
- Increased receiver sensitivity by narrowing the receive bandwidth
- Achieving higher data rates

Crystal Oscillator

The TRC101 incorporates an internal crystal oscillator circuit that provides a 10MHz reference, as well as internal load capacitors. This significantly reduces the component count required. The internal load capacitance is programmable from 8.5pF to 16pF in 0.5pF steps. This has the advantage of accepting a wide range of crystals from many different manufacturers having different load capacitance requirements. Being able to vary the load capacitance also helps with fine tuning the final carrier frequency since the crystal is the PLL reference for the carrier.

An external clock signal is also provided that may be used to run an external processor. This also has the advantage of reducing component count by eliminating an additional crystal for the host processor. The clock frequency is also programmable from eight pre-defined frequencies, each a pre-scaled value of the 10MHz crystal reference. These values are programmable through the *Battery Detect Threshold and Clock Output Register*. The internal clock oscillator may be disabled which also disables the output clock signal to the host processor. When the oscillator is disabled, the chip provides an additional 196 clock cycles before releasing the output, which may be used by the host processor to setup any functions before going to sleep.

Frequency Control (PLL) and Frequency Synthesizer

The PLL synthesizer is the heart of the operating frequency. It is programmable and completely integrated, providing all functions required to generate the carriers and tunability for each band. The PLL requires only a single 10MHz crystal reference source. RF stability is controlled by choosing a crystal with the particular specifications to satisfy the application. This gives the designer the maximum flexibility in performance.

The PLL is able to perform manual and automatic calibration to compensate for changes in temperature or operating voltage. When changing band frequencies, re-calibration must be performed. This can be done by disabling the synthesizer and re-enabling again through the *Power Management Register*. Registers common to the PLL are:

- *Power Management Register*
- *Configuration Register*
- *Frequency Setting Register*
- *Automatic Frequency Adjust Register*
- *Transmit Configuration Register*

Data Quality Detector (DQD)

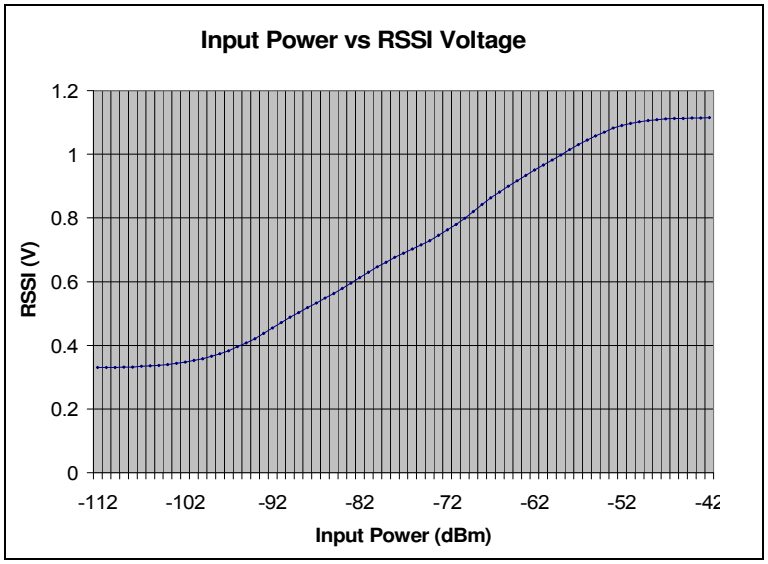
The DQD is a unique function of the TRC101. The DQD circuit looks at the prefiltered incoming data and counts the "spikes" of noise for a predetermined period of time to get an idea of the quality of the link. This parameter is programmable through the *Data Filter Command Register*. The DQD count threshold is programmable from 0 to 7 counts. The higher the count the lower the quality of the data link. This means the higher the content of noise spikes in the data stream the more difficult it will be to recover clock information as well as data.

Valid Data Detector

The DDET is an extension of the DQD. When incoming data is detected, it uses the DQD signal, the Clock Recovery Lock signal, and the Digital RSSI signal to determine if the incoming data is valid. The DDET looks for valid data transitions at an expected data rate. The desired data rate and the acceptance criteria for valid data are user programmable through the SPI port. The DDET signal is valid when using either the internal receive FIFO or an external pin to capture baseband data. The DDET has three modes of operation: slow, medium, fast. Each mode is dependent on what signals it uses to determine valid data as well as the number of incoming preamble bits present at the beginning of the packet. The DDET can be disabled by the user so that only raw data from the comparator comes out, or it can be set to accept only a preset range of data rates and data quality. The DDET saves battery power and time for a host microprocessor because it will not wake up the microprocessor unless there is valid data present. See the *Receiver Control Register* for a detailed description of the setup for valid data.

Receive Signal Strength Indicator (RSSI)

The TRC101 provides an analog RSSI and a digital RSSI. The digital RSSI threshold is programmable through the *Receiver Control Register* and is readable through the *Status Register* only. When an incoming signal is stronger than the preprogrammed threshold, the digital RSSI bit in the *Status Register* is set.



The analog RSSI is available through the RSSIA external pin (15). This pin requires an external capacitor which sets the settling time. The analog RSSI may be used to recover OOK/ASK modulated data. The RSSI level is linear with input signal levels between -100 dBm and -55 dBm. The external capacitor value will control the received ASK data rate allowed so choosing a lower value capacitor enables recovery of faster data at the expense of amplitude. Using pin (15) with a sensitive comparator will yield good results.

The analog RSSI is available through and external pin (15). This pin requires an external capacitor which sets the settling time. The analog RSSI may be used to recover ASK modulated data at a low rate on the order of a few thousand bits per sec. The external capacitor value will control the received ASK data rate allowed so choosing a lower value capacitor enables recovery of faster data at the expense of amplitude. Using pin (15) with a sensitive comparator will yield good results.

OOK/ASK Signaling

The RSSI may be used to recover an OOK/ASK signal using an external comparator, capacitively coupled to the RSSI output. Typically, Automatic Gain Control (AGC) is used to reduce the input signal level upon saturation of the RSSI in the presence of strong or near-field ASK signals. The TRC101 does not have an AGC option, however, the input LNA gain is programmable. The output RSSI signal level may be sampled upon enabling of the receiver to test if the signal level is in saturation. If saturation is confirmed, the input LNA gain may be reduced until the RSSI output signal level falls within the RSSI deviation range.

Wake-Up Mode

The TRC101 has an internal wake-up timer that has very low current consumption (1.5uA typical) and may be programmed from 1ms to several days. A calibration is performed to the crystal at startup and every 30 sec thereafter, even if in sleep mode. If the oscillator circuit is disabled the calibration circuit will turn it on briefly to perform a calibration to maintain accurate timing and return to sleep.
The TRC101 also incorporates other power saving modes aside from the wake-up timer. Return to active mode may be initiated from several external events:

- Logic '0' applied to nINT pin (16)
- Low Supply Voltage Detect
- FIFO Fill
- SPI request

If any of these wake-up events occur, including the wake-up timer, the TRC101 generates an external interrupt on the nIRQ pin (5) which may be used as a wake-up signal to a host processor. The source of the interrupt may be read out from the *Status Register* over the SPI bus.

Duty Cycle Mode

The duty cycle register may be used in conjunction with the wake-up timer to reduce the average current consumption of the receiver. The duty cycle register may be set up so that when the wake-up timer brings the chip out of sleep mode the receiver is turned on for a short time to sample if a signal is present and then goes back into sleep and the process starts over. See the *Duty Cycle Set Register*. The receiver must be disabled (RXEN bit 7 cleared in *Power Management Register*) and the wake-up timer must be enabled (WKUPEN bit 1 set in *Power Management Register*) for operation in this mode. Figure 6 shows the timing for Duty Cycle Mode.

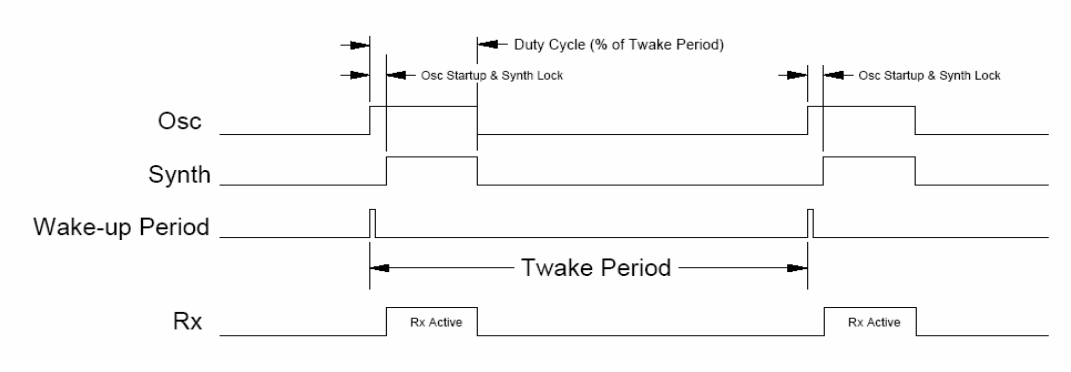


Figure 6. Duty Cycle Mode Timing

Low Battery Detector

The integrated low battery detector monitors the voltage supply against a preprogrammed value and generates an interrupt when the supply voltage falls below the programmed value. The detector circuit has 50mV of hysteresis built in.

SPI Interface

The TRC101 is equipped with a standard SPI bus that is compatible to almost all SPI devices. All functions and status of the chip are accessible through the SPI bus. Typical SPI devices are configured for byte write operations. The TRC101 uses word writes so the nCS pin(3) should be pulled low for 16 bits.

Symbol	Parameter	Minimum Value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nCS falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nCS rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram

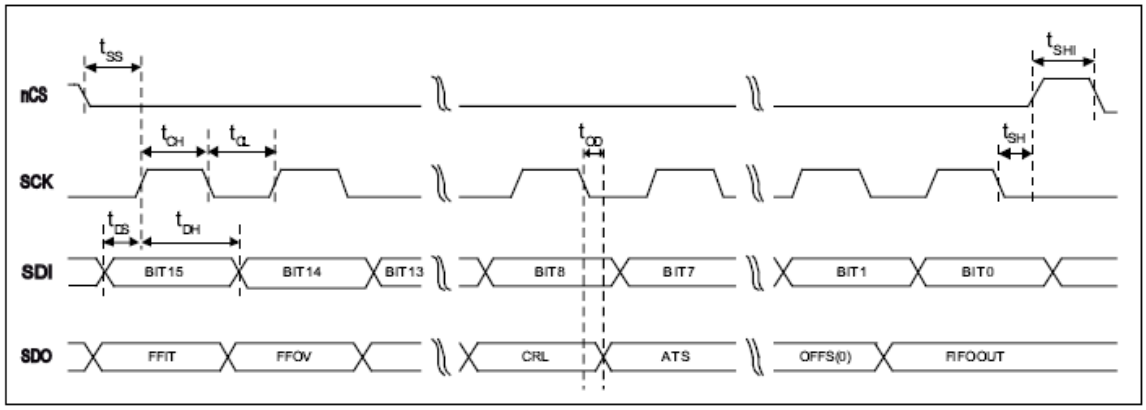


Figure 3. SPI Interface Timing

4. Control and Configuration Registers

	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	POR Value
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
STATUS	FIFTXRX	POR	FIFOV/UR	WKINT	INTRST	LB	FIFEMP	RSSI/AT	GDQD	CRLK	AFATGL	OFFSGN	OFF3	OFF2	OFF1	OFF0	- -
CONFIG	1	0	0	0	0	0	0	0	DATEN	FIFEN	BAND1	BAND0	CAP3	CAP2	CAP1	CAP0	8008h
AFA	1	1	0	0	0	1	0	0	AUTO1	AUTO0	RNG1	RNG0	STRB	ACCF	OFFEN	AFEN	C4F7h
TX CONFIG	1	0	0	1	1	0	0	MODP	DEV3	DEV2	DEV1	DEV0	0	PWR2	PWR1	PWR0	9800h
TX REG	1	0	1	1	1	0	0	0	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	B8AAh
FREQ SET	1	0	1	0	Freq11	Freq10	Freq9	Freq8	Freq7	Freq6	Freq5	Freq4	Freq3	Freq2	Freq1	Freq0	A680h
RECV CTRL	1	0	0	1	0	INT/VDI	VDIR1	VDIR0	BB2	BB1	BB0	GAIN1	GAIN0	RSSI2	RSSI1	RSSI0	9080h
BASEBAND	1	1	0	0	0	0	1	0	CRLK	CRLC	1	FILT	1	DQLVL2	DQLVL1	DQLVL0	C22Ch
FIFO READ	1	0	1	1	0	0	0	0	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	B000h
FIFO/RESET CONFIG	1	1	0	0	1	0	1	0	FINT3	FINT2	FINT1	FINT0	0	FIFST	FILLEN	RSTEN	CA80h
DATA RATE SET	1	1	0	0	0	1	1	0	PRE	BITR6	BITR5	BITR4	BITR3	BITR2	BITR1	BITR0	C623h
POWER MANAGEMENT	1	0	0	0	0	0	1	0	RXEN	BBEN	TXEN	SYNEN	OSCEN	LBDEN	WKUPEN	CLKEN	8208h
WAKE-UP PERIOD	1	1	1	R4	R3	R2	R1	R0	MUL7	MUL6	MUL5	MUL4	MUL3	MUL2	MUL1	MUL0	E196h
DUTY CYCLE SET	1	1	0	0	1	0	0	0	DC6	DC5	DC4	DC3	DC2	DC1	DC0	DCEN	C80Eh
BATT DETECT	1	1	0	0	0	0	0	0	CLK2	CLK1	CLK0	LBD4	LBD3	LBD2	LBD1	LBD0	C000h

Status Register (Read Only)

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFTXRX	POR	FIFOV/UR	WKINT	INTRST	LB	FIFEMP	RSSI/AT	GDQD	CRLCK	AFATGL	OFFSGN	OFF3	OFF2	OFF1	OFF0

The Status Register provides feedback for:

- FIFO ready/full/empty/under run/overwrite
- POR
- Interrupt state
- Low Battery
- Good Data Quality
- Digital RSSI signal level
- Clock Recovery
- Frequency Offset value and sign
- AFA

Note: The Status Register read command begins with a logic '0' where all other register commands begin with a logic '1'.

Bit [15]:FIFTXRX – When set, indicates the transmit register is ready to receive the next byte for transmission (Transmit Mode) or that the Rx FIFO has reached the preprogrammed limit (Receive Mode). This bit is multiplexed and dependent on whether you are in the respective Transmit or Receive mode. (Cleared when FIFO read).

Bit [14]:POR – When set, Power-on Reset occurred. (Cleared after Status Reg read).

Bit [13]:FIFOV/UR – When set, indicates transmit register under run or register overwrite (Transmit Mode) or receive FIFO overflow (Receive Mode). (Cleared after Status Reg read).

Bit [12]:WKINT – When set, indicates a Wake-up timer overflow. (Cleared after Status Reg read).

Bit [11]:EXINT – When set, indicates a High to Low logic level change on interrupt pin (pin 16). (Cleared after Status Reg read).

Bit [10]:LB – When set, indicates the supply voltage is below the preprogrammed limit. See Battery Detect Threshold and Clock Output Register.

Bit [9]:FIFEMP – When set, indicates receive FIFO is empty.

Bit [8]:RSSI(Rx) – When set and chip in receive mode, this bit indicates that the incoming RF signal is above the preprogrammed Digital RSSI limit.

AT(TX) – When in transmit mode this bit indicates that the antenna tuning circuit has detected a strong enough RF signal.

Bit [7]:GDQD – When set, indicates good data quality.

Bit [6]:CRLCK – When set, indicates Clock Recovery is locked.

Bit [5]:AFATGL – For each AFC cycle run, this bit will toggle between logic '1' and logic '0'.

Bit [4]:OFFSGN – Indicates the difference in frequency is higher (logic '1') or lower (logic '0') than the chip frequency.

Bit [3..0]:OFF[3..0] – The offset value to be added to the frequency control word (internal PLL). In order to get accurate values the AFA has to be disabled during the read by clearing the "AFEN" bit in the AFA Register (bit 0).

To read the status register, initiate a command beginning with a '0' and read the remaining bits on the SDO line. All other commands begin with a '1' so the TRC101 recognizes a command vs. status. See figure 4 for timing reference.

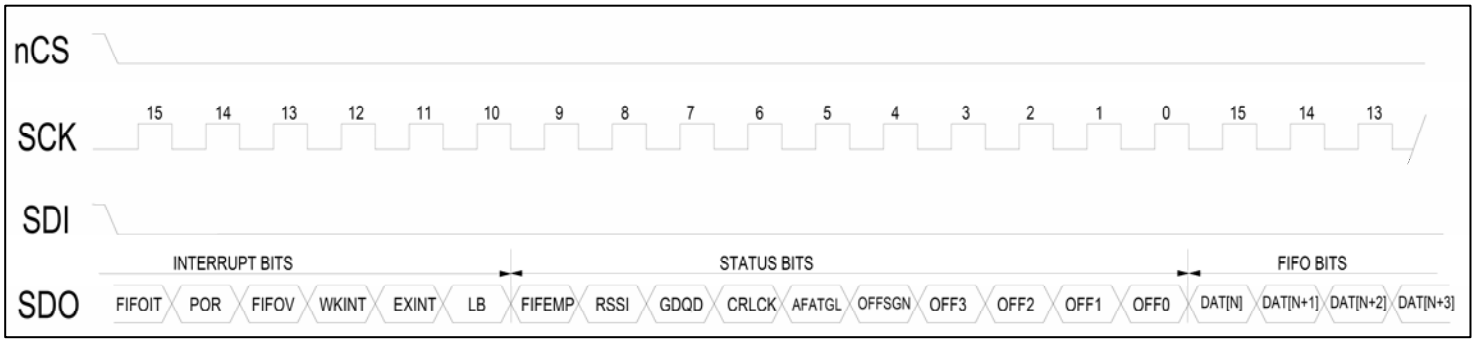


Figure 4. Status Read Timing

Configuration Register [POR=8008h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0	DATEN	FIFEN	BAND1	BAND0	CAP3	CAP2	CAP1	CAP0

The configuration register sets up the following:

- Internal Data Register
- Internal FIFO
- Frequency Band in use
- Crystal Load capacitance

Bit [15..8] – Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the configuration register.

Bit [7] – TX Data Register Enable: This bit enables the internal TX data register when set. If the internal TX data register is used, the DATA/nFSEL pin (6) must be pulled "High".

Bit [6] – FIFO Enable: This bit enables the internal data FIFO when set. If the data FIFO is enabled, the DATA/nFSEL pin (6) must be pulled "Low". The FIFO is used to store data during receive. If the FIFO is disabled by clearing this bit, pin 6 (Data) and pin 7 (Recovered Clock) are used to receive data.

Bit [5..4] – Band Select: These bits set the frequency band to be used. There are four (4) bands that are supported. See Table 3 below for Band configuration.

TABLE 3.

Frequency Band	BAND1	BAND0
315	0	0
433	0	1
868	1	0
916	1	1

Bit [3..0] – Load Capacitance Select: These bits set the load capacitance for the crystal reference. The internal load capacitance can be varied from 8.5pF to 16pF in 0.5pF steps to accommodate a wide range of crystal vendors as well as adjust the reference frequency and compensate for stray capacitance that may be introduced due to PCB layout. See Table 4 below for load capacitance configuration.

TABLE 4.

CAP3	CAP2	CAP1	CAP0	Crystal Load Capacitance
0	0	0	0	8.5
0	0	0	1	9
0	0	1	0	9.5
0	0	1	1	10
0	1	0	0	10.5
0	1	0	1	11
0	1	1	0	11.5
0	1	1	1	12
1	0	0	0	12.5
1	0	0	1	13
1	0	1	0	13.5
1	0	1	1	14
1	1	0	0	14.5
1	1	0	1	15
1	1	1	0	15.5
1	1	1	1	16

Automatic Frequency Adjust Register [POR=C4F7h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	1	0	0	AUTO1	AUTO0	RNG1	RNG0	STRB	ACCF	OFFEN	AFEN

The AFA (Automatic Frequency Adjust) Register configures:

- Manual or Automatic frequency offset adjustment
- Calculation of the offset value and write to the Status Register
- Fine offset adjustment control

The AFA (Automatic Frequency Adjust) Register controls and configures the frequency adjustment range and mode for keeping the transmitter and receiver frequency locked, providing for an optimal link. The AFA may be manually controlled by an external processor by asserting a strobe signal to initiate a sample, or may be setup for automatic operation, which uses the Valid Data Detector (VDI) signal to initiate a frequency adjustment. When the VDI goes active, the AFA circuit performs a sample and updates the offset register automatically. The elapsed time for an AFA is determined by the setting of the clock recovery (CR) bit in the *Baseband Filter Register*. The AFA also calculates the offset of the transmit and receive frequency. This offset value is included in the status register read and the AFA must be disabled during the status read to ensure reporting good offset accuracy.

Bit [15..8] - Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Automatic Frequency Adjust Register.

Bit [7..6] – Mode Selection: These bits select Automatic or Manual operation. When set to Manual operation, the TRC101 will take a sample when a strobe signal (See Bit [3]) is written to the register. There are four modes of operation. See Table 5 below for configuration.

TABLE 5.

Automatic fOFFSET Mode	AUTO1	AUTO0
Mode Off	0	0
Run Once after Pwr-up	0	1
Keep offset during Rcv ONLY	1	0
Keep offset indep of VDI state	1	1

Mode(0,1) – The circuit takes a measurement only once after power-up.

Mode(1,0) – When the Valid Data Detector (VDI) pin is low, indicating poor receiving conditions, the offset register is automatically cleared. Use this setting when receiving from several different transmitters that are operating very close to the same frequencies so that the receiver may align itself on each transmission from a different transmitter.

Mode(1,1) – This setting is best used when receiving from a single transmitter. The measured offset value is kept independent of the state of the VDI signal. Once the link is aligned it may be manually toggled by the user.

Bit [5..4] – Allowable Frequency Offset: These bits select the amount of offset allowable between Transmitter and Receiver frequencies. The allowable range can be specified as in Table 6 below.

TABLE 6.

Freq Offset Range	RNG1	RNG0
No Limit	0	0
+15*fres/-16*fres	0	1
+7*fres /-8*fres	1	0
+3*fres /-4*fres	1	1

where fres is the tuning resolution for each band as follows:

fres: 315 MHz Band = 2.5kHz
433 MHz Band = 2.5kHz
868 MHz Band = 5kHz
916 MHz Band = 7.5kHz

Bit [3] – Manual Frequency Adjustment Strobe: This bit is the strobe signal that initiates a manual frequency adjustment sample. When set, a sample of the received signal is compared to the Receiver LO signal and an offset is calculated. If enabled, this value is written to the Offset Register (See Bit [1]) and added to the frequency control word of the PLL. This bit MUST be reset before initiating another sample.

Bit [2] – High Accuracy (Fine) Mode: This bit, when set, switches the frequency adjustment mode to high accuracy. In this mode the processing time is twice the regular mode, but the uncertainty of the measurement is significantly reduced.

Bit [1] – Frequency Offset Register Enable: This bit, when set, enables the offset value calculated by the offset sample to be added to the frequency control word of the PLL that tunes the desired carrier frequency.

Bit [0] – Offset Frequency Enable: This bit, when set, enables the TRC101 to calculate the offset frequency by the sample taken from the Automatic Frequency Adjustment circuit.

Transmit Configuration Register [POR=9800h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	1	0	0	MODP	DEV3	DEV2	DEV1	DEV0	0	PWR2	PWR1	PWR0

The Transmit Configuration Register configures:

- Modulation Polarity
- Modulation Bandwidth
- Output Transmit Power

Bit [15..9] - Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Transmit Configuration Register.

Bit [8] – Modulation Polarity: When clear, a logic '0' is defined as the lower channel frequency and a logic '1' as the higher channel frequency (positive deviation). When set, a logic '0' is defined as the higher channel frequency and a logic '1' as the lower channel frequency (negative deviation).

Bit [7..4] – Modulation Bandwidth: These bits set the FSK frequency deviation for transmitting a logic '1' and logic '0'. The deviation is programmable from 15kHz to 240kHz in 15kHz steps. See Table 7 below for deviation settings.

TABLE 7.

Modulation Bandwidth	Hex	DEV3	DEV2	DEV1	DEV0
15 kHz	0	0	0	0	0
30 kHz	1	0	0	0	1
45 kHz	2	0	0	1	0
60 kHz	3	0	0	1	1
75 kHz	4	0	1	0	0
90 kHz	5	0	1	0	1
105 kHz	6	0	1	1	0
120 kHz	7	0	1	1	1
135 kHz	8	1	0	0	0
150 kHz	9	1	0	0	1
165 kHz	A	1	0	1	0
180 kHz	B	1	0	1	1
195 kHz	C	1	1	0	0
210 kHz	D	1	1	0	1
225 kHz	E	1	1	1	0
240 kHz	F	1	1	1	1

Bit [3] – Not used. Write as logic '0'.

Bit [2..0] – Output Transmit Power: These bits set the transmit output power. The output power is programmable from Max to -21dB in -3dB steps. See Table 8 below for Output Power settings.

TABLE 8.

Output Power (Relative)	PWR2	PWR1	PWR0
Max	0	0	0
-3dB	0	0	1
-6dB	0	1	0
-9dB	0	1	1
-12dB	1	0	0
-15dB	1	0	1
-18dB	1	1	0
-21dB	1	1	1

Transmit Register [POR=B8AAh]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	0	0	0	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0

The *Transmit Register* holds the 8 bits to be transmitted. Bit [7] of the Configuration Register must be set (logic '1') in order to use this. If Bit [7] is not set, use pin 6 to manually modulate the data.

The initial value on power-up of the register is AAh. This can be used to send a preamble signal by setting Bit [5] of the *Power Management Register* (See Figure 5 below). When this bit is set, transmission begins immediately and the initial value AAh is sent. The SDO pin(4) may be monitored to see when the next byte of data may be written to the register (SDO is logic '1'). It is recommended that the register be preloaded with a preamble regardless of the POR value.

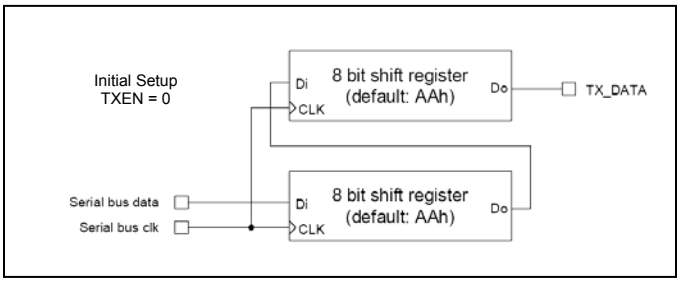


FIGURE 5. Initial TX Register Setting

Bit [15..8] - Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Transmit Register.

Bit [7..0] – Transmit Byte: The data byte to be sent is written here. As soon as the power amplifier is enabled the data byte is sent. The SDO pin(4) may be monitored to determine when the byte has been sent.

Sequential Byte Write Method (Recommended)

The transmit register may be continuously accessed by holding the nCS pin (3) 'Low" for the duration of the data stream. On the first falling edge of nCS the register command should be issued as normal. Sequential byte writes to the register afterwards will load the transmit register directly without having to re-issue the command byte. The SDO pin (4) may be used as a "Transmit Register Empty" flag to write the next byte. Figure 6 shows the timing sequence.

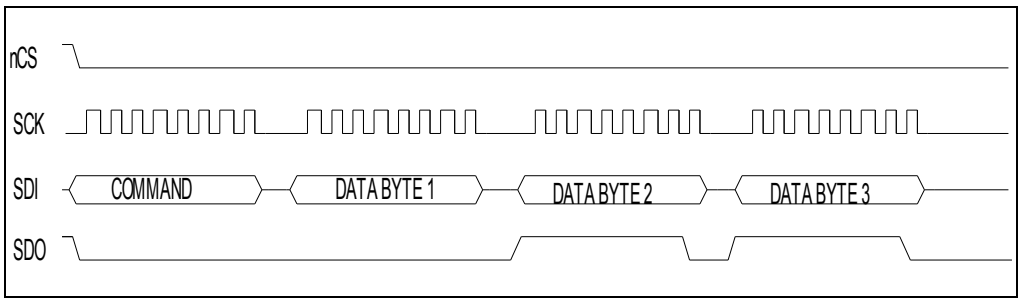


Figure 6. Sequential Byte Write Timing

Frequency Setting Register [POR=A680h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	Freq11	Freq10	Freq9	Freq8	Freq7	Freq6	Freq5	Freq4	Freq3	Freq2	Freq1	Freq0

The *Frequency Setting Register* sets the exact frequency within the selected band for transmit or receive. Each band has a range of frequencies available for channelization or frequency hopping. The selectable frequencies for each band are:

Frequency Band	Min (MHz)	Max (MHz)	Tuning Resolution
300 MHz	310.24	319.75	2.5 kHz
400 MHz	430.24	439.75	2.5 kHz
800 MHz	860.48	879.51	5.0 kHz
900 MHz	900.72	929.27	7.5 kHz

Bit [15..12] – Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the *Frequency Setting Register*.

Bit [11..0] – Frequency Setting: These bits set the center frequency to be used during transmit or receive. The value of bits[11..0] must be in the decimal range of 96 to 3903. Any value outside of this range will cause the previous value to be kept and no frequency change will occur. To calculate the center frequency fc, use Table 9 below and the following equation:

$$f_c = 10 * B1 * (B0 + f_{VAL}/4000) \text{ MHz}$$

where f_{VAL} = decimal value of Freq[11..0] = $96<f_{VAL}<3903$.

TABLE 9.

Range	B1	B0
315 MHz	1	31
433 MHz	1	43
868 MHz	2	43
916 MHz	3	30

Receiver Control Register [POR=9080h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	INT/VDI	VDIR1	VDIR0	BB2	BB1	BB0	GAIN1	GAIN0	RSSI2	RSSI1	RSSI0

The *Receiver Control Register* configures the following:

- Receiver LNA gain
- Digital RSSI threshold
- Receive baseband bandwidth
- Valid Data Detector response time
- Function of pin 16

Bit [15..11] – Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the *Receiver Control Register*.

Bit [10] – Pin 16 Func: Selects the function of Pin 16. See Table 10 below.

Table 10.

Pin 16 Function	INT/VDI
Interrupt Input	0
Valid Data Output	1

Bit [9..8] – Valid Data Detector Response Time: When Pin 16 is selected as Valid Data Detector output these bits set the response time in which the TRC101 will detect the incoming synchronous bit pattern and issue an interrupt to the host processor. See Table 11 below for response settings.

Table 11.

VDI Response Time	VDIR1	VDIR0
Fast	0	0
Mid	0	1
Slow	1	0
Continuous	1	1

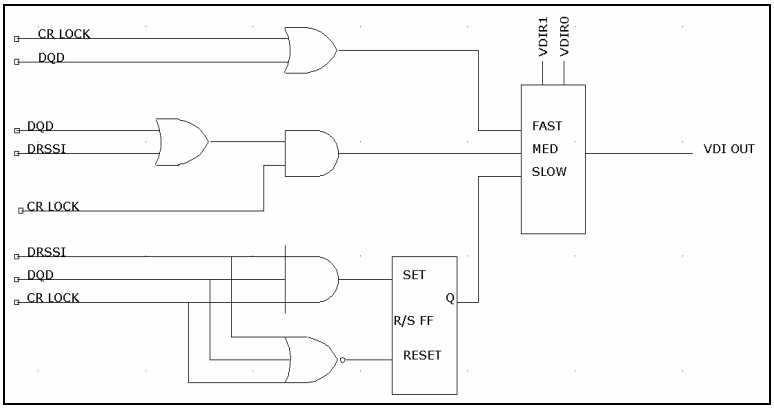


Figure 7. VDI Signal Response Configuration

Receiver Control Register (continued)

Bit [7..5] – Receiver Baseband Bandwidth: These bits set the baseband bandwidth of the demodulated data. The bandwidth can accommodate different FSK deviations and data rates. See Table 12 for bandwidth configuration.

Table 12.

Baseband BW (kHz)	BB2	BB1	BB0
Resvd	0	0	0
400	0	0	1
340	0	1	0
270	0	1	1
200	1	0	0
134	1	0	1
67	1	1	0
Reserved	1	1	1

Bit [4..3] – Receiver LNA Gain: These bits set the receiver LNA gain, which can be changed to accommodate environments with high interferers. The LNA gain also affects the true RSSI value. Refer to Bit [2..0] for RSSI. See Table 13 below for gain configuration.

Table 13.

LNA GAIN (dB)	GAIN1	GAIN0
0	0	0
-6	0	1
-14	1	0
-20	1	1

Bit [2..0] – Digital RSSI Threshold: The digital receive signal strength indicator threshold may be set to indicate that the incoming signal strength is above a preset limit. The result is stored in bit 7 of the status register. There are eight (8) predefined thresholds that can be set. See Table 14 below for settings.

Table 14.

RSSI Thresh	RSSI2	RSSI1	RSSI0
-103	0	0	0
-97	0	0	1
-91	0	1	0
-85	0	1	1
-79	1	0	0
-73	1	0	1
Resvd	1	1	0
Resvd	1	1	1

The RSSI threshold is affected by the LNA gain set value. Calculate the true RSSI set threshold when the LNA gain is set to a value other than 0 dB as:

$$RSSI = RSSIthres + |GainLNA|$$

Baseband Filter Register [POR=C22Ch]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	1	0	CRLK	CRLC	1	FILT	1	DQLVL2	DQLVL1	DQLVL0

The Baseband Filter Register configures:

- Clock Recovery lock control
- Baseband Filter type, Digital or Analog RC
- Data Quality Detect Threshold parameter

Bit [15..8] - Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Baseband Filter Register.

Bit [7] – Automatic Clock Recovery Lock: When set, this bit configures the CR (clock recovery) lock control to automatic. In this setting the clock recovery will startup in "Fast" mode and automatically switch to "Slow" mode after locking. See Bit [6] description for details of "Fast" and "Slow" modes.

Bit [6] – Manual Clock Recovery Lock Control: When set, this bit configures the CR lock to "Fast" mode. "Fast" mode requires a preamble of at least 6 to 8 bits to determine the clock rate, then locks. When cleared, this bit configures the CR lock to "Slow" mode. "Slow" mode takes a little longer in that it requires a preamble of at least 12 to 16 bits to determine the clock rate, then locks. Use of the "Slow" mode requires more accurate bit timing. See Data Rate Setup Register for the relationship of data rate and CR.

Bit [5] – Not Used. Write a "1".

Bit [4] – Filter Type: When clear, this bit configures the baseband filter as a Digital filter. The Digital filter is a digital version of a simple RC lowpass filter followed by a comparator with hysteresis. The time constant for the Digital filter is automatically calculated internally based on the bit rate as set in the Data Rate Setup Register.

When set, this bit configures the baseband filter as an Analog RC lowpass filter. The baseband signal is fed to pin 7 thru an internal 10K Ohm resistor. The lowpass cutoff frequency is set by the external capacitor connected from pin 7 to GND. To calculate the baseband capacitor value for a given data rate, use:

Filter Type	FILT (Bit 4)
Digital	0
Analog	1

$$C_{FILT} = 1 / (30{,}000 * \text{Data Rate})$$

Bit [3] - Not Used. Write a "1".

Bit [2..0] – Data Quality Detect Threshold: The threshold parameter should be set less than four (<4) in order for the Data Quality Detector to report good signal quality in the case that the bit rate is close to the deviation. As the data rate << deviation, a higher threshold parameter is permitted and may report good signal quality.

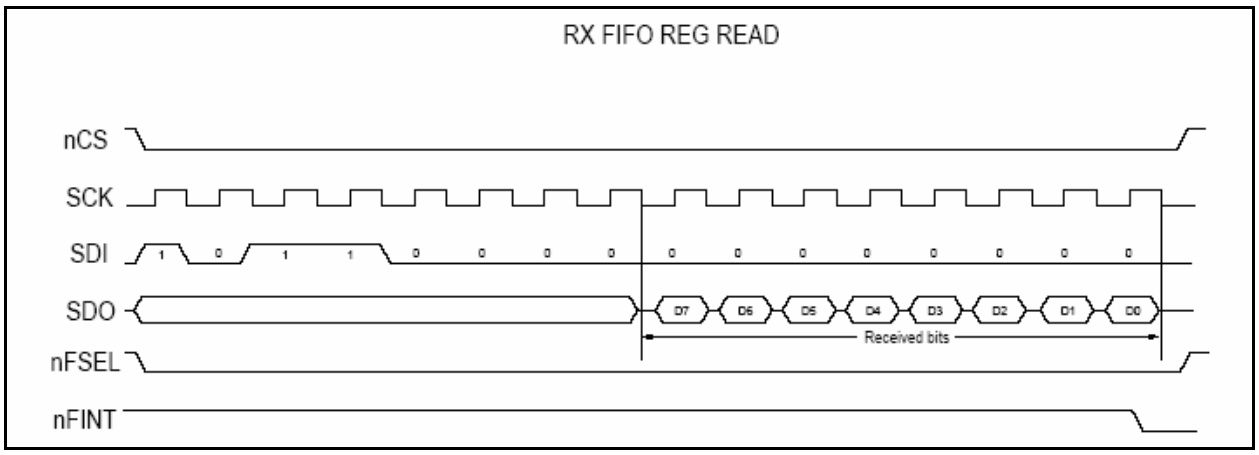
FIFO Read Register [POR=B000h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0

The FIFO Read Register stores the received data and can be read out by the host processor. The FIFO must be enabled by setting Bit[6] of the *Configuration Register*.

Bit [15..8] - Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the *Data FIFO Configuration Register*.

Bit [7..0] – FIFO Data Bits: These bits are the recovered data bits stored in the FIFO. These bits may be read out over the SPI bus.



*Alternate Read Method

A faster method of reading the internal FIFO is recommended. The Rx FIFO is directly accessible by using the nFSEL select pin (6) and monitoring the FINT interrupt pin (7) for pending data. Each data bit may be clocked in on the rising edge of SCK.

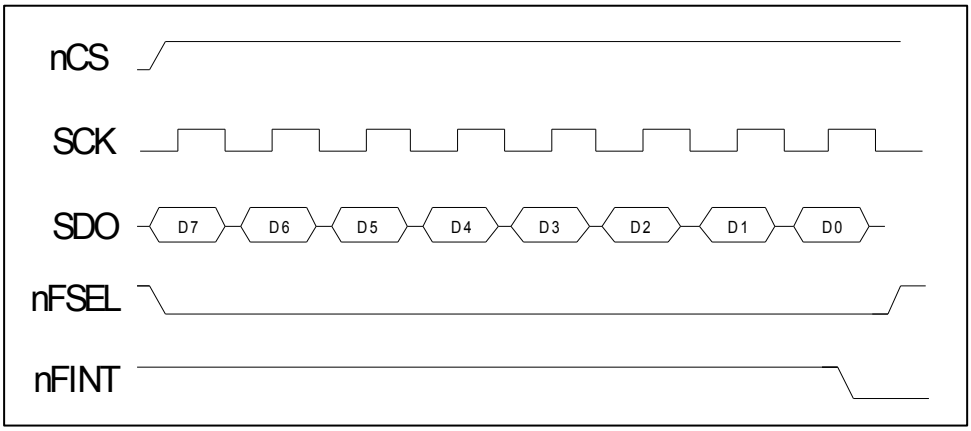


Figure 8. Recommended FIFO Read Method Timing

***NOTE: The internal FIFO cannot be accessed faster than $f_{XTAL}/4$ when reading the FIFO or data errors will occur. For a 10MHz ref xtal the max SCK <2.5MHz.**

FIFO and RESET Mode Configuration Register [POR=CA80h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	1	0	FINT3	FINT2	FINT1	FINT0	0	FIFST	FILLEN	RSTEN

The Data FIFO Configuration Register configures:

- FIFO fill interrupt condition
- FIFO fill start condition
- FIFO fill on synchronous pattern
- RESET Mode

Bit [15..8] - Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Data FIFO Configuration Register.

Bit [7..4] – FIFO Fill Bit Count: This sets the number of bits that are received before generating an external interrupt to the host processor that the receive FIFO data is ready to be read out. It is possible to set the maximum fill level to 15, but the designer must account for the processing time it will take to read out the data before a register overrun occurs, at which data will be lost. It is recommended to set the fill value to half of the desired number of bits to be read to ensure enough time for additional processing. See Status Register for description of FIFO status bits that may be read and FIFO Read Register for polling and interrupt-driven FIFO reads from the SPI bus.

Bit [3] – Not Used. Write a "0".

Bit [2] – FIFO Fill Start Condition: This bit sets the condition at which the FIFO begins filling with data. When set, the FIFO will continuously fill regardless of noise or good data. When clear, the FIFO will fill when it recognizes the synchronous pattern as defined internally. The internal pattern is 2DD4h.

Note: This pattern is not configurable and is not accessible to a host processor.

Bit [1] – Synchronous Pattern FIFO Fill: When set, the FIFO will begin filling with data when it detects the synchronous pattern as defined in Bit [2]. The FIFO fill stops when this bit is cleared. To restart the synchronous pattern recognition, simply clear the bit and set again.

Note: Clearing this bit will issue a FIFO reset. See Figure 9 for FIFO write and reset configuration.

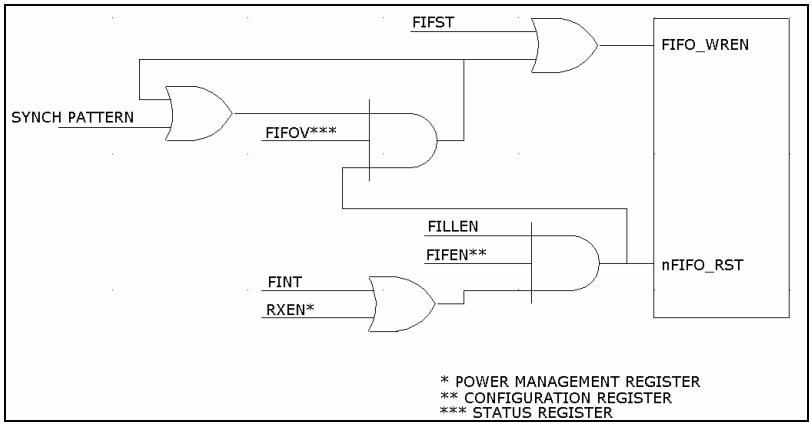


Figure 9. FIFO Write and Reset Configuration

Bit [0] – Disable RESET Mode: When cleared, if the TRC101 encounters a 0.2V spike in the power supply, the glitch could cause a system reset. When set, this mode is disabled.

Data Rate Setup Register [POR=C623h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	1	1	0	PRE	BITR6	BITR5	BITR4	BITR3	BITR2	BITR1	BITR0

The Data Rate Setup Register configures:

- Expected data rate for the receiver
- Prescaler
- Effects of the data rate on clock recovery

Bit [15..8] - Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Data Rate Setup Register.

Bit [7] – Prescaler Enable: When set this bit enables the prescaler to obtain smaller values of expected data rates. The prescaler value is approximately 1/8.

Bit [6..0] – Data Rate Parameter Value: These bits represent the decimal value of the 7-bit parameter used to calculate the expected data rate. To calculate the expected data rate, use the following formula:

$$DR_{exp}(kbps) = 10000 / [29 * (BITR[6..0]+1) * (1+PRE*7)]$$

where BITR[6..0] is the decimal value 0 to 127 and the prescaler (PRE) is ‘1’ (on) or ‘0’ (off).

To calculate the BITR[6..0] decimal value for a given bit rate, use the following formula:

$$BITR[6..0] = 10000 / [29 * (1+PRE*7) * DR_{exp}] -1$$

where DRexp is the expected data rate and PRE is defined above.

Without the prescaler, the definable data rates range from 2.694kpbs to 344.828kbps. With the prescaler enabled, the definable data rates range from 337 bps to 43.103kpbs.

The Slow clock recovery mode requires more accurate bit timing when setting the data rate. To calculate the accuracy of the data rate for both Fast and Slow mode, use the following:

$$\text{Slow mode Acc} = \Delta BR/BR < 1/(29 * N) \qquad \text{Fast mode} = \Delta BR/BR < 3/(29 * N)$$

where N is the longest number of expected ones or zeros in the data stream, ΔBR is the difference in the actual data rate vs. the set data rate in the transmitter, and BR is the expected data rate as set above using BITR[6..0].

Power Management Register [POR=8208h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	1	0	RXEN	BBEN	TXEN	SYNEN	OSCEN	LBDEN	WKUPEN	CLKDIS

The Power Management Register enables/disables the following:

- Receiver chain
- Transmit Chain
- Baseband Circuit
- PLL
- Power Amplifier
- Synthesizer
- Crystal Oscillator
- Low battery Detect Circuit
- Wake-up Timer
- Clock Output

Bit [15..8] – Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Power Management register.

Bit [7] – Receiver Chain Enable: This bit enables the entire receiver chain when set. The receiver chain comprises the baseband circuit, synthesizer, and crystal oscillator.

Bit [6] – Baseband Circuit Enable: This bit enables the baseband circuit when set. The baseband circuit, synthesizer, and oscillator work together to demodulate and recover the data transmitted so the synthesizer (Bit 4) and oscillator (Bit 3) must be enabled at the same time as the baseband circuits in order to receive data. This bit can be disabled to conserve current consumption.

Bit [5] – Transmit Chain Enable: This bit enables the entire transmit chain when set. The transmit chain consists of the power amplifier, synthesizer, oscillator, and transmit register. When the transmit chain and transmit register is enabled, any data in the transmit register is shifted out and transmission is started.

Bit [4] – Synthesizer Enable: This bit enables the synthesizer when set. The synthesizer contains the PLL, oscillator, and VCO for controlling the channel frequency. This must be enabled when either the transmitter is enabled or the receiver is enabled. The oscillator also must be enabled to provide the reference frequency for the PLL. On power-up the synthesizer performs a calibration automatically. If there are significant changes in voltage or temperature, recalibration can be performed by simply disabling the synthesizer and re-enabling it.

Bit [3] – Crystal Oscillator: This bit enables the oscillator circuit when set. The oscillator provides the reference signal for the synthesizer when setting the transmit or receive frequency of use.

Bit [2] – Low Battery Detector: This bit enables the battery voltage detect circuit when set. The battery detector can be programmed to 32 different threshold levels. See Battery Detect Threshold and Clock Output Register section for programming.

Bit [1] – Wake-up Timer Enable: This bit enables the wake-up timer when set. See Wake-up Timer Period Register section for programming the wake-up timer interval value.

Bit [0] – Clock Output Disable: This bit disables the oscillator clock output when set. On chip reset or power up, clock output is enabled so that a processor may begin execution of any special setup sequences as required by the designer. See Battery Detect Threshold and Clock Output Register section for programming details.

NOTE: If this bit is cleared, the oscillator will continue to run even though the Crystal Oscillator Enable bit (3) is cleared and the device will not fully enter sleep mode.

Wake-up Timer Period Register [POR=E196h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	R4	R3	R2	R1	R0	M7	M6	M5	M4	M3	M2	M1	M0

The Wake-up Timer Period register sets the wake-up interval for the TRC101. After setting the wake-up interval, the WKUPEN (bit 1 of Power Management Register) should be cleared and set at the end of every wake-up cycle. To calculate the wake-up interval desired, use the following:

$$T_{WAKE}(ms) = M[7..0] * 2^{R[4..0]}$$

where M[7..0] = decimal value 0 to 255 and R[4..0] = decimal value 0 to 31.

Bit [15..13] – Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Wake-up Timer Period register.

Bit [12..8] – Exponential: These bits define the exponential value as used in the above equation. The value used must be the decimal equivalent between 0 and 31.

Bit [7..0] – Multiplier: These bits define the multiplier value as used in the above equation. The value used must be the decimal equivalent between 0 and 255.

Duty Cycle Set Register [POR=C80Eh]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	0	DC6	DC5	DC4	DC3	DC2	DC1	DC0	DCEN

The duty cycle register may be used in conjunction with the wake-up timer to reduce the average current consumption of the receiver. The duty cycle register may be set up so that when the wake-up timer brings the chip out of sleep mode the receiver is turned on for a short time to sample if a signal is present and then goes back into sleep and the process starts over.

The duty cycle uses the Multiplier value of the wake-up timer in part for its calculation. To calculate the duty cycle use:

$$\text{Duty Cycle}(\%) = ((D[6..0] * 2) + 1)/M * 100$$

where M is M[7..0] of the *Wake-up Timer Period Register*.

Bit [15..8] – Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the *Duty Cycle Set Register*.

Bit [7..1] – Duty Cycle Multiplier: These bits are the decimal value used to calculate the Duty Cycle or "On time" of the Receiver after the wake-up timer has brought the TRC101 out of sleep mode.

Bit [0] – Duty Cycle Mode Enable: This bit enables the duty cycle mode when set.

NOTE: The receiver must be disabled (RXEN = '0' in Power *Management Register*) and the wake-up timer must be enabled (WKUPEN = '1' in *Power Management Register*) for operation in this mode.

Battery Detect Threshold and Clock Output Register [POR=C000h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0	CLK2	CLK1	CLK0	LBD4	LBD3	LBD2	LBD1	LBD0

The Battery Detect Threshold and Clock Output Register configures the following:

- Low Battery Detect Threshold
- Output Clock frequency

The Low Battery Threshold is programmable from 2.2V to 5.3V using the following equation:

$$VT = (LBD[4..0] / 10) + 2.2 \ (V)$$

where LBD[4..0] is the decimal value 0 to 31.

Bit [15..8] - Command Code: These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Battery Detect Threshold and Clock Output Register.

Bit [7..5] – Clock Output Frequency: These bit set the output frequency of the on-board clock that may be used to run an external host processor. See Table 15 below.

TABLE 15.

Output Clock Frequency (MHz)	CLK2	CLK1	CLK0
1	0	0	0
1.25	0	0	1
1.66	0	1	0
2	0	1	1
2.5	1	0	0
3.33	1	0	1
5	1	1	0
10	1	1	1

Bit [4..0] – Low Battery Detect Value: These bits set the decimal value as used in the equation above to calculate the value of the battery detect threshold voltage. When the battery level falls 50mV below this value, the LBD bit (5) in the status register is set indicating that the battery level is below the programmed threshold. This is useful in monitoring discharge sensitive batteries such as Lithium cells.

The Low Battery Detect can be enabled by setting the LBDEN bit (2) of the Power Management Register and disabled by clearing the bit.

The Clock Output can be enabled by setting the CLKEN bit (0) of the Power Management Register and disabled by clearing the bit.

5. Maximum Ratings

Absolute Maximum Ratings

Symbol	Parameter	Notes	Min	Max	Units
VDD	Positive supply voltage		-0.5	6	V
Vin	Voltage on any pin (except RF_P and RF_N)		-0.5	Vdd+0.5	V
Voc	Voltage on open collector outputs (RF1, RF2)	1	-0.5	Vdd+1.5	V
Iin	Input current into any pin except VDD and VSS		-25	25	mA
ESD	Electrostatic discharge with human body model			1000	V
Tstg	Storage temperature		-55	125	°C
Tlead	Lead temperature (soldering, max 10 s)			260	°C

Note 1: At maximum, VDD+1.5 V cannot be higher than 7 V.

Recommended Operation Ratings

Symbol	Parameter	Notes	Min	Max	Units
VDD	Positive supply voltage		2.2	5.4	V
VDCRF	DC voltage on open collector outputs (RF1, RF2)	1,2	Vdd-1.5	Vdd+1.5	V
VACRF	AC peak voltage on open collector outputs (RF1, RF2)	1	Vdd-1.5	Vdd+1.5	V
Top	Ambient operating temperature		-40	85	°C

Note 1: At minimum, VDD - 1.5 V cannot be lower than 1.2 V.
Note 2: At maximum, VDD+1.5 V cannot be higher than 5.5 V.

6. DC Electrical Characteristics

(Min/max values are valid over the recommended operating range Vdd = 2.2-5.4V. Typical conditions: Top = 27°C; Vdd = 3.0 V)

Digital I/O	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			**min**	**typ**	**max**		
Supply current (TX mode, Pout = Pmax)	Idd_TX			20	22	mA	315MHz Band
				21	25		433MHz Band
				22	26		868MHz Band
				24	28		916MHz Band
Supply current (TX mode, Pout = 0 dBm, 50Ω Load)	Idd_TX0			15		mA	315MHz Band
				16			433MHz Band
				22			868MHz Band
				24			916MHz Band
Supply current (RX mode)	Idd_RX			8.5	13	mA	315MHz Band
				8.5	14		433MHz Band
				9.5	15		868MHz Band
				11	17		916MHz Band
Sleep current	Is				0.25	µA	All blocks disabled
Idle current	IIDLE			3	3.5	mA	Oscillator and baseband enabled
Low battery voltage detector current consumption	IVD			0.5		µA	
Wake-up timer current consumption	IWUT			1.5		µA	
Low battery detect threshold	Vlb		2.2		5.3	V	Programmable in 0.1 V steps
Low battery detection accuracy				±75		mV	
Analog RSSI Output Level	RSSIL		300		1000	mV	-50dBm>RFin>-115dBm
Digital input low level	Vil				0.3*Vdd	V	
Digital input high level	Vih		0.7*Vdd			V	
Digital input current low	Iil		-1		1	µA	Vil = 0 V
Digital input current high	Iih		-1		1	µA	Vih = Vdd, Vdd = 5.4 V
Digital output low level	Vol				0.4	V	Iol = 2 mA
Digital output high level	Voh		Vdd-0.4			V	Ioh = -2 mA
Digital input capacitance					2	pF	

Digital output rise/fall time					10	ns	Load = 15 pF

7. AC Electrical Characteristics

(Min/max values are valid over the recommended operating range Vdd = 2.2-5.4V. Typical conditions: Top = 27°C; Vdd= 3.0V)

Receiver	**Sym**	**Notes**		**Limit Values**		**Unit**	**Test Conditions**
Parameter			**min**	**typ**	**max**		
RF input impedance (real,differential)				250		Ohms	LNA gain (0 dB, -14 dB)
Maximum input power			0			dBm	LNA Max gain
Receiver bandwidth			67		400	kHz	
Receiver Sensitivity		1		-108		dBm	315MHz Band
				-105			433MHz Band
				-101			868MHz Band
				-101			916MHz Band
IIP3 In band interferers (-85dBm carrier,1MHz offset,CW)		3		-64		dBm	315MHz Band
				-66			433MHz Band
				-60			868MHz Band
				-60			916MHz Band
IIP3 Out of band interferers (-85dBm carrier,10 MHz offset,CW)				-40		dBm	315MHz Band
				-40			433MHz Band
				-37			868MHz Band
				-34			916MHz Band
FSK bit rate			0.6		115.2	kbps	Digital filters
					256		Analog filter
AFA lock range				0.8*Δdev		kHz	Δdev = FSK deviation
RF input capacitance				1		pF	
Analog RSSI Filter Cap			1			nF	
Analog RSSI deviation		4			350	mV	
RSSI accuracy				+/-5		dB	
RSSI dynamic range				46			
RSSI programmable threshold steps				6		dBm	
Digital RSSI response time				500		us	RSSI signal goes high after input signal exceeds programmed limit. CAPARRSI = 5 nF
Spurious emission (@ Pmax)				<95		dBc	315 MHz Band
							433 MHz Band
							868 MHz Band
							916 MHz Band

AC Electrical Characteristics - continued

(Min/max values are valid over the recommended operating range Vdd = 2.2-5.4V. Typical conditions: Top = 27°C; Vdd = 3.0 V)

Transmitter	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			min	typ	max		
FSK bit rate					256	kbps	
FSK frequency deviation			15		240	kHz	Programmable in 15 kHz steps
Output power (into 50 Ohms)	Pmax			+7		dBm	315 MHz Band
				+5			433 MHz Band
				0			868 MHz Band
				0			916 MHz Band
Output power (into differential load)		5		+8		dBm	315 MHz Band
				+7			433 MHz Band
				+5			868 MHz Band
				+4			916 MHz Band
Open collector output DC current			0.5		6	mA	Programmable
Reference Spur (@ Pmax)				-50		dBc	315MHz Band
				-57			433MHz Band
				-60			868MHz Band
				-60			916MHz Band
2nd Harmonics (@ Pmax)				-35		dBc	315MHz Band
				-37			433MHz Band
				-58			868MHz Band
				-58			916MHz Band
3rd Harmonics (@ Pmax)				-35		dBc	315MHz Band
				-43			433MHz Band
				-65			868MHz Band
				-60			916MHz Band
Antenna tuning capacitance			2	2.6	3.2	pF	315MHz Band
							433MHz Band
			2.1	2.7	3.3		868MHz Band
							916MHz Band
Output Capacitance Quality factor			13	15	17		315MHz Band
							433MHz Band
			8	10	12		868MHz Band
							916MHz Band
Phase noise				-75		dBc/Hz	100 kHz from carrier
				-85			1 MHz from carrier

AC Electrical Characteristics - continued

(Min/max values are valid over the recommended operating range Vdd = 2.2-5.4V. Typical conditions: Top = 27°C; Vdd = 3.0 V)

Timing	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			min	typ	max		
Transmit to Receive switch time				450		us	Synthesizer off, osc on, 10 MHz step
				425		us	Both ON, 10 MHz step
Receive to Transmit switch time				350		us	Synthesizer off, osc on, 10MHz step
				300		us	Both ON, 10 MHz step
Internal POR timeout					100	ms	Vdd at 90% of final value
Wake-up timer clock period				1		ms	Calibrated every 30 seconds

PLL Characteristics	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			min	typ	max		
PLL reference freq	f_{REF}	2	8	10	12	MHz	
PLL lock time				10		us	within 1kHz settle, 10MHz step
PLL startup time					250	us	Crystal running
Crystal load capacitance	CL		8.5		16	pF	Programmable in 0.5 pF steps, tolerance +/- 10%
Xtal oscillator startup time				1.25	5	ms	Crystal ESR < 100 Ohms
Frequency Range (w/ 10MHz ref xtal)			310.24		318.75	MHz	315MHz Band (2.5kHz steps)
			430.24		439.75		433MHz Band (2.5kHz steps)
			860.48		879.51		868MHz Band (5.0kHz steps)
			900.72		929.27		916MHz Band (7.5kHz steps)

NOTES:

1- BW=67 kHz, BER=10^{-3}, Data Rate=2.4 kbps, digital filter.

2- Other crystal frequencies may be used, but every function on chip, including wake-up timer, output clock, data rate, clock recovery, etc…, is dependent on this reference frequency and everything will scale accordingly.

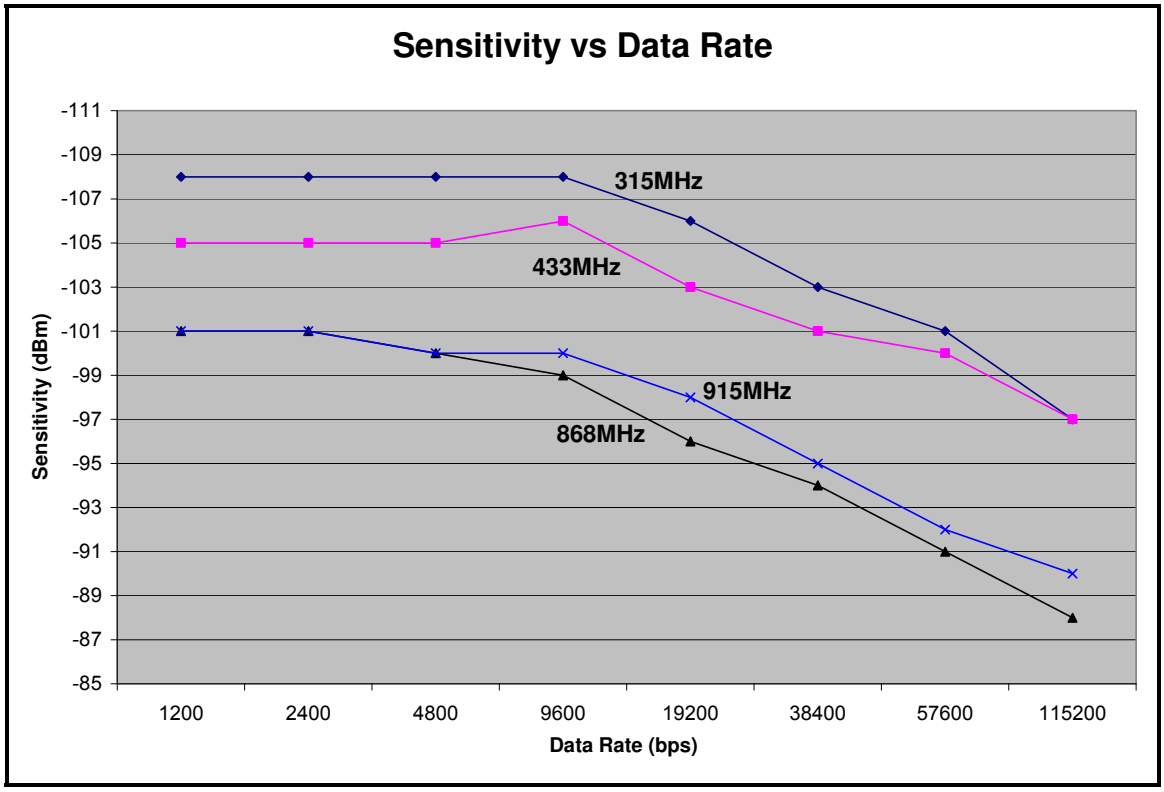
3- FCC Class 2 Blocking.

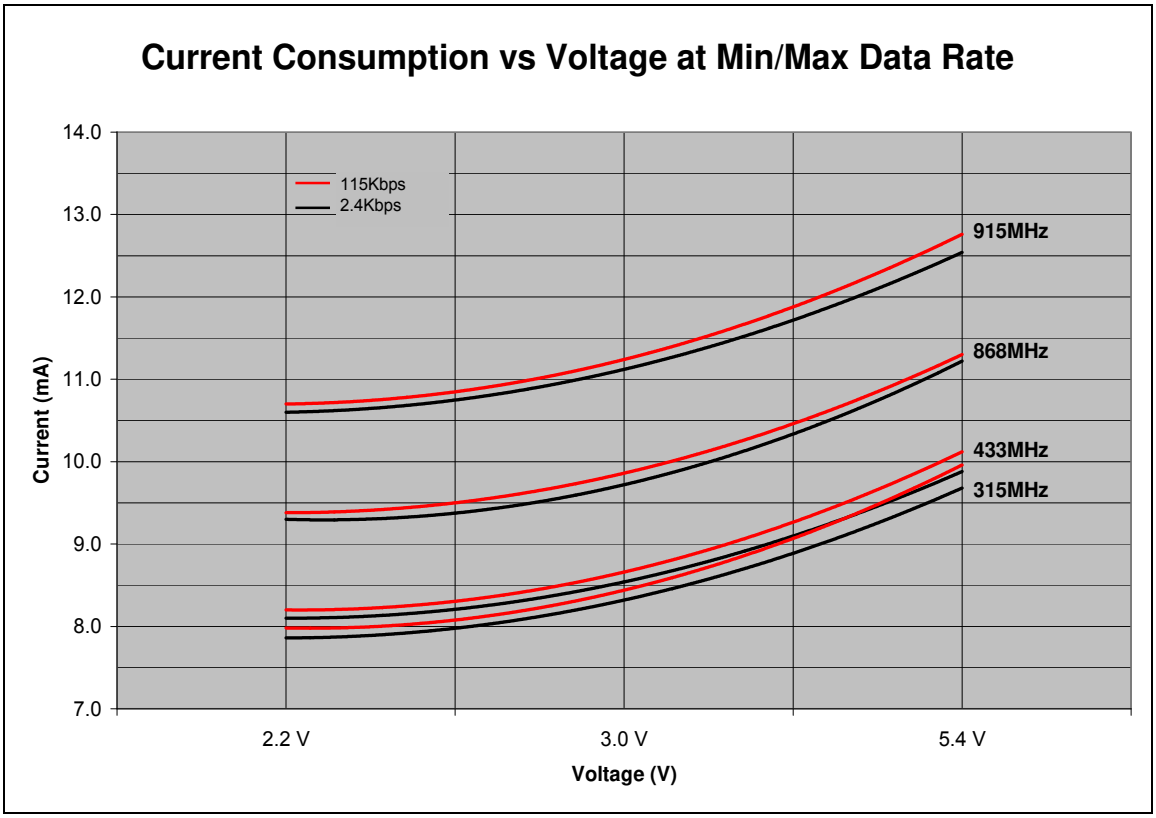
4- ASK using the Analog RSSI detector. ASK_{RFin} > -60dBm.

5- Load equivalent to a tuned Loop or Dipole Antenna at the required operating frequency.

8. Receiver Measurement Results

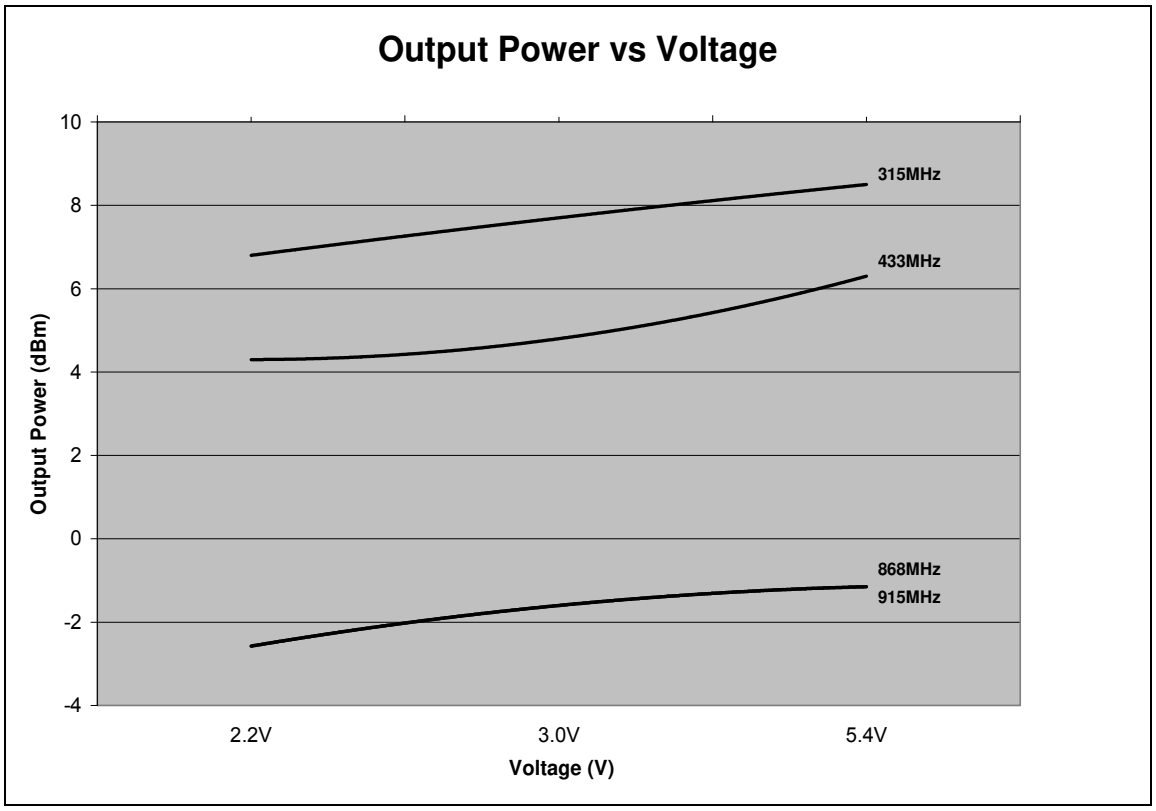
The sensitivity measurements were derived from the *Typical Application Circuit* of Figure 1 and the layout as suggested on pgs 5-6. All data rates are based on a 10^{-3} BER.

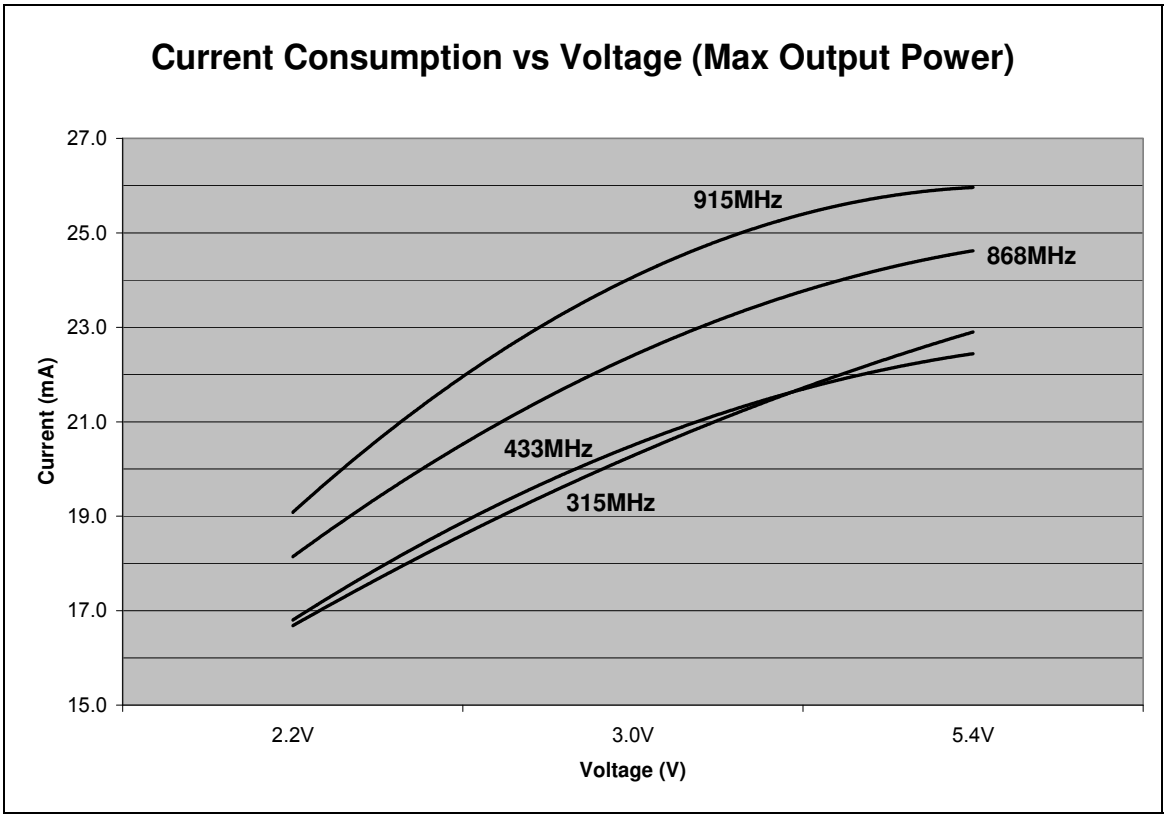




9. Transmitter Measurement Results

The transmitter measurements were derived from the Typical Application Circuit of Figure 1, pg 4, and the layout as suggested on pgs 5-6.

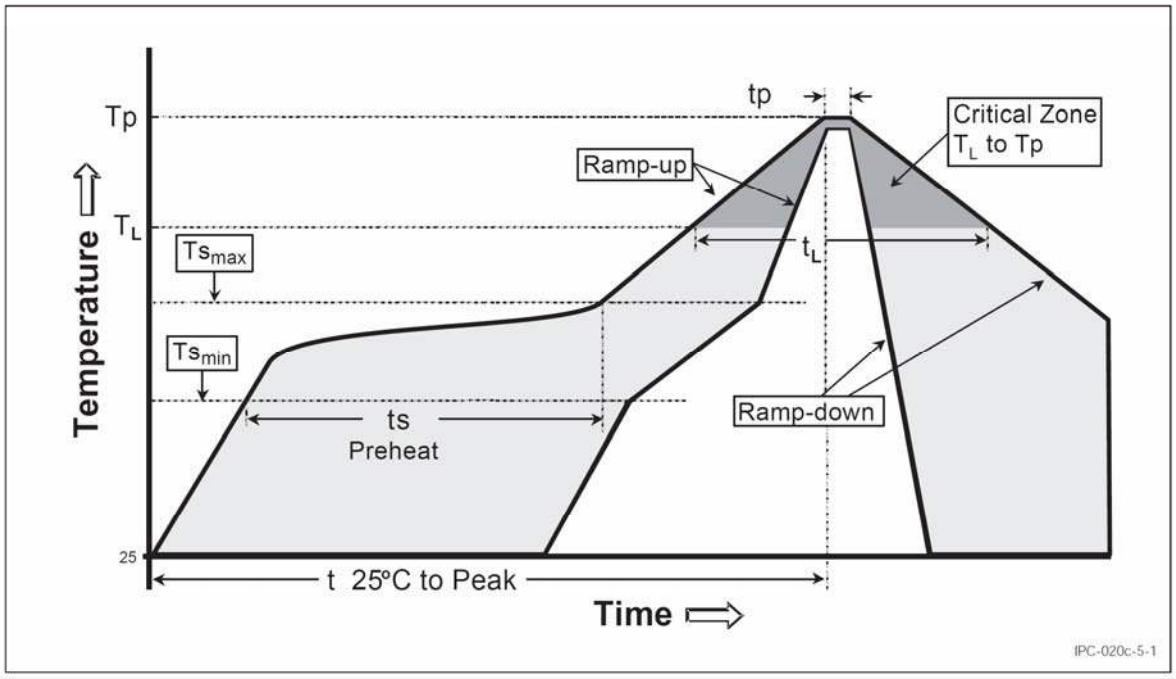




IPC/JEDEC J-STD-020C REFLOW PROFILE

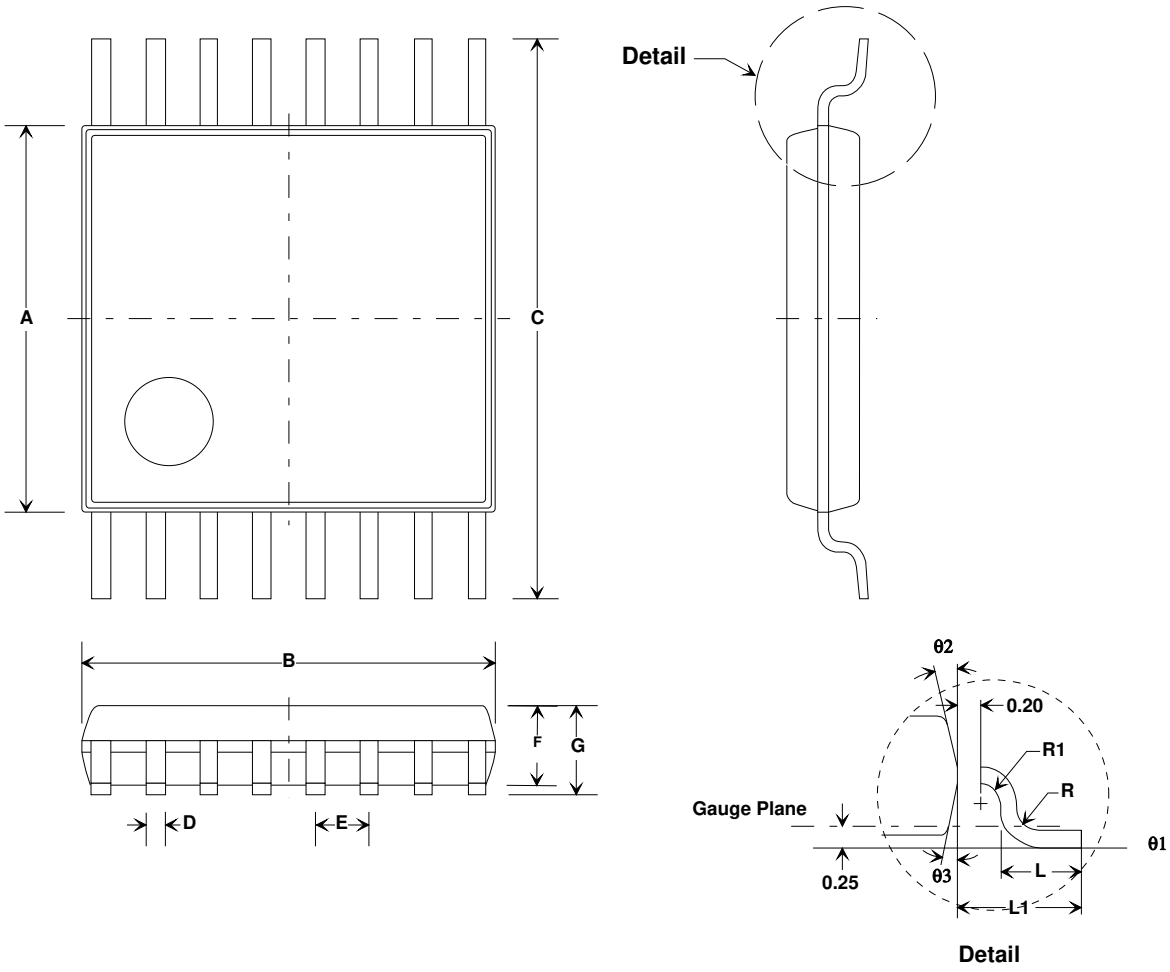
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.



10.0 Package Dimensions – 6.4x5mm 16-pin TSSOP Package

(all values in mm)



Symbol	Dimensions in mm			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.30	4.40	4.50	0.169	0.173	0.177
B	4.90	5.00	5.10	0.193	0.197	0.201
C		6.40 BSC.			0.252 BSC.	
D	0.19		0.30	0.007		0.012
E		0.65 BSC.			0.026 BSC.	
F	0.80	0.90	1.05	0.031	0.035	0.041
G			1.20			0.47
L	0.50	0.60	0.75	0.020	0.024	0.030
L1		1.00 REF.			0.39 REF	
R	0.09			0.004		
R1	0.09			0.004		
θ1	0		8	0		8
θ2		12 REF.			12 REF.	
θ3		12 REF.			12 REF.	