

File Number 2342

D43C Series

T-33-17

3-Ampere Silicon P-N-P Power Transistors

Complementary to the D42C Series

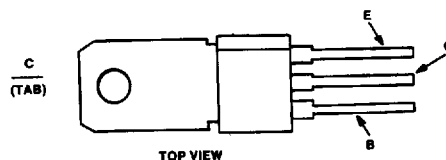
Features:

- High free-air power dissipation
- Low collector saturation voltage (-0.5V typ. @ -3A I_C)
- Excellent linearity
- Fast switching

The D43C-series of silicon p-n-p power transistors are designed for various specific and general purpose applications, such as: output and driver stages of amplifiers operating at frequencies from DC to greater than 1 MHz; series, shunt and switching regulators; and low and high frequency inverters/converters.

These devices are supplied in the JEDEC TO-202AB plastic package.

TERMINAL DESIGNATIONS



92CS-43473

JEDEC TO-202AB

POWER
TRANSISTORS

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$) (unless otherwise specified)

RATING	SYMBOL	D43C1, 2, 3	D43C4, 5, 6	D43C7, 8, 9	D43C10, 11, 12	UNITS
Collector-Emitter Voltage	V_{CEO}	-30	-45	-60	-80	Volts
Collector-Emitter Voltage	V_{CES}	-40	-55	-70	-90	Volts
Emitter Base Voltage	V_{EBO}	-5	-5	-5	-5	Volts
Collector Current — Continuous	I_C	-3	-3	-3	-3	A
Peak ⁽¹⁾	I_{CM}	-5	-5	-5	-5	A
Base Current — Continuous	I_B	-2	-2	-2	-2	A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ @ $T_C = 25^\circ\text{C}$	P_D	2.1 12.5	2.1 12.5	2.1 12.5	2.1 12.5	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	60	60	60	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	10	10	10	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	+260	+260	+260	+260	$^\circ\text{C}$

(1) Pulse Test Pulse Width = 300ms Duty Cycle \leq 2%.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$) (unless otherwise specified)

T-33-17

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS⁽¹⁾ HARRIS SEMICOND SECTOR					
Collector-Emitter Sustaining Voltage ($I_C = -100\text{mA}$)	D43C1, 2, 3 D43C4, 5, 6 D43C7, 8, 9 D43C10, 11, 12	$V_{CEO(sus)}$	-30 -45 -60 -80	— — — —	Volts
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CES}$)		I_{CES}	—	—	μA
Emitter Cutoff Current ($V_{EB} = -5\text{V}$)		I_{EBO}	—	—	μA

SECOND BREAKDOWN

Second Breakdown with Base Forward Biased	FBSOA	SEE FIGURE 3
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ON CHARACTERISTICS⁽¹⁾

DC Current Gain ($I_C = -200\text{mA}$, $V_{CE} = -1\text{V}$)	D43C1, 4, 7, 10 D43C2, 5, 8, 11 D43C3, 6, 9, 12	h_{FE}	25 40 40	— — —	— 120 120	—
($I_C = -1\text{A}$, $V_{CE} = -1\text{V}$)	D43C1, 4, 7, 10	h_{FE}	10	—	—	—
($I_C = -2\text{A}$, $V_{CE} = -1\text{V}$)	D43C2, 5, 8, 11 D43C3, 6, 9, 12		20 20	— —	— —	—
Collector-Emitter Saturation Voltage ($I_C = -1\text{A}$, $I_B = -50\text{mA}$)	D43C2, 5, 8, 11 D43C3, 6, 9, 12	$V_{CE(sat)}$	— —	— —	-0.5 -0.5	Volts
($I_C = -1\text{A}$, $I_B = -100\text{mA}$)	D43C1, 4, 7, 10	$V_{CE(sat)}$	—	—	-0.5	Volts
Base-Emitter Saturation Voltage ($I_C = -1\text{A}$, $I_B = -100\text{mA}$)		$V_{BE(sat)}$	—	—	-1.3	Volts

DYNAMIC CHARACTERISTICS

Collector Capacitance ($V_{CB} = -10\text{V}$, $f = 1\text{MHz}$)	C_{CBO}	—	—	125	pF
Current-Gain — Bandwidth Product ($I_C = -20\text{mA}$, $V_{CE} = -4\text{V}$)	f_T	—	40	—	MHz

SWITCHING CHARACTERISTICS

Resistive Load					
Delay Time + Rise Time	$I_C = -1\text{A}$, $I_{B1} = I_{B2} = -0.1\text{A}$ $V_{CC} = 30\text{V}$, $t_p = 25 \mu\text{sec}$	$t_d + t_r$	—	50	—
Storage Time		t_s	—	500	—
Fall Time		t_f	—	50	—

(1) Pulse Test PW = 300ms Duty Cycle \leq 2%.

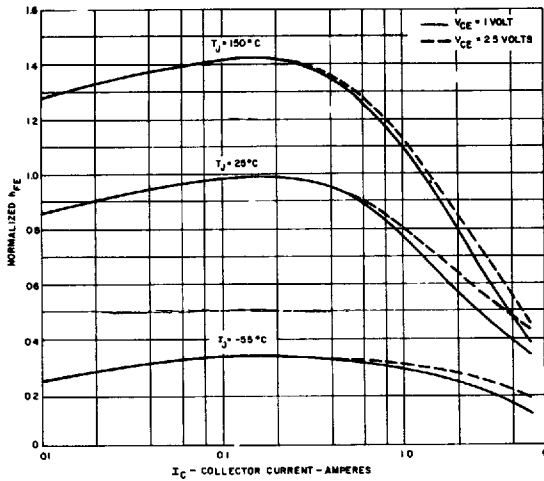


FIG. 1 TYPICAL NORMALIZED h_{FE} VS. I_C
HARRIS SEMICONDUCTOR

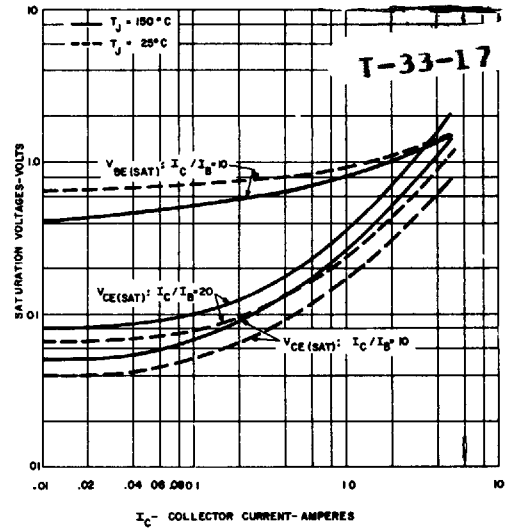


FIG. 2 TYPICAL SATURATION VOLTAGE CHARACTERISTICS

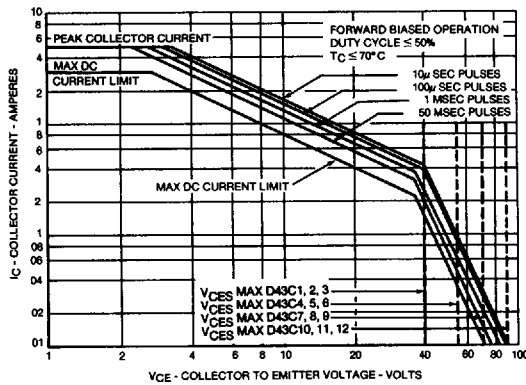


FIG. 3 SAFE REGION OF OPERATION

POWER TRANSISTORS

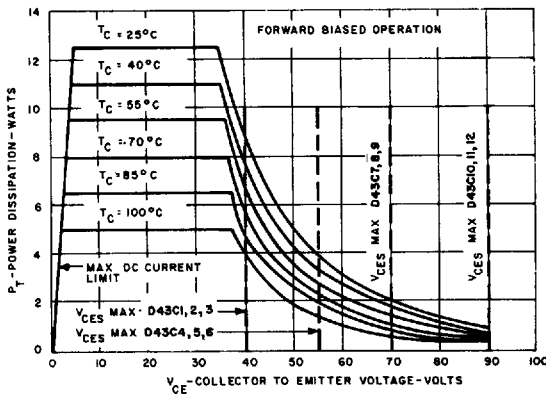


FIG. 4 MAXIMUM PERMISSIBLE DC POWER DISSIPATION

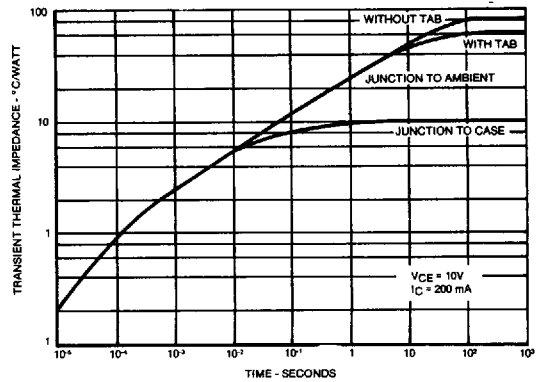


FIG. 5 MAXIMUM TRANSIENT THERMAL IMPEDANCE