SM802120

ClockWorks™ 125MHz LVDS / 125 MHz HCSL Ultra-Low Jitter Frequency Synthesizer

General Description

The SM802120 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution. It is based upon a unique patented RotaryWave® architecture that provides very low phase noise.

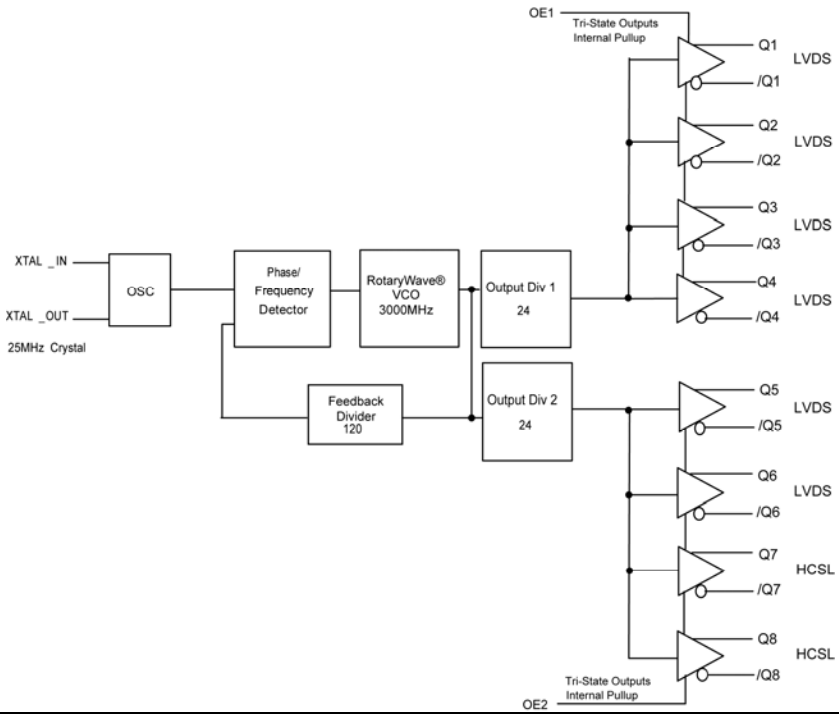
The device operates from a 3.3V or 2.5V power supply and synthesizes eight differential 125MHz output clocks, six LVDS and two HCSL. The SM802120 accepts a 25 MHz crystal input.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Generates six LVDS 125MHz clocks and two HCSL 125MHz clocks
- 2.5V or 3.3V operating range
- Typical phase jitter @ 125 MHz (1.875MHz to 20MHz): 100fs
- Industrial temperature range (–40°C to +85°C)
- Green, RoHS, and PFOS compliant
- Available in 44-pin 7mm × 7mm QFN package

Block Diagram



Ordering Information

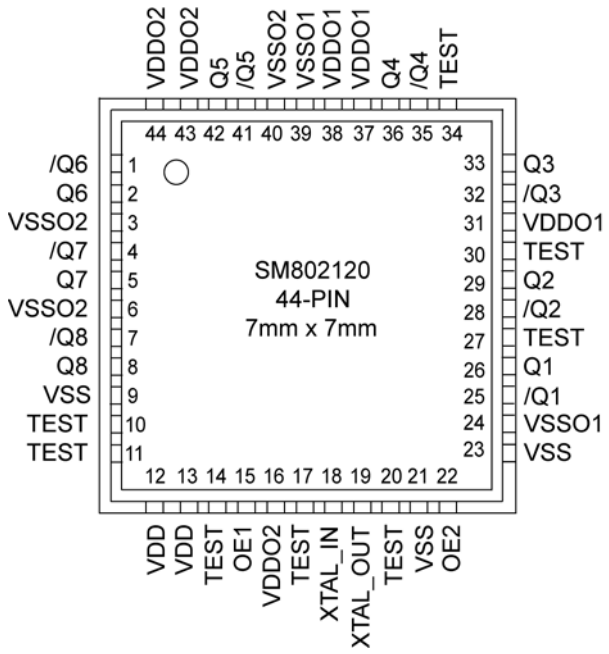
Part Number	Marking	Shipping	Temperature Range	Package

ClockWorks is a trademark of Micrel, Inc
RotaryWave is a registered trademark of Micrel, Inc.

SM802120UMG	802120	Tray	–40°C to +85°C	44-Pin QFN
SM802120UMGTR	802120	Tape and Reel	–40°C to +85°C	44-Pin QFN

Note:
1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



44-Pin QFN
(Top View)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
25, 26 28, 29 32, 33 35, 36	/Q1, Q1 /Q2, Q2 /Q3, Q3 /Q4, Q4	O, (DIF)	LVDS	Differential Clock Outputs from Bank 1 125MHz
41, 42 1, 2	/Q5, Q5 /Q6, Q6	O, (DIF)	LVDS	Differential Clock Outputs from Bank 2 125MHz
4, 5 7, 8	/Q7, Q7 /Q8, Q8	O, (DIF)	HCSL	Differential Clock Outputs from Bank 2 125MHz
31, 37, 38	VDDO1	PWR		Power Supply for the Outputs on Bank 1
43, 44, 16	VDDO2	PWR		Power Supply for the Outputs on Bank 2
24, 39	VSSO1	PWR		Power Supply Ground for the Outputs on Bank 1
3, 6, 40	VSSO2	PWR		Power Supply Ground for the Outputs on Bank 2
10, 11, 14, 17, 20, 27, 30, 34	TEST			Factory Test Pins. Do not connect anything to these pins.
12, 13	VDD	PWR		Core Power Supply
9, 21, 23	VSS (Exposed Pad)	PWR		Core Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
18	XTAL_IN	I, (SE)	Crystal	Crystal Reference Input, no load caps needed. See Fig. 7.
19	XTAL_OUT	O, (SE)	Crystal	Crystal Reference Output, no load caps needed. See Fig. 7.
15	OE1	I, (SE)	LVCMOS	Output Enable, Q1-Q4 disables to tri-state, 0 = Disabled, 1 = Enabled, 45KΩ pull-up
22	OE2	I, (SE)	LVCMOS	Output Enable, Q5-Q8 disables to tri-state, 0 = Disabled, 1 = Enabled, 45KΩ pull-up

Truth Table

OE1/2	OUTPUTS
0	Tri-state
1	HCSL / LVDS

Application Information

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal.

Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a Quartz crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for further details.

Contact Micrel's HBW applications group if you need assistance on selecting a suitable crystal for your application at: hbwhelp@micrel.com.

LVDS Outputs

LVDS outputs are to be terminated with 100Ω across Q and /Q. For best performance, load all outputs. Outputs can be DC or AC-coupled.

HCSL Outputs

HCSL outputs are to be terminated with 50Ω to V_{SS}. For best performance, load all outputs. For AC-coupled or to change the termination, contact Micrel's application group: hbwhelp@micrel.com.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}, $V_{DDO1/2}$) ……..…….+4.6V
Input Voltage (V_{IN})…….……..……-0.50V to V_{DD}+0.5V
Lead Temperature (soldering, 20 sec.)…….....…….260°C
Case Temperature…….....…….115°C
Storage Temperature (T_s)…… ..... …..-65°C to +150°C

Operating Ratings[2]

Supply Voltage ($V_{DD,}$ $V_{DDO1/2}$)..... +2.375V to +3.465V
Ambient Temperature (T_A)..... –40°C to +85°C
Junction Thermal Resistance[3]
QFN (θ_{JA})
Still-Air ..... 24°C/W
QFN (ψ_{JB})
Junction-to-Board ..... 8°C/W

DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD,}$ $V_{DDO1/2}$	3.3V Operating Voltage	V_{DDO1}=V_{DDO2}	3.135	3.3	3.465	V
	2.5V Operating Voltage	V_{DDO1}=V_{DDO2}	2.375	2.5	2.625	V
I_{DD}	Total supply current	Outputs loaded		185	240	mA

LVCMOS INPUT (OE1, OE2) DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, $_{TA}$ = –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

LVCMOS OUTPUT DC Electrical Characteristics[4]

V_{DD} = $_{VDDO1/2}$ = 3.3V ±5% or 2.5V ±5%, V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5% T_A = –40°C to +85°C. R_L = 100Ω across Q and /Q.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	Figures 1, 5	275	350	475	mV
ΔV_{OD}	V_{OD} Magnitude Change				40	mV
V_{OS}	Offset Voltage		1.15	1.25	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

HCSL OUTPUT DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%, V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5% T_A = –40°C to +85°C. R_L = 50Ω to V_{SS}.

Symbol	Parameter	Condition	Min	Typ	Max
V_{OH}	Output High Voltage	Figures 1, 4	660	700	850
V_{OL}	Output Low Voltage		-150	0	27
V_{CROSS}	Crossing Point Voltage		250	350	550

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	10pF to 12pF Load	Fundamental, Parallel Resonant			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			1	5	pF
Correlation Drive Level			10	100	uW

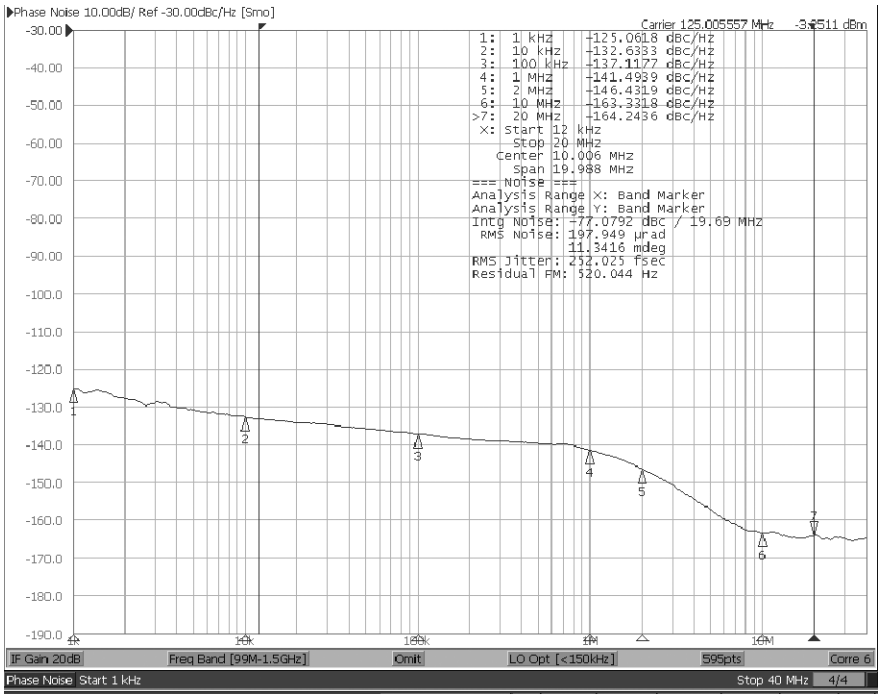
AC Electrical Characteristics[4, 5]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C.

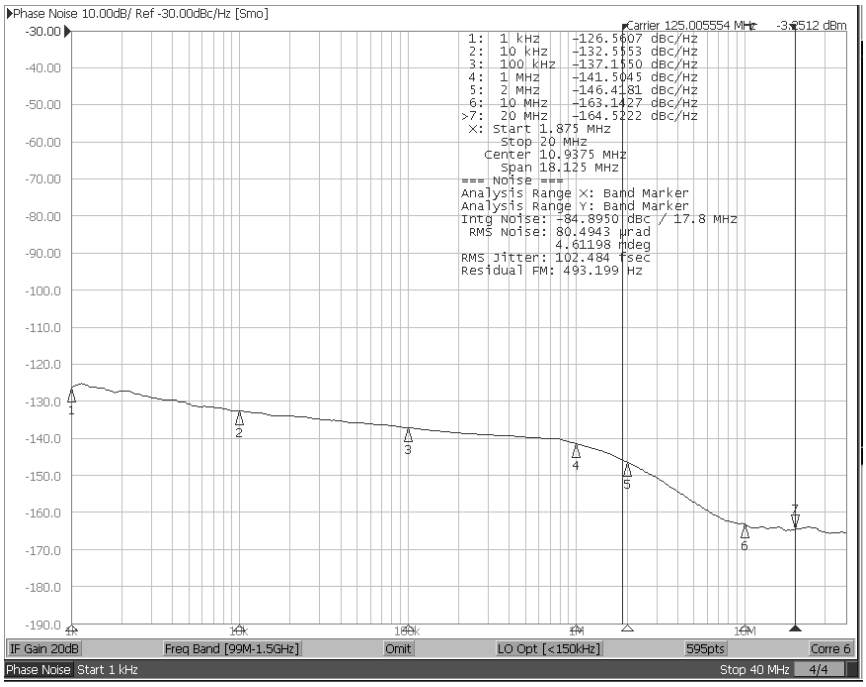
Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{OUT}	Output Frequency			125		MHz
T_R/T_F	LVDS Output Rise/Fall Time	20% – 80%, Figures 2, 5	100	160	400	ps
T_R/T_F	HCSL Output Rise/Fall Time	20% – 80%, Figures 2, 4	150	300	450	ps
ODC	Output Duty Cycle	HCSL, LVDS outputs	48	50	52	%
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter[6] (Output = 125MHz LVDS)	Integration Range:(12KHz – 20MHz)		250		fs
		Integration Range:(1.875MHz – 20MHz)		100		fs
	RMS Phase Jitter[6] (Output = 125MHz HCSL)	Integration Range:(12KHz – 20MHz)		250		fs
		Integration Range:(1.875MHz – 20MHz)		100		fs
	Spurious Noise Components	25MHz (LVDS outputs)		-80		dBc
		25MHz (HCSL outputs)		-85		

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table after thermal equilibrium has been established.
5. All phase noise measurements were taken with an Agilent 5052B phase noise system
6. Measured using 25MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

Phase Noise Plots

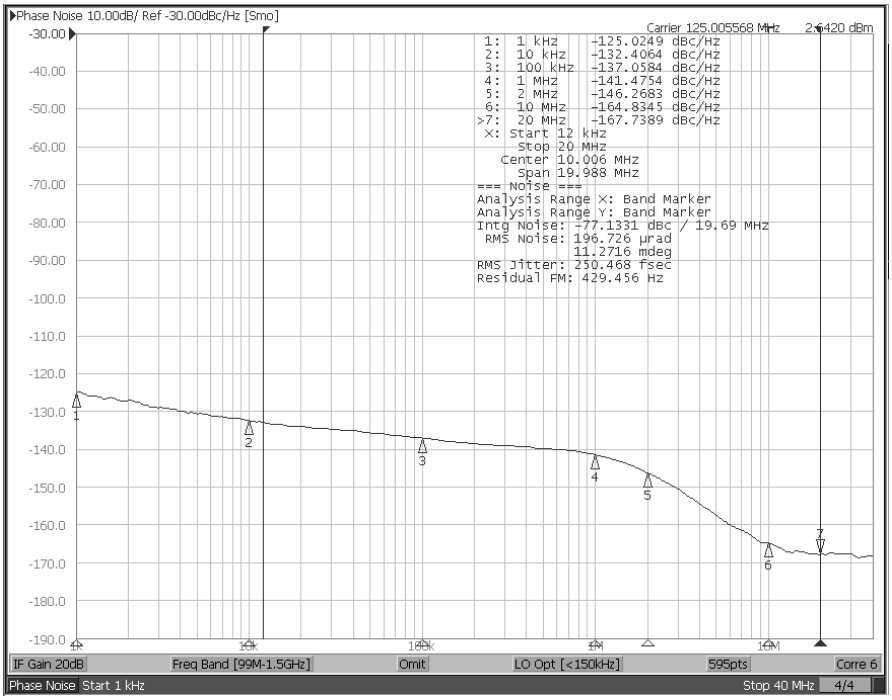


125MHz LVDS Integrated Jitter 12KHz-20MHz 252fs

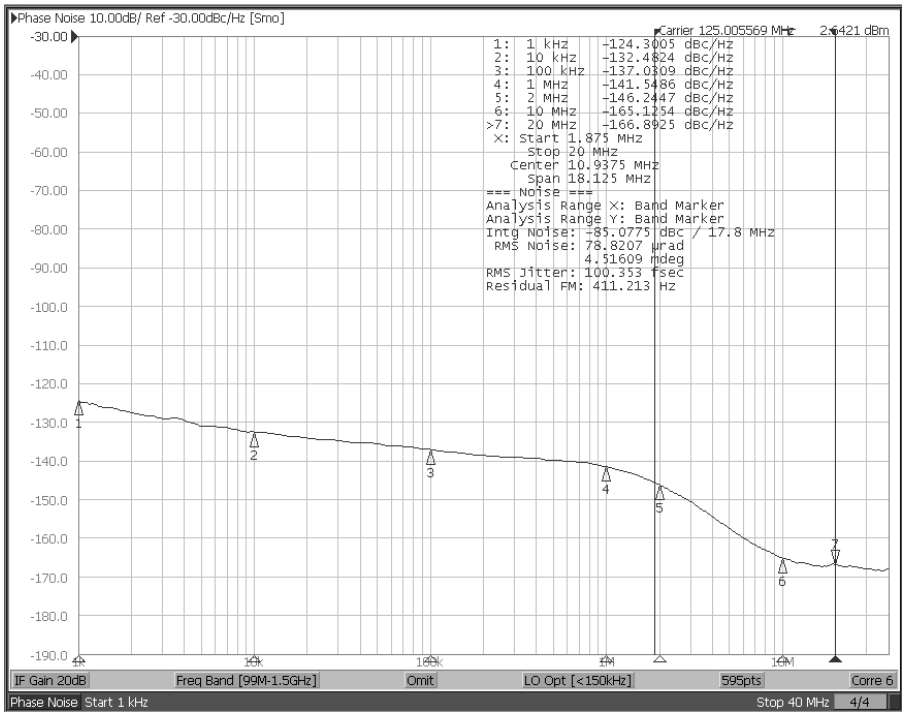


125MHz LVDS Integrated Jitter 1.875MHz-20MHz 102fs

Phase Noise Plots (Continued)



125MHz HCSL Integrated Jitter 12KHz-20MHz 250fs



125MHz HCSL Integrated Jitter 1.875MHz-20MHz 100fs

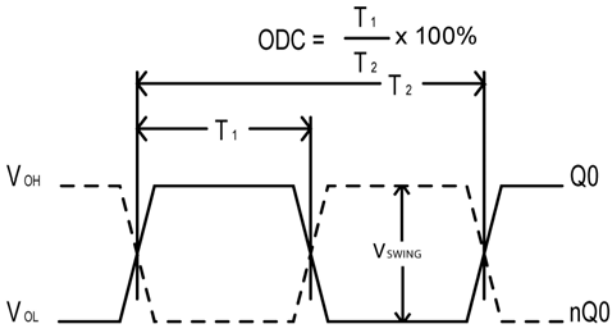


Figure 1. Duty Cycle TIming

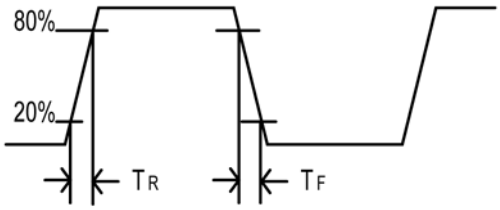


Figure 2. All Outputs Rise/Fall Time

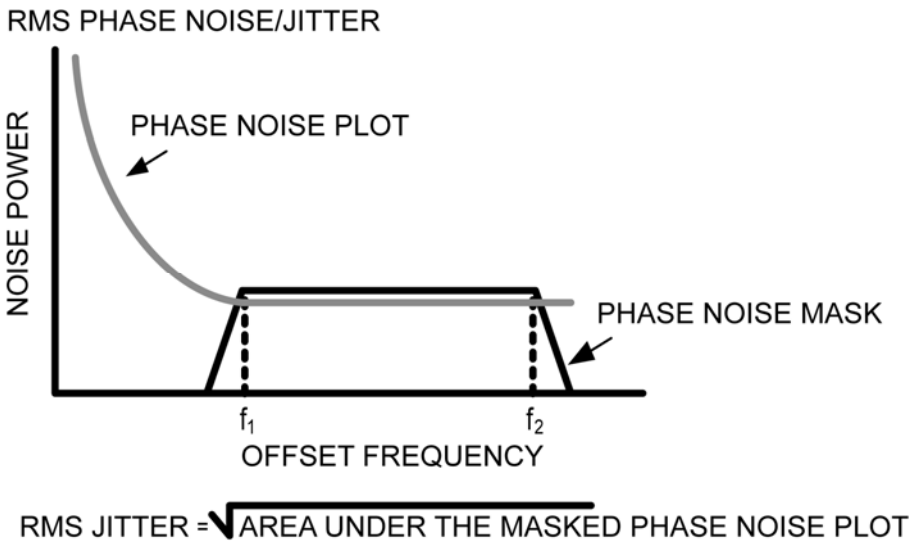


Figure 3. RMS Phase/Noise/Jitter

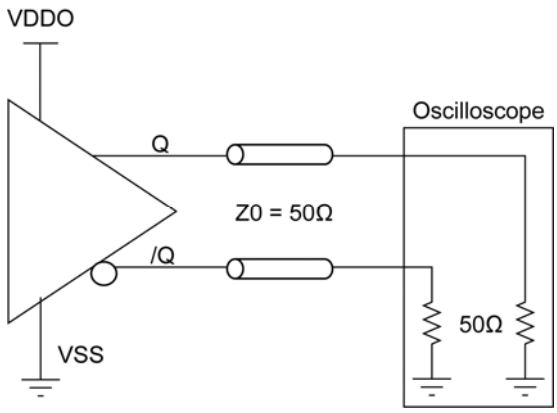


Figure 4. HCSL Output Load

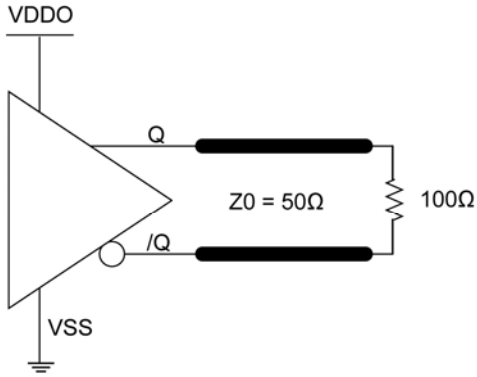


Figure 5. LVDS Output Load

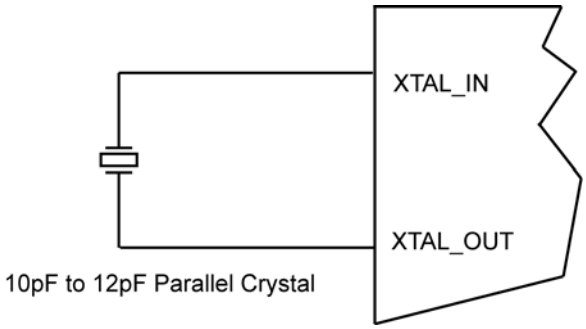
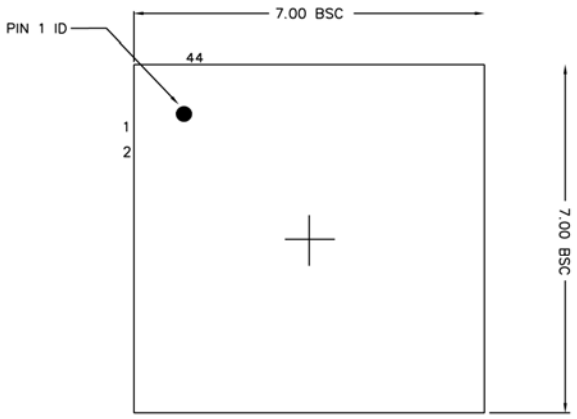
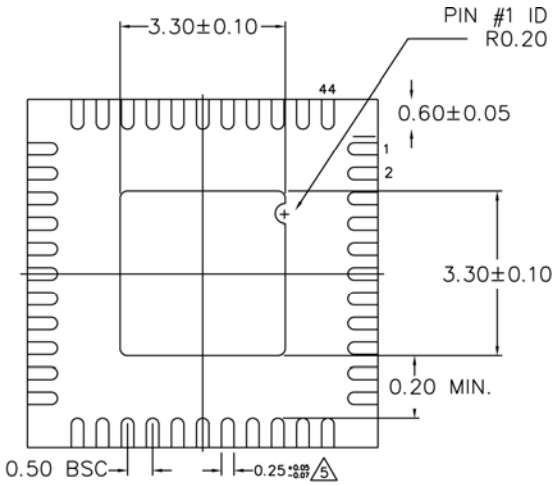


Figure 7. Crystal Input Interface

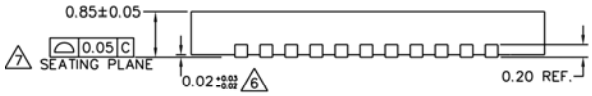
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

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Revision Template History

Date	Change Description/Edits by:	Rev.
8/4/10	Added new paragraph to disclaimer in boiler plate. Per Colin Sturt. M.Galvan	14