ADS62xxEVM User's Guide

User's Guide

Literature Number: SLAU197B
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1 Overview

This user's guide gives a general overview of the evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the ADS6245, ADS6244, ADS6243, ADS6225, ADS6224, and ADS6223, which collectively are referred to as ADS62xx. The ADS62xxEVM provides a platform for evaluating the dual-channel ADS62xx 14- and 12-bit analog-to-digital converters (ADC) under various signal, reference, and supply conditions. In certain instances, the user's guide may offer directions for only the 14-bit ADC family, which is referred to as the ADS624x, or only the 12-bit ADC family, which is referred to as the ADS622x. In addition, this user's guide explains the procedure for hooking up the ADS62xxEVM to TI's high-speed LVDS deserializer and capture card, the TSW1200.

This document must be used in combination with the respective ADC data sheet.

1.1 *ADS62xxEVM Quick-Start Procedure*

Using the quick-start procedure, many users can begin evaluating the ADC in a minimal amount of time. The quick-start procedure includes details on how to set up the ADS62xxEVM used along with TI's high-speed LVDS deserializer. A complete listing of all EVM features follows in Section 2. The quick-start instructions are delineated as ADS62xx, which refers to instructions pertaining to the ADC EVM; or TSW1200, which refers to instructions pertaining to the high-speed LVDS deserializer.

1. ADS62xx: Verify all jumper settings against the schematic jumper list in Table 1:

Table 1. Three-Pin Jumper List

JUMPER	FUNCTION	ADS624x DEFAULT	ADS622x DEFAULT
J17	Sets ADC coarse gain mode and ADC reference mode. Use silkscreen for configuration.	0-dB gain, internal references	0-dB gain, internal references
J20 (1)	Sets ADC output mode to either 1-wire, 2-wire, SDR, or DDR. Use silkscreen for configuration.	DDR, 2-wire	DDR, 2-wire
J18 (1)	Sets ADC output serialization to either 14x or 16x and sets data formatting to rising edge or falling edge when the ADC is used in SDR mode. Use silkscreen for configuration.	16x, rising edge	14x, rising edge (2)
J19 (1)	This is an ADC reserved pin and must always be set to *divide by 1*.	Divide by 1	Divide by 1
J21 (1)	Selects the data output format as MSB- or LSB-first and 2s-complement or offset-binary.	MSB-first, offset binary	MSB-first, offset binary

(1) Although the ADS62xx supports many different output formats, for customers using the TSW1200 data capture card for ADC evaluation, one must leave these jumpers in their default condition. The TSW1200 is programmed to only accept one specific output format that the ADS62xx offers.

(2) The silkscreen on the EVM only refers to the modes of the ADS624x. When an ADS622x, or 12-bit ADC, is being evaluated, the silkscreen 14x refers to the 12x serialization mode and the silkscreen 16x refers to the 14x serialization mode.

2. ADS62xx: Connect 3.3-Vdc supplies to P1 and P3, with the returns to P2 and P4, respectively. The grounds can be shorted together.
3. TSW1200: Connect 5 Vdc to J15 and the return to J14.
4. TSW1200: If evaluating the 12-bit ADC, or ADS622x, verify that jumper J11 is set to short pins 1–2, which configures the FPGA for deserialization of a 12-bit ADC serial data stream. On J11, short pins 2–3 for evaluating an ADS624xEVM.
5. Connect the two boards together by connecting J9 on the TSW1200 circuit board to J15 of the ADS62xxEVM.
6. ADS62xx and TSW1200: Switch power supplies on.

7. ADS62xx: Using a low-phase-noise, filtered frequency generator with 50-Ω source output impedance, generate a 0-V offset, 1.5-Vrms sine-wave clock into J12. The frequency of the clock must be within the specification for the device speed grade. TI uses an Agilent 8644B with a crystal MCF filter as a clock source.
8. TSW1200: Depress SW4 (FPGA reset). This resets the logic inside the FPGA and must be done every time one changes the ADC clock frequency.
9. ADS62xx: Using a low-phase-noise, filtered frequency generator with a 50-Ω source output impedance, generate a 10-MHz, 0-V offset, –1-dBFS-amplitude sine-wave signal into either J10 (input channel A) or J11 (input channel B). This provides a transformer-coupled differential input signal to the ADC. TI uses an Agilent 8644B with an LC filter as a signal source.
10. TSW1200: Connect the TSW1200 or suitable logic analyzer to J5 to capture the resulting digital data. If you connect a TSW1200 to capture data, follow the additional alphabetically labeled steps.
    a. After installing the TSW1200 software and connecting the TSW1200 to the USB port, open the TSW1200 software.
    b. Depending on the ADC under evaluation, select from the TI ADC Section pulldown .
    c. Change the ADC Sample Rate and ADC Input Frequency to match those of the signal generator.
    d. After selecting a Single Tone FFT test, press the Capture Data button.

Note: Any time the clock frequency of the ADC changes during the ADC evaluation, one must reset the FPGA deserializer by depressing SW4. This allows the deserializer to re-align the ADC data capture to the new output clock frequency.

2 Circuit Description

2.1 Schematic Diagram

The schematic diagram for the EVM is in Section 4.3.

2.2 ADC Circuit Function

The following sections describe the function of individual circuits. Refer to the relevant data sheet for device operating characteristics.

2.2.1 ADC Operational Mode

By default, the ADC is configured to operate in parallel-mode operation, because the surface-mount jumper asserts a 3.3-V state to the ADC reset pin. Consequently, the SW1 reset pushbutton must be pressed only when the device is configured into serial operational mode. Because the ADC is in parallel operation mode, voltages are used to set the ADC modes. Users can use the EVM silkscreen to set the operation modes.

2.2.2 ADC Power

Power is supplied to the EVM via banana jack sockets. Separate connections are provided for a 3.3-V digital buffer supply (P1) and 3.3-V analog supply (P3). In most cases, these can be shorted together for ADC evaluation. When using the amplifier evaluation path, users must connect the positive rail to J21 and the negative rail to J22. The voltages depend on the coupling method and connection to the ADC. If the ADC VCM is not supplied to the amplifier and the amplifier is connected to the ADC in a dc-coupled fashion, users must set J21 to 4 V and J22 to –1 V. In ac-coupled configurations where the ADC VCM biases the ADC inputs, users can connect J21 to 5 V and J22 to GND.

2.2.3 ADC Analog Inputs

The EVM is configured to accept a single-ended input source and convert it to an ac-coupled differential signal using a transformer. The inputs to the ADC must be dc-biased, which is accomplished by using the ADC VCM output. The inputs are provided via SMA connectors J10 for ADC channel A, J11 for ADC channel B, J13 for ADC channel C, and J14 for ADC channel D. ADC input channel C also includes the option for ADC evaluation using an amplifier signal chain.

TI has tested this ADC with a variety of transformer brands, transformer configurations and terminations. For many applications, a single low-cost transformer can be used in the input signal chain to a very high degree of performance. Customers must select a transformer configuration based on their ADC input bandwidth frequency. To assist in this process, TI has swept the analog input frequency and plotted the resulting ADC SFDR performance with various transformers. Figure 1 and Figure 2 show the ADC performance using the Mini-Circuits TC1-1T, Mini-Circuits TC4-1W, and Coilcraft WBC1-1TLB in one- and two-transformer configurations, respectively. In both plots, the results were taken on an ADS6443, sampling at 80 MSPS and on the same input channel. The termination was changed according to the impedance ratio of the transformer used.

Using SMA input J2, users can evaluate the ADC using a THS4509 amplifier, which converts a single-ended input into a differential signal while providing 10 dB of signal gain. Users must enable the amplifier path by connecting JP6 1–2 and by shorting positions 1–2 on both surface-mount jumpers JP1 and JP2. At low input frequencies, the ADC represents a high input impedance and R10, R19, and C45 form a low-pass filter with a 3-db cutoff frequency of 70 MHz. Users must change these component values depending on the bandwidth of the signal they are digitizing to band-limit the input noise into the ADC. Using an excessively high cutoff frequency degrades the SNR of the system.

In a dc-coupled system, users must replace C46 and C47 with 0-Ω resistors and remove R9 and R18. The ADC VCM must be used to set the CM input of the amplifier by making sure R84 is populated with a 0-Ω resistor. Because the ADC has a common-mode voltage of 1.5 V, and because the THS4509 is not a rail-to-rail amplifier, users must adjust VCC to 4 V and –VCC to –1 V, which can be done by applying the respective voltages to J21 and J22.

For an ac-coupled system, users must use the voltage divider R9 and R18 to set the common-mode input of the amplifier, which must be set to the midpoint of the amplifier supply. C46 and C47 ac-couple the system, and the ADC inputs can then be biased by the R14 and R15 combination. Another ac-coupled approach, not supported on this EVM, would be to use a transformer at the outputs of the THS4509. In this case, the transformer would provide for ac-coupling, and one could bias the inputs of the ADC by feeding the ADC VCM to the transformer center tap on the secondary.

It must be noted that the THS4509 used on this EVM is pinout-compatible with the THS4508, THS4511, THS4513, and THS4520. Users can easily interchange the amplifier on this EVM and must pick the appropriate amplifier based on common-mode range, power supplies, and frequency of operation. TI application engineers can assist in the best selection of these amplifiers based on the user requirements.

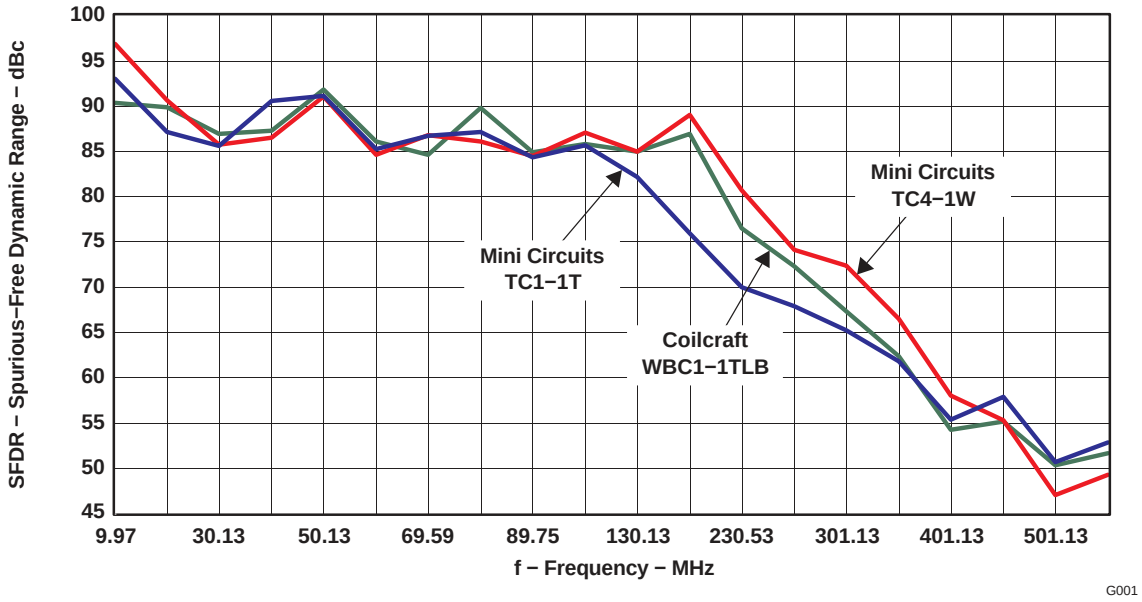


Figure 1. SFDR vs Frequency Using a Single Transformer

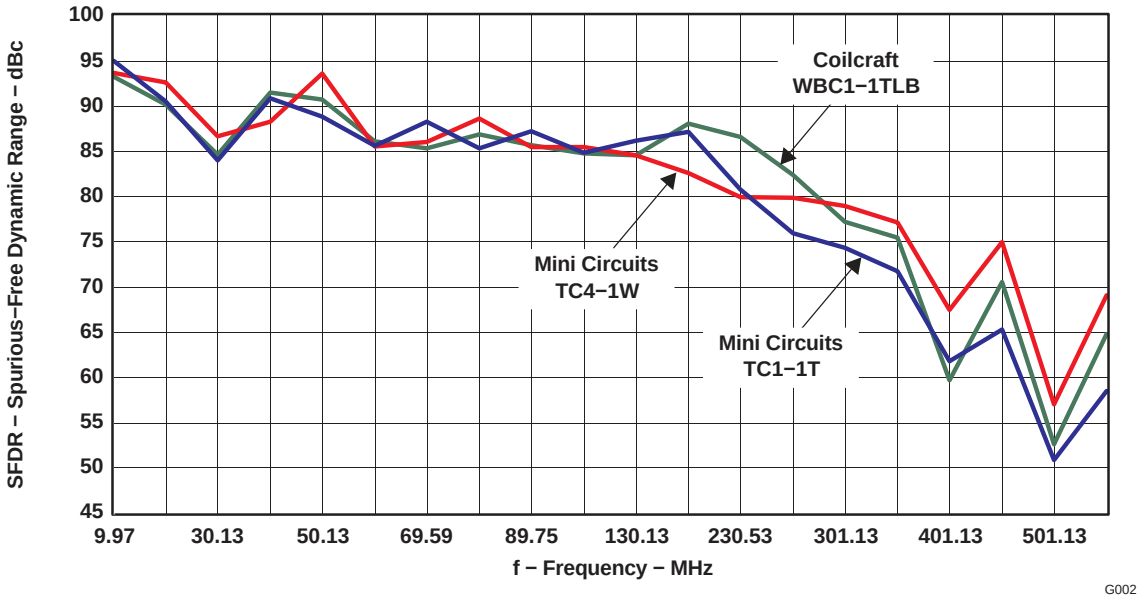


Figure 2. SFDR vs Frequency Using a Dual Transformer

2.2.4 ADC Clock Input

Users must connect a filtered, low-phase-noise clock input to J12. A transformer, T5, provides the conversion from a single-ended clock signal into a differential clock signal. When selecting the clock signal level, users must account for the transformer having an impedance ratio of 4, with a voltage step-up of 2.

2.2.5 ADC Digital Outputs

The ADS62xx ADC outputs serialized data, a bit clock (DCLK), and a frame clock (FCLK). These signals are brought to a high-density Samtec™ connector, J15. Users have three options in processing the ADC data.

1. Customers can use the mating logic analyzer breakout board and capture the ADC data using a logic analyzer. Users would be required to perform a software deserialization of the digital data before conducting analysis. Contact the factory for a breakout board for your logic analyzer.
2. Customers can create their own digital interface card which directly interfaces to the ADC. In this case, customers would design their mating digital interface board with the Samtec part number QSH-060-01-F-D-A, which is the companion part number to the EVM connector.
3. In most cases, customers can use a hardware deserialization solution such as the TSW1200. The TSW1200 features a powerful Xilinx™ Virtex 4 that comes preloaded with both 12-bit and 14-bit deserialization routines. In addition, customers can use the FPGA to develop their own deserializer and digital prototypes. The digital output of the TSW1200 easily plugs into logic analyzers or TI's own digital capture and analysis solution, the TSW1100.

2.2.6 Surface-Mount Jumper Selections

The EVM features surface-mount jumpers in cases where either the signal integrity is important or the functions are not often used. Table 2 summarizes these options.

Table 2. Surface Mount Jumpers

ADC Signal	Reference Designator	Default Selection	Optional Selection
RESET	J7	2–3, parallel mode operation	1–2, serial mode operation
SCLK	J6	Not populated, pin tied low	1–2, TSW1200 control over SCLK
SDATA	J8	Not populated, pin tied low	1–2, TSW1200 control over SDATA
SEN	J5	2–3: EVM J16 controls parallel operation modes	1–2, TSW1200 control over SEN
PD	J9	Not populated, pin tied low, device operational	1–2, TSW1200 control over PD
INC_M	JP1	2–3, Transformer-coupled analog input to channel C	1–2, Amplifier-coupled path to channel C
INC_P	JP2	2–3, Transformer-coupled analog input to channel C	1–2, Amplifier-coupled path to channel C

2.3 Deserialization and the TSW1200

While the specifics of the deserializer are out of the scope of this user's guide, TI has partnered up with Xilinx to deliver an open-source deserializer solution with application note documentation. When designing the deserializer, users must consult Xilinx application note XAPP866, hosted on the Xilinx website.

3 ADC Evaluation

This section describes how to set up a typical ADC evaluation system that is similar to what TI uses to perform testing for data sheet generation. Consequently, the information in this section is generic in nature and is applicable to all high-speed, high-resolution ADC evaluations. This section covers signal tone analysis, which yields ADC data sheet figures of merit such as signal-to-noise ratio (SNR) and spurious free dynamic range (SFDR).

3.1 Hardware Selection

To reveal the true performance of the ADC under evaluation, tremendous care must be taken in selecting both the ADC signal source and ADC clocking source. The hardware setup that TI uses for its analysis is shown graphically in Figure 3.

3.1.1 Analog Input Signal Generator

When choosing the quality of the ADC analog input source, one must consider both harmonic distortion performance of the signal generator and the noise performance of the source.

In many cases, the harmonic distortion performance of the signal generator is inferior to that of the ADC, and additional filtering is needed if users expect to reproduce the ADC SFDR numbers found in the data sheet. Users can easily evaluate the harmonic distortion of their signal generator by hooking it directly to a spectrum analyzer and measuring the power of the output signal and comparing that to the power of the integer multiples of the output signal frequency. If the harmonic distortion is worse than the ADC under evaluation, the ADC digitizes the performance of the signal generator and the ADC's true SFDR is masked. To alleviate this, it is recommended that users provide additional LC filtering after the signal generator output.

Another important metric when deciding on a signal generator is its noise performance. As with the distortion performance, if the noise performance is worse than that of the ADC under evaluation, the ADC digitizes the performance of the source. Noise can be broken into two components, broadband noise and close-in phase noise. Broadband noise can be improved by the LC filter added to improve distortion performance; however, the close-in phase noise typically cannot be improved by additional filtering. Therefore, when selecting an analog signal source it is extremely important to review the manufacturer's phase noise plots, and great care must be taken to choose a signal generator with the best phase-noise performance.

3.1.2 Clock Signal Generator

Equally important in the high-performance ADC evaluation setup is the selection of the clocking source. Most modern ADCs, the ADS62xx included, accept either a sinusoidal or a square-wave clock input. The key metric in selecting a clocking source is selecting a source with the lowest jitter. This becomes increasingly important as the ADC's input frequency (Fin) increases, because the ADC SNR evaluation setups can become jitter-limited (Tj) as shown by the following equation.

$$\text{SNR (dBc)} = 20 \log (2\pi \times \text{Fin} \times \text{Tj(rms)})$$

In theory, a square-wave source with femtosecond jitter would be ideal for an ADC evaluation setup. However, in practical terms, most commercially available square-wave generators offer jitter measured in picoseconds, which is too great for high-resolution ADC evaluation setups. Therefore, most evaluation setups rely on the ADC's internal clock buffer to convert a sinusoidal input signal into an ultralow-jitter square wave. When selecting a sinusoidal clocking source, it has been shown that phase noise has a direct impact on jitter performance. Consequently, great scrutiny must be applied to the phase-noise performance of the clocking signal generator. TI has found that high-Q monolithic crystal filters can improve the phase noise of the signal generator, and they become essential elements of the evaluation setup when high ADC input frequencies are being evaluated.

3.2 Coherent Input Frequency Selection

Typical ADC analysis requires users to collect the resulting time-domain data and perform a Fourier transform to analyze the data in the frequency domain. A stipulation of the Fourier transform is that the signal must be continuous-time; however, this is not practical when looking at a finite set of ADC samples, usually collected from a logic analyzer. Consequently, users typically apply a window function to minimize the time-domain discontinuities that arise when analyzing a finite set of samples. For ADC analysis, window functions have their own frequency signatures or lobes that distort both SNR and SFDR measurements of the ADC.

TI uses the concept of coherent sampling to work around the use of a window function. The central premise of coherent sampling entails that the input signal into the ADC is carefully chosen such that when a continuous-time signal is reconstructed from a finite sample set, no time-domain discontinuities exist. To achieve this, the input frequency must be an integer multiple of the ratio of the ADC's sample rate (f_s) and the number of samples collected from the logic analyzer (N_s). The ratio of f_s to N_s is typically referred to as the fundamental frequency (f_f). Determining the ADC input frequency is a two-step process. First, the users select the frequency of interest for evaluating the ADC; then they divide this by the fundamental frequency. This yields typically a non-integer value, which must be rounded to the nearest odd, preferably prime, integer. Once that integer, or frequency bin (f_{bin}), has been determined, users multiply this with the fundamental frequency to obtain a coherent frequency to program into their ADC input signal generator. The procedure is summarized as follows.

$$f_f = f_s/N_s$$

$$f_{bin} = \text{Odd\_round}(f_{desired}/f_f)$$

$$\text{Coherent frequency} = f_f \times f_{bin}$$

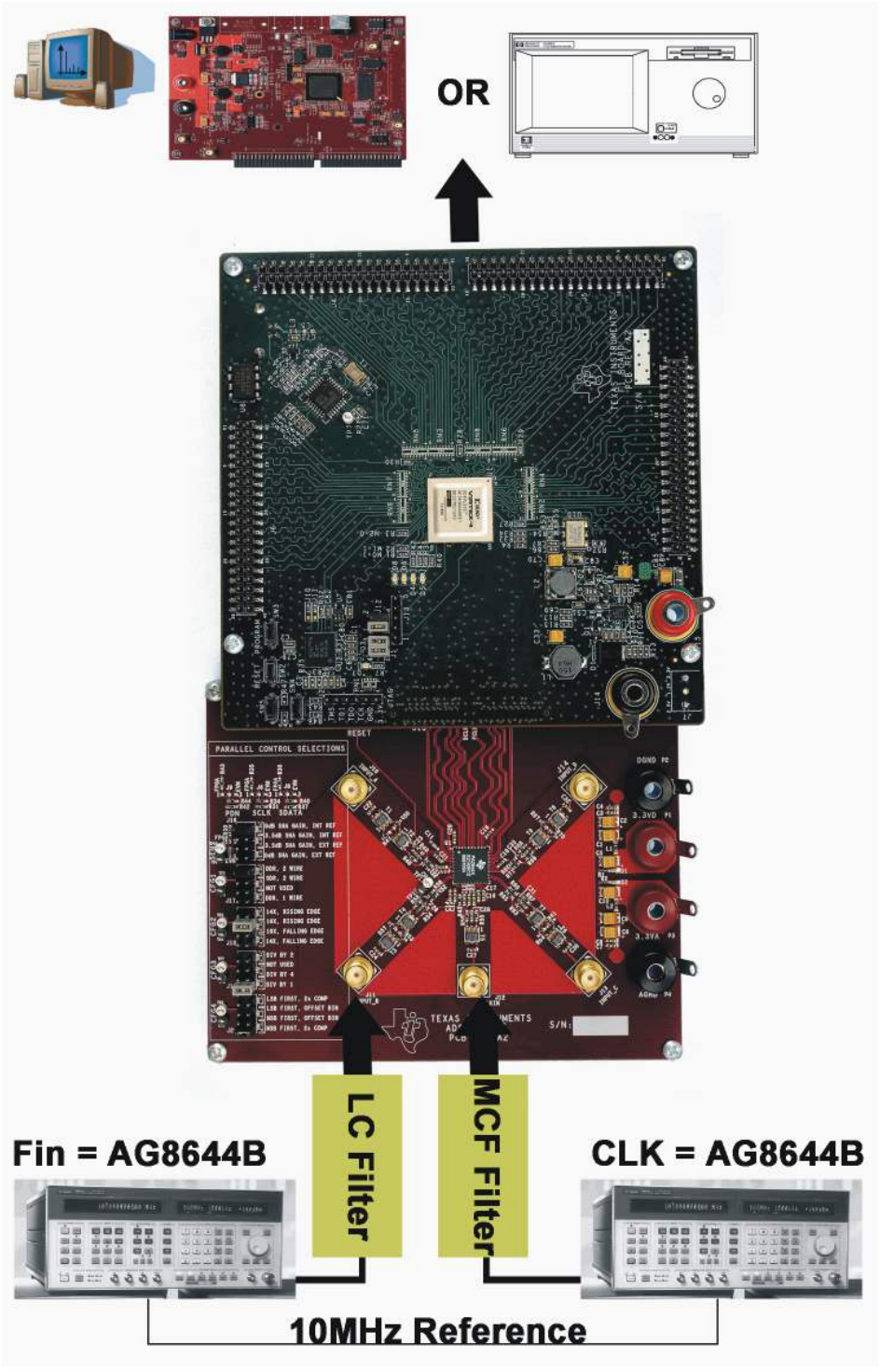


Figure 3. ADS62xxEVM Setup

4 Physical Description

This section describes the physical characteristics and PCB layout of the EVM.

4.1 PCB Layout

To be filled in, consult factory for details.

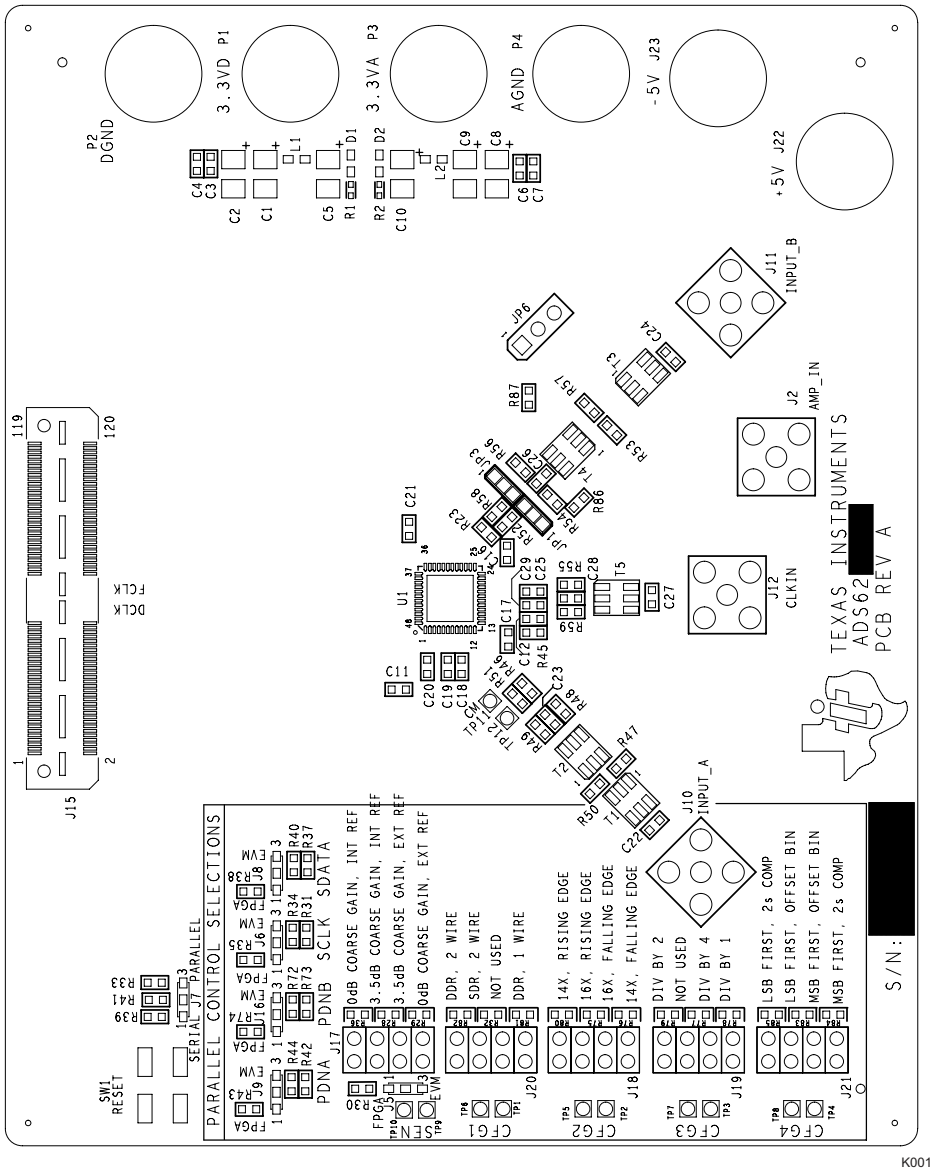


Figure 4. Layer 1, Top Layer

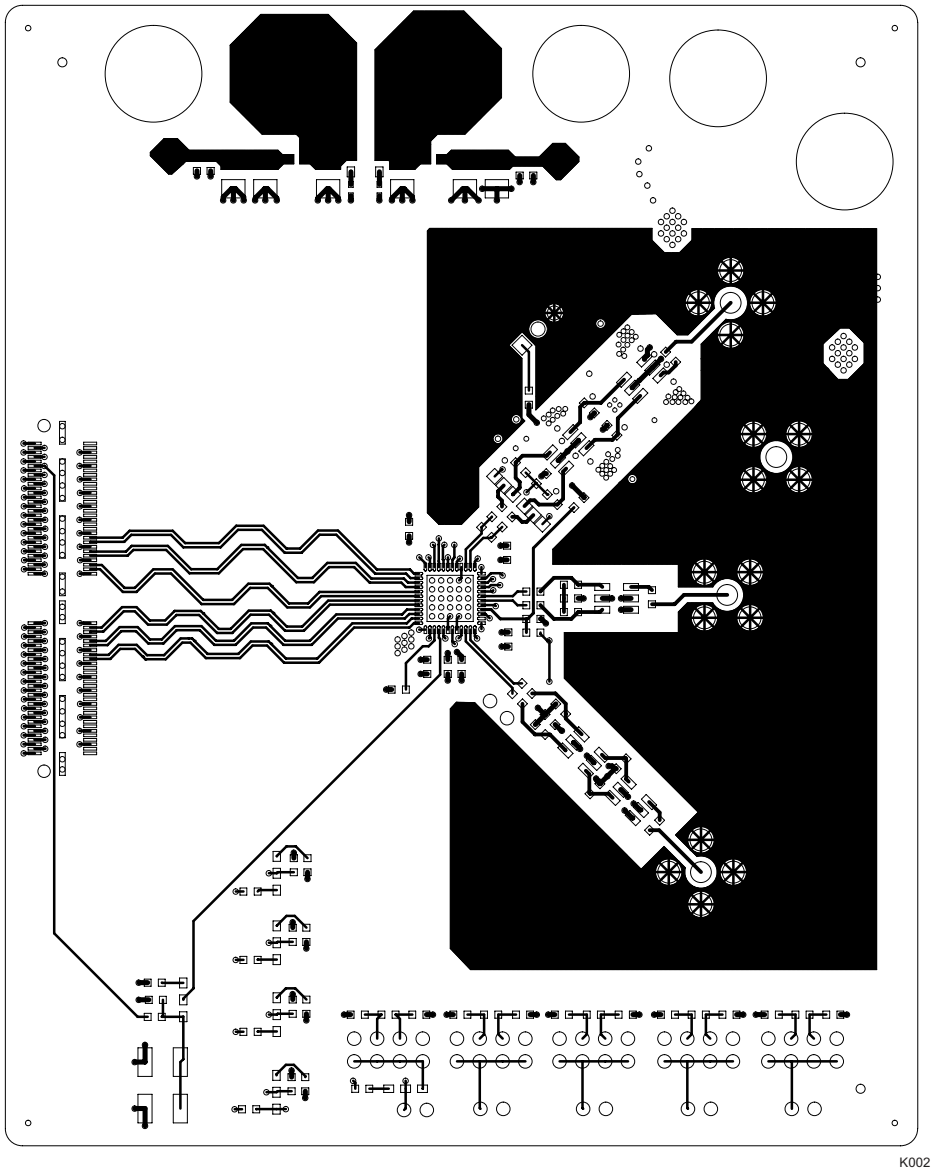


Figure 5. Layer 2, Ground Plane

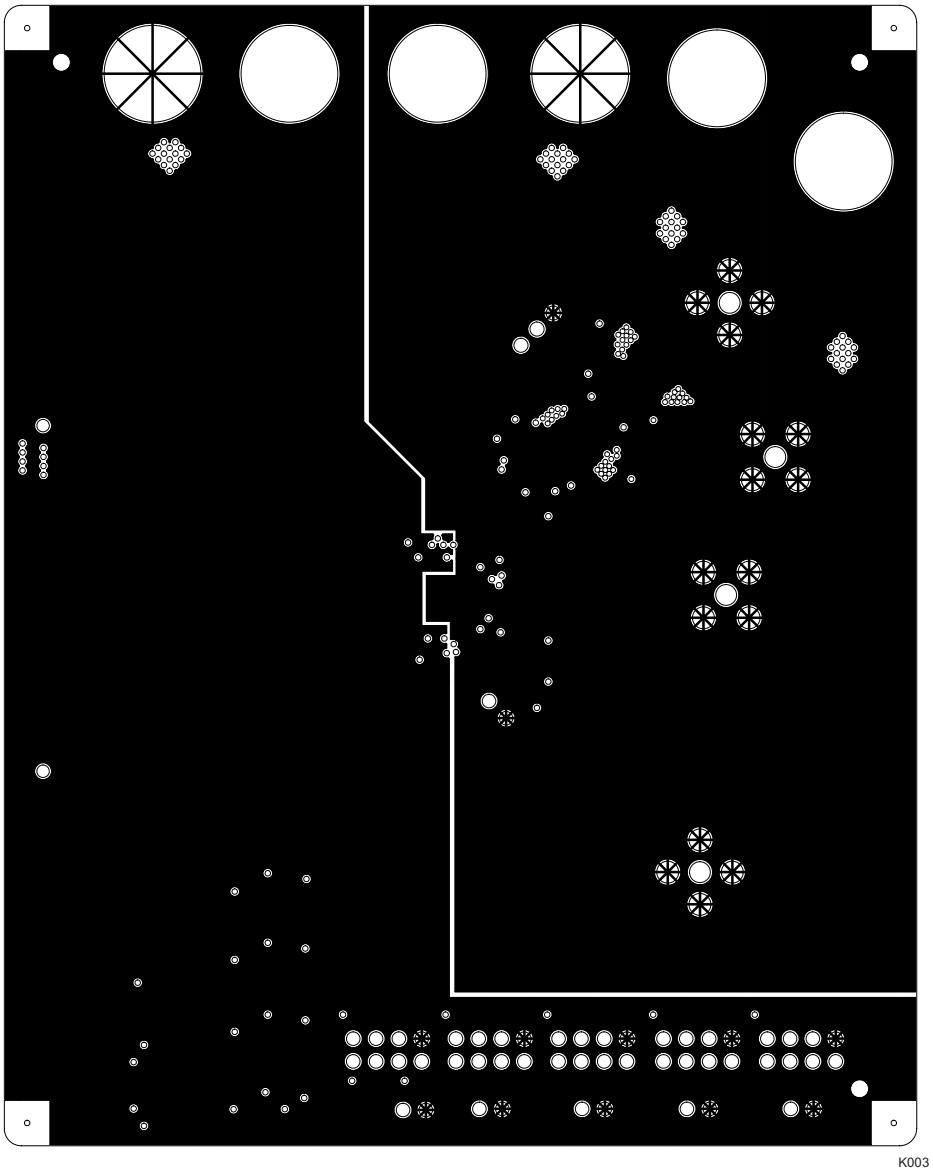


Figure 6. Layer 3, Power Plane #1

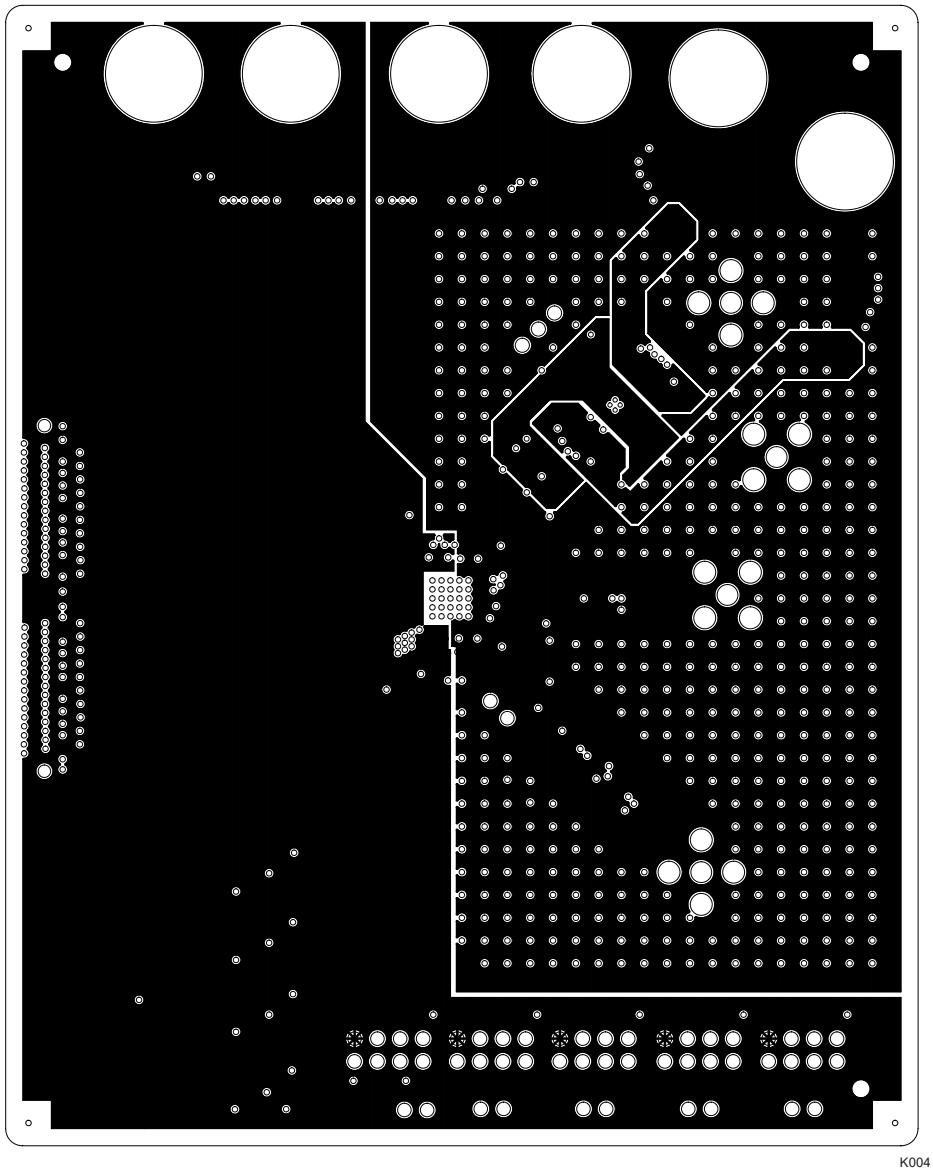


Figure 7. Layer 4, Power Plane #2

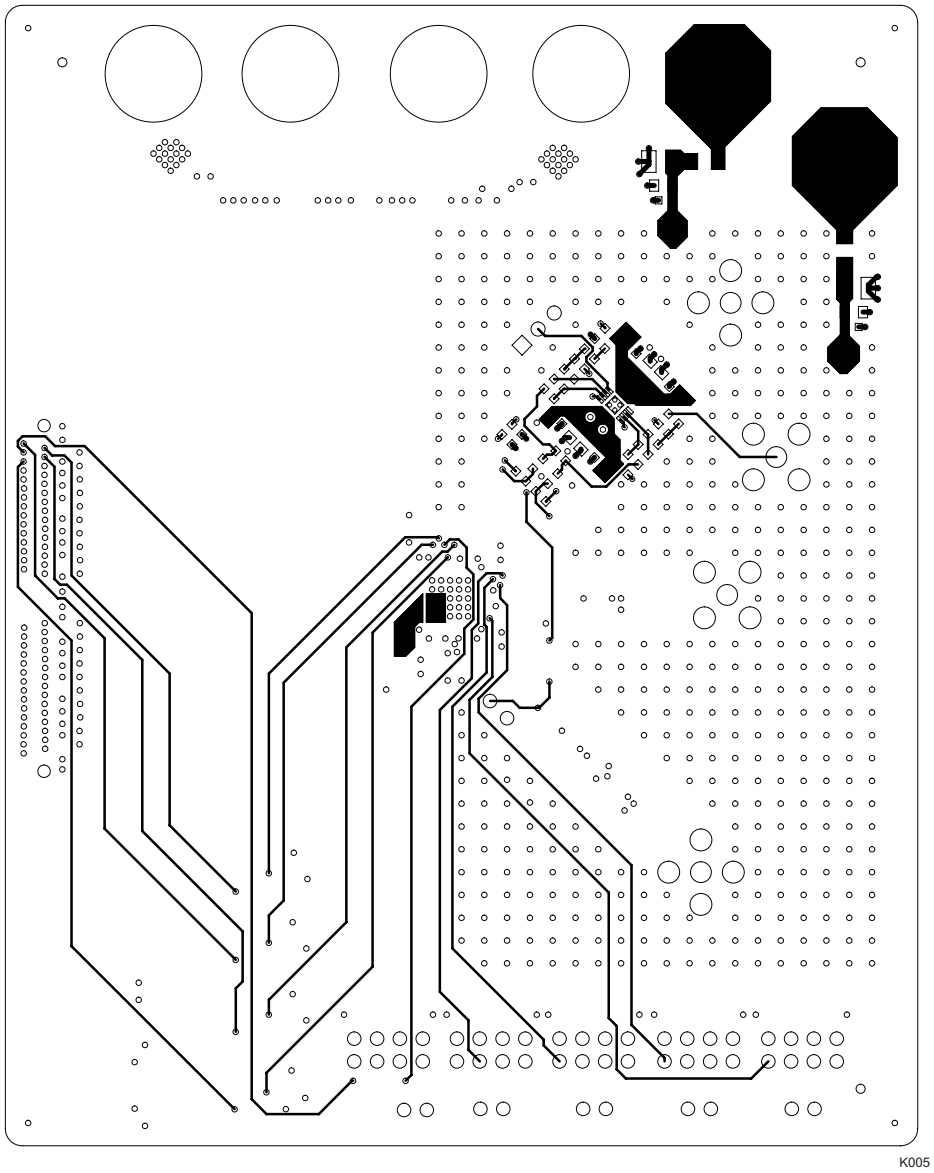


Figure 8. Layer 5, Ground Plane

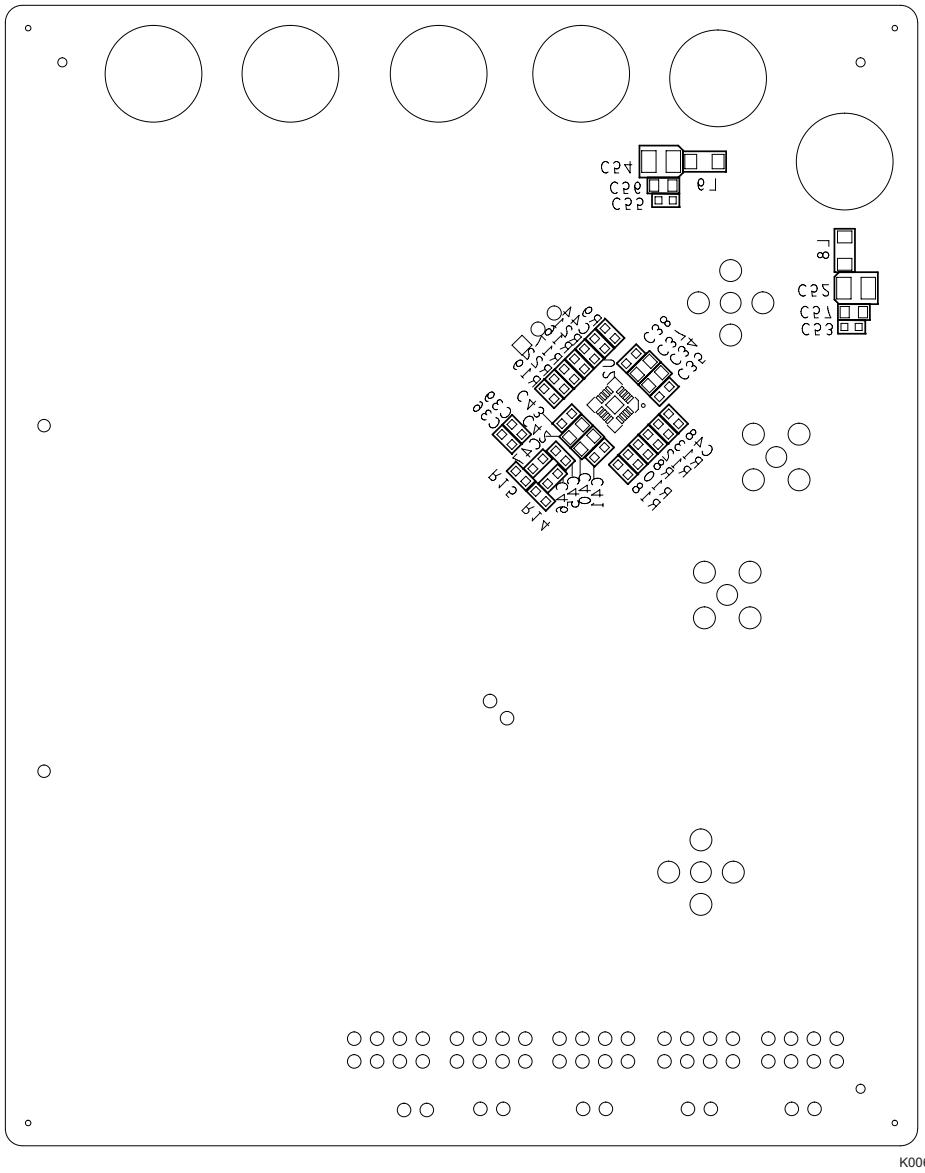


Figure 9. Layer 6, Bottom Layer

4.2 Bill of Materials

Table 3 is the bill of materials for the ADS62xxEVM.

Table 3. ADS62xxEVM Bill of Materials

Reference	Quantity	Not Installed	Part	Footprint	Part Number	Manufacturer
C1, C5, C8, C10	4		22 µF	smd_cap_1210_pol	ECS-T1CC226R	Panasonic
C2, C9	2		10 µF	smd_cap_1210_pol	ECS-H1CC106R	Panasonic
C3, C6	2		1 µF	603	ECJ-1VB1A105K	Panasonic
C4, C7, C22, C23, C24, C25, C26, C27, C28, C29	10		0.1 µF	603	GRM188R71H104KA93D	Murata
C11	1		2000 pF	603	GRM1885C1H202JA01D	Murata
C34, C37, C40, C42, C56, C57	6		10 µF	805	ECJ-2FB1A106K	Panasonic
C35, C36, C38, C39, C41, C43, C46, C47, C48, C53, C55	11		0.1 µF	603	ECJ-1VB1C104K	Panasonic
C44	1		0.22 µF	603	ECJ-1VB1A224K	Panasonic
C45	1		18 pF	603	ECJ-1VC1H180J	Panasonic
C52, C54	2		33 µF	TANT _B	TPSB336K016R0350	EPCOS Inc.
D1, D2	2		Green	smd_0603	LNJ312G8TRA	Panasonic
J2	1		SMA	SMA_THVT_320x320	142-0701-201	Johnson Components
J5, J7	2		SMD3P_BRIDGE	smd_bridge_0603	No part	
J6, J8, J9, J16	3		SMD3P_BRIDGE		No part	
J10, J11, J12	3		SMA	SMA_THVT_320x320	No part	Johnson Components
J15	1		CONN_QTH_30X2-D-A	conn_QTH_30X2-D-A	QTH-60-02-F-D-A	Samtec
J17, J18, J19, J20, J21	5		Header 4x2	hdr4X2_100ctr	90131-0124	Molex
L1, L2	2		Bead, 220–Ω	smt_0603	EXC-3BB221H	Panasonic
L8, L9	2		68	1206	EXC-ML32A680U	Panasonic
MP2	4		Screw machine, PH 4-40 × 3/8		PMS 440 0038 PH	Building Fasteners
MP3	4		Stand-off hex .5/4-40THR		1902C	Keystone Electronic
P1, P3, J22, J23	4		Banana jack, red	banana_jack	845R	SPC Technology
P2, P4	2		Banana jack, black	banana_jack	845B	SPC Technology
R1, R2	2		750 Ω	402	ERJ-3EKF7500V	Panasonic
R8, R22	2		348 Ω	603	ERJ-3EKF3480V	Panasonic
R9, R18	2		499 Ω	603	ERJ-3EKF4990V	Panasonic
R10, R19, R21, R48, R49, R54, R56	7		49.9 Ω	603	ERJ-3EKF49R9V	Panasonic
R12, R17, R31, R35, R37, R38, R39, R42, R43, R55, R59, R73, R74	13		100 Ω	603	ERJ-3EKF1000V	Panasonic
R13, R16	2		69.8 Ω	603	ERJ-3EKF69R8V	Panasonic

Table 3. ADS62xxEVM Bill of Materials (continued)

Reference	Quantity	Not Installed	Part	Footprint	Part Number	Manufacturer
R14, R15, R23	0	Not installed	200 Ω	603	ERJ-3EKF2000V	Panasonic
R28, R29, R32, R36, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85	15		1 kΩ	603	ERJ-3EKF1001V	Panasonic
R30, R84	2		0 Ω	603	ERJ-3GEY0R00V	Panasonic
R33, R34, R40, R41, R44, R72, R87	7		10 kΩ	603	ERJ-3EKF1002V	Panasonic
R45, R46, R51, R52, R58	5		10 Ω	603	ERJ-3EKF10R0V	Panasonic
R47, R50, R53, R57	4		200 Ω	603	ERJ-3EKF2000V	Panasonic
SW1	1		Switch, pushbutton	switch_reset	KT11P3JM	C & K Switch
TP1, TP2, TP3, TP4, TP9, TP12	6		Test point, black	testpoint	5001	Keystone
TP5, TP6, TP7, TP8, TP10, TP11	6		Test point, white	testpoint	5002	Keystone
T1,T2,T3,T4	4		WBC1-1TLB		WBC1-1TLB	Coilcraft
T5	1		TC4-1W		TC4-1W	Mini-Circuits
U1	1		ADS62xx	QFN48		
U2	1		THS4509	QFN16	THS4509RGTT	TI
	5		Conn. jumper, shorting		S9000-ND	Digi-Key

4.3 PCB Schematics

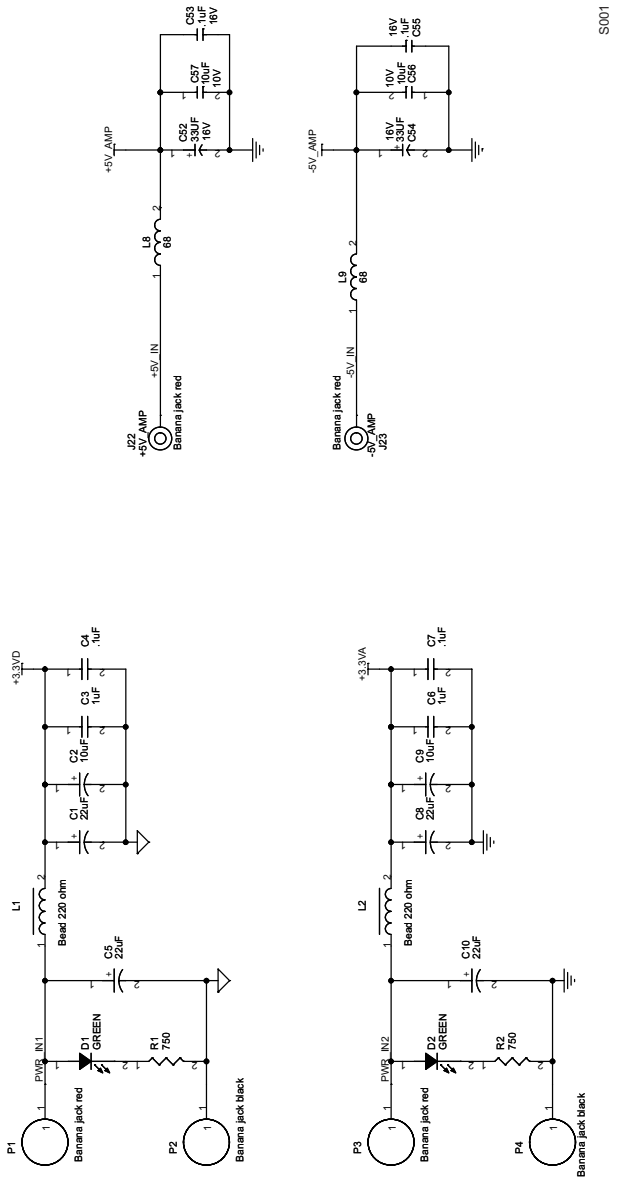


Figure 10. Sheet 1 of 5

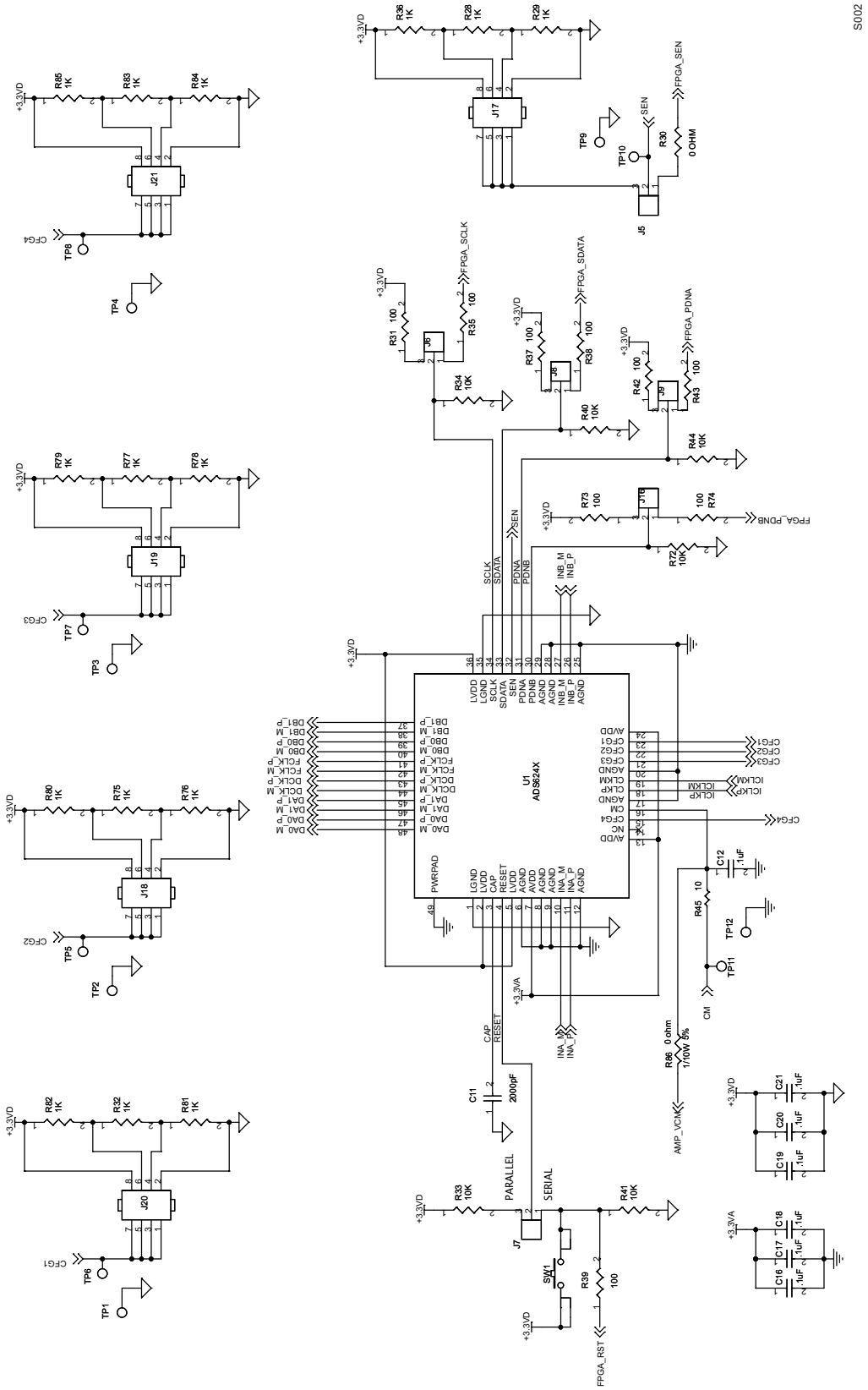


Figure 11. Sheet 2 of 5

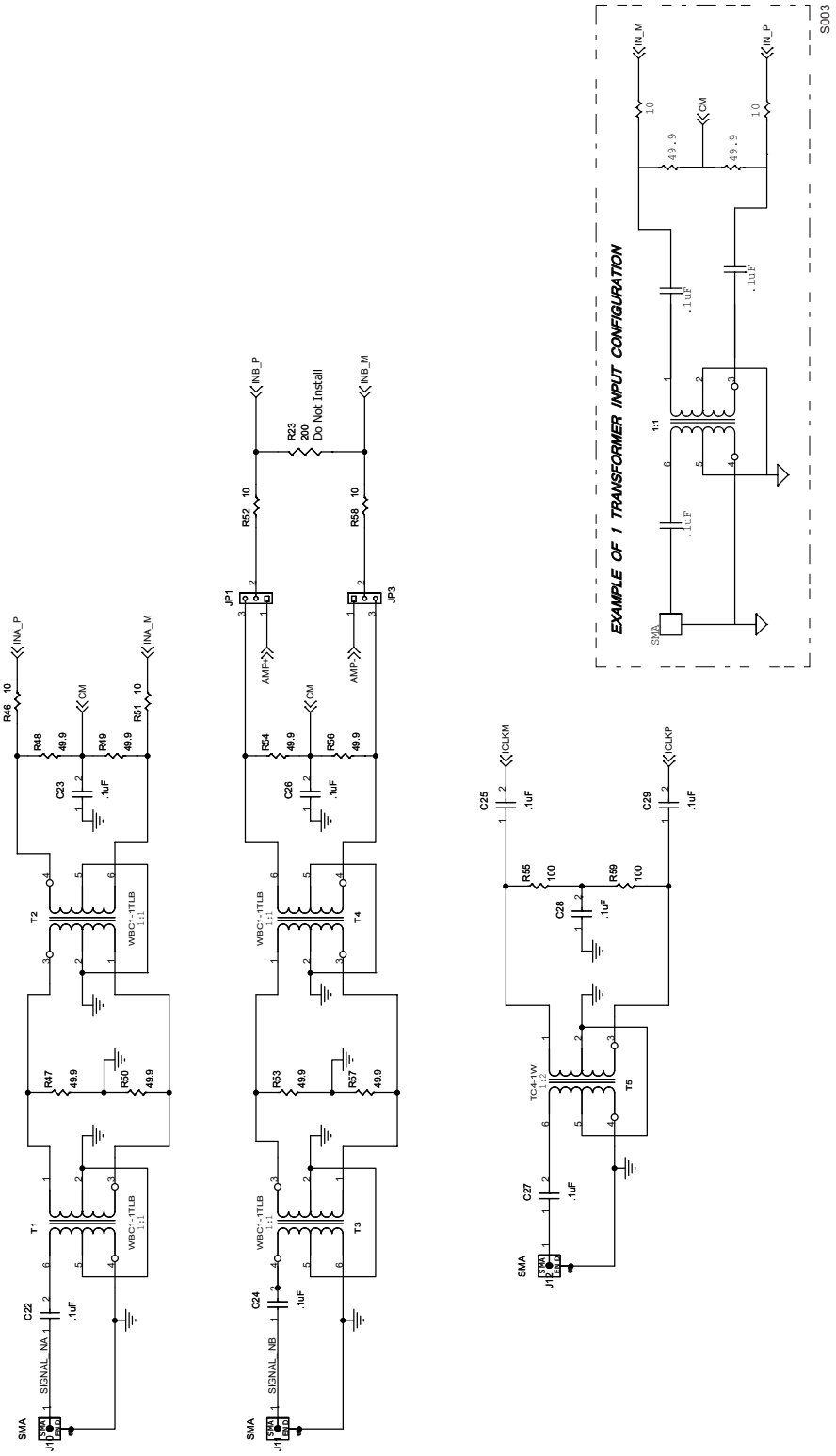


Figure 12. Sheet 3 of 5

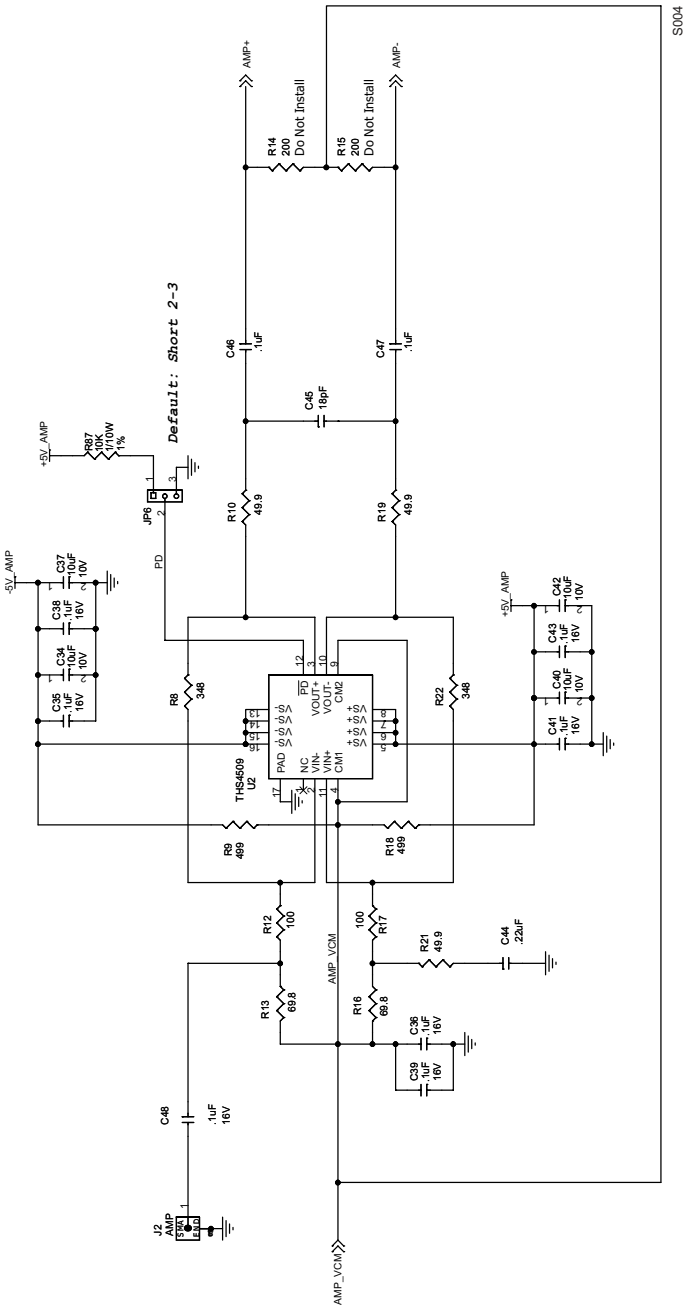
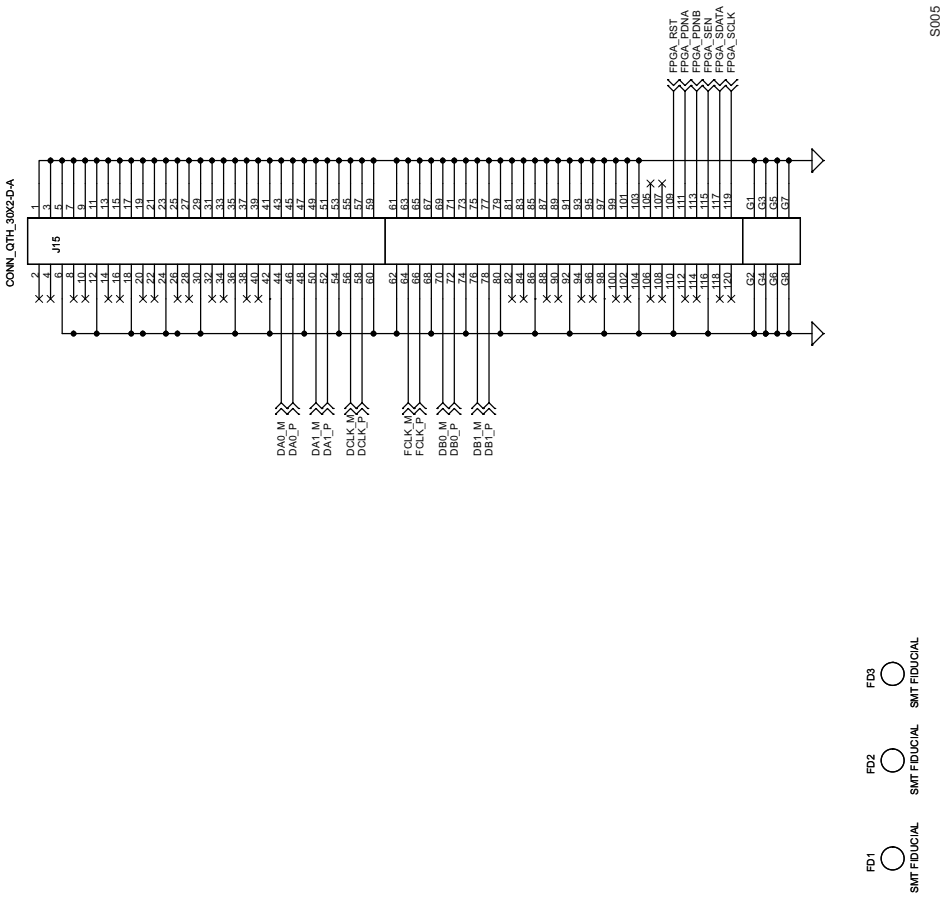


Figure 13. Sheet 4 of 5



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It is important to operate this EVM within the input voltage range of -3 V to 3.8 V and the output voltage range of -3 V to 3.8 V.

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During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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