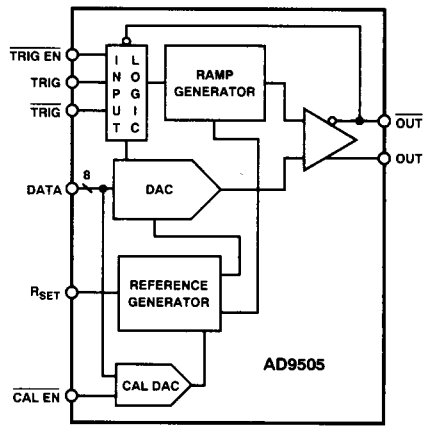
Digitally Programmable Pulse Edge Delay Vernier

AD9505

FEATURES
60 MHz Update Rate
±1.5 LSB Dynamic Nonlinearity
100 MHz Update Rate
±5 LSB Dynamic Nonlinearity
On-the-Fly Delay Update
8-Bit Resolution
2.5 ns to 25 ns Full-Scale Range
10 ps Incremental Delay
On-Board Calibration DAC

APPLICATIONS
ATE Pattern Generator
Programmable Pulse Generator
Frequency-Agile Clock Generator
Precise Pulse Phase Delay
Variable Duty Cycle Clock
Laser Printers
High Speed PWM
Line-to-Line Deskew

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9505 is a high performance, digitally programmable timing vernier with "on-the-fly" update capability. The delay from the triggering edge to the output is proportional to the 8-bit delay data.

With the timing capacitor and CalDAC included on the die, external components are reduced and manual trim of full-scale range is not required. A single external resistor sets the nominal full scale, and fine tuning can be accomplished under processor control. Pulse edge placement can be controlled to 10 ps resolution when full scale is set to its minimum value of 2.5 ns.

The AD9505 is designed specifically for applications requiring dynamic delay update such as ATE pulse pattern generation and very high speed, pulse width modulation. A new delay value is latched into the DAC on the positive edge of each TRIGGER pulse. This permits generation of high speed, pseudo-random pulse patterns with edges controlled to very precise increments.

Logic input and output levels are compatible with ECL-10K. TRIGGER and OUTPUT signals are differential to assure maximum noise immunity and minimum jitter when interfacing to any ECL logic family. An ECL midpoint reference is included for single-ended input interface.

Only 650 mW is required from a single −5.2 V power supply. This makes it possible to package the AD9505 in plastic PLCC. As a result, dense PC board layout is made possible. The AD9505KP is rated for operation from 0°C to +70°C.

PRODUCT HIGHLIGHTS

1. On-the-Fly Delay Update
2. Low Power—650 mW
3. Single Power Supply
4. 10K ECL Compatible

AD9505–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V; R_{SET} = 62 Ω; FSR = 4.1 ns; R_L = 100 Ω to −2 V)

Parameter	Temp	Test Level	Min	Typ	Max	Units
RESOLUTION			8			Bits
ACCURACY[1]						
Differential Nonlinearity[2]	+25°C	I		±0.5	±1	LSB
Integral Nonlinearity[2]	+25°C	I		±0.75	±1.75	LSB
Dynamic Integral Nonlinearity[3]	+25°C	V		±1		LSB
	Full	V		±2		LSB
Monotonicity	+25°C	I		Guaranteed		
DIGITAL INPUTS						
Logic "1" Voltage	Full	VI	−1.1			V
Logic "0" Voltage	Full	VI			−1.5	V
Logic "1" Input Current	Full	VI			25	μA
Logic "0" Input Current	Full	VI			25	μA
ECL Midpoint Reference	Full	VI	−1.38		−1.17	V
Input Capacitance	+25°C	V		3		pF
TRIG EN Setup Time (t_{SU})[4]	+25°C	V		1.5		ns
TRIG EN Hold Time (t_H)[5]	+25°C	V		2.5		ns
Data Setup Time (t_{DSU})[6]	+25°C	V		1		ns
Data Hold Time (t_{DH})[6]	+25°C	V		3		ns
Minimum Trigger Pulse Width High	Full	V		2		ns
DIGITAL OUTPUT						
Logic "1" Voltage	Full	IV	−1.0			V
Logic "0" Voltage	Full	IV			−1.63	V
DYNAMIC PERFORMANCE[1]						
Maximum Trigger Rate	+25°C	I	60			MHz
Minimum Propagation Delay (t_{PD})	+25°C					
FSR = 4 ns		I	4		6	ns
FSR = 20 ns		V		7		ns
Minimum Propagation Delay TC	Full	V		6		ps/°C
Full-Scale Range TC	Full	V		1		ps/°C
Delay Uncertainty	+25°C	V		6		ps
Output Rise Time	+25°C	V		900		ps
Output Fall Time	+25°C	V		900		ps
Output Pulse Width	+25°C	I	3.2	3.9	4.6	ns
POWER SUPPLY[7]						
Negative Supply Current (−5.2 V)	Full	VI		125	150	mA
Power Dissipation	Full	VI		650	780	mW
Power Supply Rejection Ratio[8]						
Full-Scale Range Sensitivity	+25°C	I		100	275	ps/V
Minimum Propagation Delay Sensitivity	+25°C	I		50	200	ps/V

NOTES
[1]With full scale set at 4.1 ns and 60 MHz TRIGGER rate.
[2]Measured with delay data changing at a slow rate and trigger at 60 MHz (Best Fit).
[3]Measured with delay changing on each trigger at 60 MHz.
[4]TRIGGER ENABLE must remain stable for the specified time prior to the leading edge of TRIGGER.
[5]TRIGGER ENABLE must remain stable for the specified time after the leading edge of TRIGGER.
[6]The DATA inputs must be stable for the specified times prior to and after the leading edge of TRIGGER.
[7]Supply voltage should remain stable within ±5% for normal operation.
[8]Measured at ±5% of V_{EE}.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Negative Supply Voltage (V_{EE}) . . . . . −7 V
Digital Input Voltage Range . . . . . GND to V_{EE}
Trigger Input Voltage Range . . . . . GND to V_{EE}
Minimum R_{SET} . . . . . 20 Ω
Digital Output Current (Sourcing) . . . . . 30 mA
Operating Temperature Range
AD9505KP . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[2] . . . . . +175°C
Vapor Phase Soldering (1 minute)[3] . . . . . +220°C

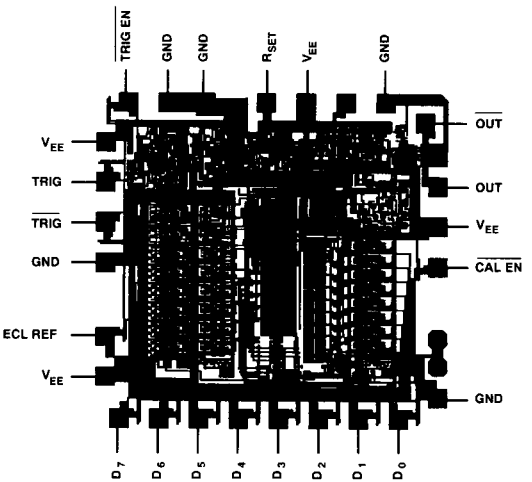
NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability may be impaired. Functional operability under any of these conditions is not necessarily implied.
[2]Typical thermal impedance:
28-Lead PLCC, θ_{JA} = 55°C/W; θ_{JC} = 15°C/W.
[3]Prior to vapor phase soldering, plastic packages should receive a minimum of 8 hours bake-out at 110°C to assure that moisture trapped during shipping and storage is driven out.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9505KP	0°C to +70°C	Plastic PLCC	P-28A

*For outline information see Package Information section.

MECHANICAL INFORMATION

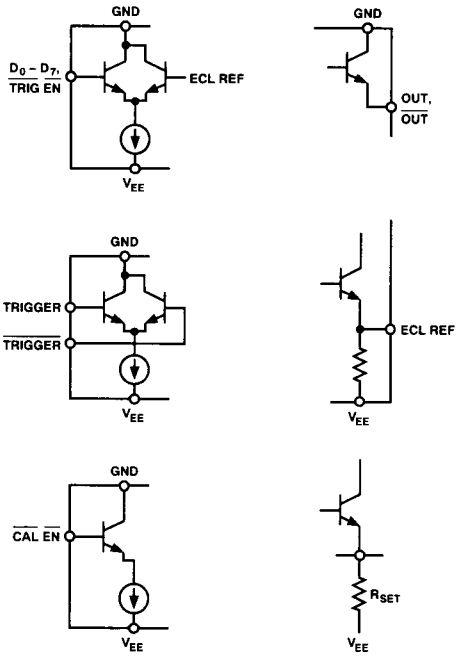


Die Dimensions . . . . . 101 × 97 × 15 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Aluminum
Backing . . . . . None
Substrate Potential . . . . . V_{EE}
Passivation . . . . . Oxynitride
Die Attach . . . . . Epoxy or Gold Eutectic
Bond Diameter . . . . 1.25 mil, Aluminum; Ultrasonic Bonding
. . . . . or 1 mil, Gold; Gold Ball Bonding

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Periodically sample tested.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



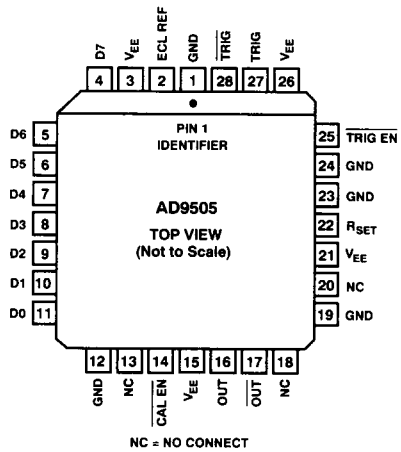
Equivalent Circuits

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	GND	Ground Return; Digital Current.
2	ECL REF	Logic Midpoint Reference.
3	V_{EE}	Negative Supply; −5.2 V, Digital.
4	D7	Delay Data Bit 7 (MSB).
5	D6	Delay Data Bit 6.
6	D5	Delay Data Bit 5.
7	D4	Delay Data Bit 4.
8	D3	Delay Data Bit 3.
9	D2	Delay Data Bit 2.
10	D1	Delay Data Bit 1.
11	D0	Delay Data Bit 0 (LSB).
12	GND	Ground Return; Digital Current.
13	N/C	No Connection: Do Not Use as a Tie Point.
14	$\overline{CAL}$ $\overline{EN}$	Calibrate Enable; Cal Is Initiated When Logic "Zero" Applied.
15	V_{EE}	Negative Supply; −5.2 V, Digital.
16	OUT	True Output Signal.
17	$\overline{OUT}$	Complementary Output.
18	NC	No Connection; Do Not Use as a Tie Point.
19	GND	Ground Return; Digital Current.
20	NC	No Connection; Do Not Use as a Tie Point.
21	V_{EE}	Negative Supply; −5.2 V, Analog.
22	R_{SET}	Resistor to Set Nominal Full Scale.
23	GND	Ground Return; Analog Current.
24	GND	Ground Return; Analog Current.
25	$\overline{TRIG}$ $\overline{EN}$	Trigger Enable; Enabled When Logic "Zero" Applied.
26	V_{EE}	Negative Supply, −5.2 V, Digital.
27	TRIG	Trigger Input; Initiates Delay.
28	$\overline{TRIG}$	Complementary Trigger Input.

PIN CONFIGURATION

28-Lead PLCC



FUNCTIONAL DESCRIPTION

The AD9505 comprises a ramp generator, DAC, and comparator. A TRIGGER signal initiates a linear ramp and latches data into the DAC. The comparator monitors the ramp signal versus the DAC reference level. When the ramp crosses the level set by the DAC, an OUTPUT signal of constant pulse width is generated.

The comparator also generates an internal signal which resets the ramp and returns the DAC latch to its transparent state. The DAC then switches and settles to the voltage corresponding to its next data word. It is then ready for the next triggering event.

TIMING CONSIDERATIONS

As shown in the timing diagram below, the leading edge of TRIGGER initiates a delay cycle whenever $\overline{\text{TRIGGER ENABLE}}$ is a logic zero. Minimum setup and hold times must be observed to assure that DATA is properly latched into the DAC and the TRIGGER is enabled.

For "on-the-fly" operation, the DATA setup time should be a minimum of 5 ns. This is necessary to assure minimum settling time for the DAC. The DAC latches become transparent immediately following the previous delayed event. Figure 1 demonstrates typical nonlinearity versus update rate with new DATA for each TRIGGER (FSR = 4 ns).

Some applications for delay verniers do not require the delay value to change on a TRIGGER-by-TRIGGER basis. In cases where delay DATA changes relatively slowly, dynamic linearity will improve markedly. An octal holding register may be required since the AD9505 data inputs are latches rather than registers. Figure 2 shows nonlinearity versus TRIGGER rate with DATA update at 100 Hz (FSR = 4 ns).

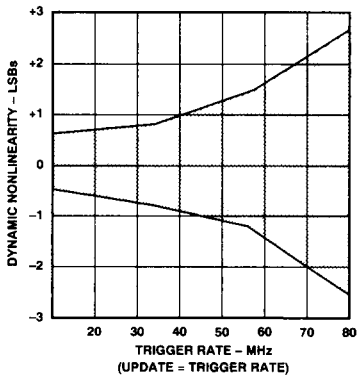


Figure 1. Dynamic Nonlinearity vs. Update Rate

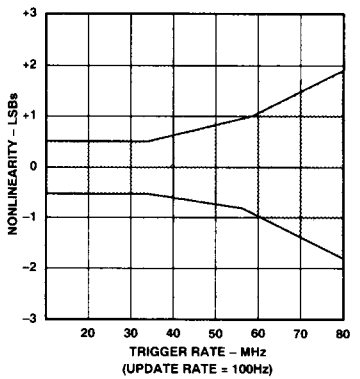


Figure 2. Nonlinearity vs. Trigger Rate

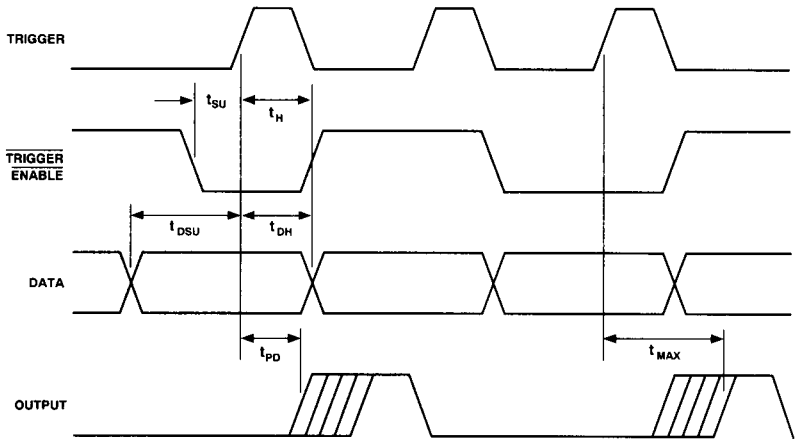


Figure 3. Timing Diagram

Because of timing overhead such as setup times, minimum propagation delay, and ramp/DAC settling time, it is not possible for the programmed delay to be as long as the full TRIGGER interval. The table below lists maximum full-scale ranges for various trigger rates to maintain rated linearity.

Trigger Rate	Trigger Interval	Maximum FSR
60 MHz	16.7 ns	5 ns
50 MHz	20 ns	11 ns
25 MHz	40 ns	15 ns

Figure 4 illustrates dynamic nonlinearity versus full-scale range for 20 MHz, 60 MHz, and 100 MHz TRIGGER rates.

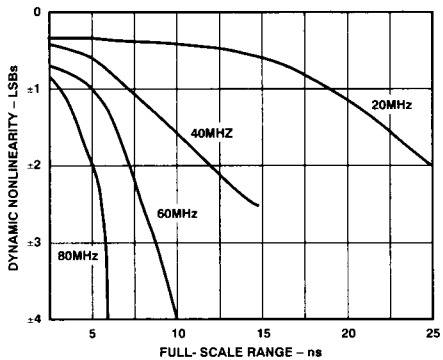


Figure 4. Dynamic Nonlinearity vs. FSR

The AD9505 outputs a constant width pulse whose leading edge is delayed with respect to the leading edge of TRIGGER. Total delay is the sum of a minimum delay and the programmed delay or:

$$t_{TOTAL} = t_{PD} + t_{PROG}$$

Minimum delay (t_{PD}) consists of the fixed propagation delay of the input logic and the comparator plus a variable ramp delay. The ramp delay is due to an offset between the reset ramp level and the most positive DAC value. This offset is necessary to avoid false output signals when the ramp resets. The offset is constant, but the delay varies as a function of the slope of the ramp. Thus, this portion of t_{PD} will be proportional to the full-scale range.

Minimum delay can be calculated by the equation:

$$t_{PD} = 4.7\ ns + (0.1 \times FSR)$$

Minimum delays for various full-scale delays are shown in Figure 5.

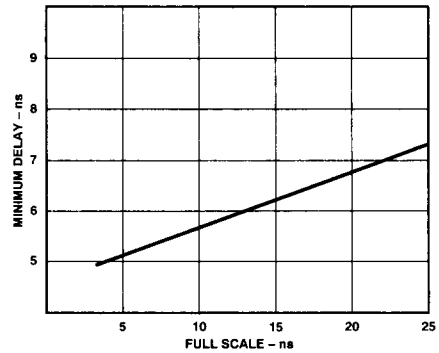


Figure 5. Minimum Delay

Full-scale programmable range is set by an external R_{SET} in combination with an internal capacitor with a nominal value of 14 pF. Full-scale range is found by the equation:

$$FSR = 4.7 \cdot R_{SET} \cdot C_{INT}$$

or R_{SET} is found by:

$$R_{SET} = FSR/(65.8 \cdot 10^{-12})$$

For best overall performance, the full-scale range for the AD9505 should be limited to the range from 2.5 ns to 25 ns. It should be noted that data sheet specifications are based on a full-scale range of 4.1 ns. Figure 6 shows the required value for R_{SET} for various nominal full-scale ranges.

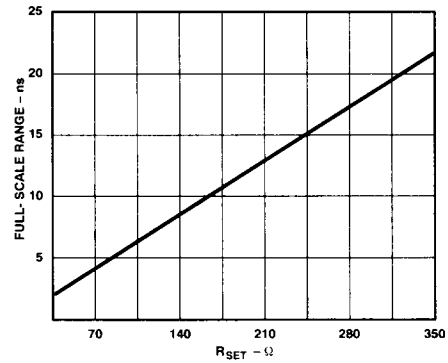


Figure 6. Full Scale vs. R_{SET}

Although operation at longer delay ranges is possible, certain characteristics may degrade to undesirable levels. The first characteristic to degrade will be FSR tempco. The reference circuit which regulates this tempco is effective over the R_{SET} range from 35 Ω to 350 Ω. Further imbalance in this circuit causes rapid degradation of tempco.

Additionally, the jitter (which is actually a measure of timing repeatability) increases rapidly. Since the purpose of the AD9505 is to provide repeatable delay with fine incremental resolution, jitter is undesirable. Typical jitter versus full-scale delay is illustrated below. Data for Figure 7 was taken with the AD9505 operating at low data update..

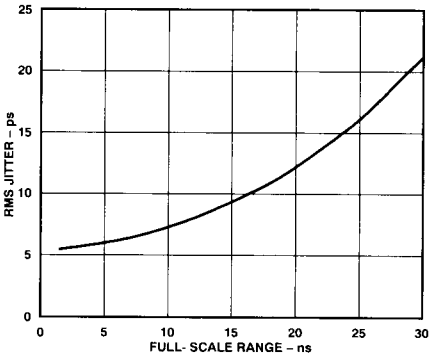


Figure 7. Jitter vs. FSR

The tolerance on the internal capacitor is approximately ±20%. Thus, the full-scale range calculated by the above equations will have a like tolerance. Because many applications for timing verniers require better absolute range tolerance as well as tight matching between multiple devices, the AD9505 also includes an on-board CalDAC. This facilitates fine tuning the FSR under processor control.

APPLICATIONS INFORMATION

Fine-Tuning FSR with the CalDAC

Data for the CalDAC is applied to the same 8-bit bus as delay DATA. When CAL Enable is low, data is loaded into the CalDAC; when it goes high, the data is latched. (It should be noted that this data is also loaded into the delay DATA latches. Therefore, a new delay value should be loaded prior to testing the new calibration value or returning to normal operation.)

Since the capacitor may vary by ±20%, the CalDAC's range is proportional to FSR so it is always slightly more than ±20%. Additionally, it is guaranteed monotonic by design so it will operate properly in a closed correction loop. The effective resolution of the calibration is ±1/4 LSB referred to the full-scale range.

R_{SET} is selected per the equations under Timing Considerations. Starting with a midscale code in the CalDAC, its input should be increased to lengthen FSR and vice versa.

As long as CAL ENABLE is held high, the CalDAC will retain its calibration code until another calibration cycle is initiated. The user should note that the calibration code is lost when power is removed. The CalDAC latch may come up in any state. Therefore, a power-up cal should always be performed.

Layout Considerations

Although the AD9505 performs an essentially digital function, its incremental resolution and accuracy depend upon linear analog subcircuits. The internal comparator measures millivolt levels in order to resolve very small time increments. Therefore, high frequency analog layout techniques should be employed in order to obtain rated performance.

Driving the device with a differential signal will enhance the repeatability of the timing accuracy. The complementary outputs should also be loaded equally to balance output digital switching currents.

Grounding and power supply decoupling should receive special attention. The ground plane should cover as much as possible of the component side or first interior layer of the board. Avoid signal runs on the component side of the board between the device and ground plane.

All ground pins should be connected directly to the ground plane. In systems with split grounds, all ground pins of the AD9505 should be connected to the Analog Ground. A single point connection from the ground plane of the AD9505 to digital ground is required for return currents for the digital interface.

All V_{EE} pins should be decoupled with 0.01 μF to 0.1 μF chip capacitors. Circuit connections from the capacitors to package pins and ground should be as short as possible to minimize inductance.

The analog V_{EE}, Pin 21, should require no special treatment except on boards with considerable digital switching current. In those cases, a ferrite bead in series with the supply connection should provide satisfactory isolation. Otherwise, normal decoupling should be adequate.

In most cases, sockets should be avoided, even for prototyping. The contacts in sockets add capacitance and inductance which usually degrade dynamic performance of high performance ICs such as the AD9505. If socketing is necessary, and the user can tolerate small losses in performance, the best-known socket through our experience is the Methode 213-028-602 for the PLCC.

An evaluation board is available. Its part number is AD9505PCB.