![TEXAS INSTRUMENTS]

DRV8804

SLVSAW4F –JULY 2011–REVISED DECEMBER 2015

DRV8804 Quad Serial Interface Low-Side Driver IC

1 Features

- 4-Channel Protected Low-Side Driver
  - Four N-Channel MOSFETs With Overcurrent Protection
  - Integrated Inductive Clamp Diodes
  - Serial Interface
- DW Package: 1.5-A (Single Channel On) / 800-mA (Four Channels On) Maximum Drive Current per Channel (at 25°C)
- PWP Package: 2-A (Single Channel On) / 1-A (Four Channels On) Maximum Drive Current per Channel (at 25°C, With Proper PCB Heatsinking)
- 8.2-V to 60-V Operating Supply Voltage Range
- Thermally-Enhanced Surface Mount Package

2 Applications

- Relay Drivers
- Unipolar Stepper Motor Drivers
- Solenoid Drivers
- General Low-Side Switch Applications

3 Description

The DRV8804 provides a 4-channel low-side driver with overcurrent protection. It has built-in diodes to clamp turnoff transients generated by inductive loads and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

In the SOIC (DW) package, the DRV8804 can supply up to 1.5-A (one channel on) or 800-mA (all channels on) continuous output current per channel, at 25°C. In the HTSSOP (PWP) package, it can supply up to 2-A (one channel on) or 1-A (four channels on) continuous output current per channel, at 25°C with proper PCB heatsinking.

A serial interface is provided including a serial data output, which can be daisy-chained to control multiple devices with one serial interface.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature, and faults are indicated by a fault output pin.

The DRV8804 is available in a 20-pin, thermally-enhanced SOIC package and a 16-pin HTSSOP package (Eco-friendly: RoHS & no Sb/Br).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8804	SOIC (20)	12.80 mm × 7.50 mm
	HTSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
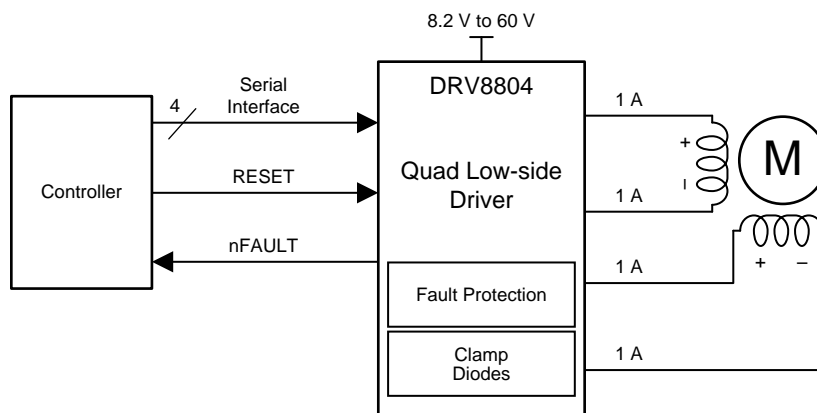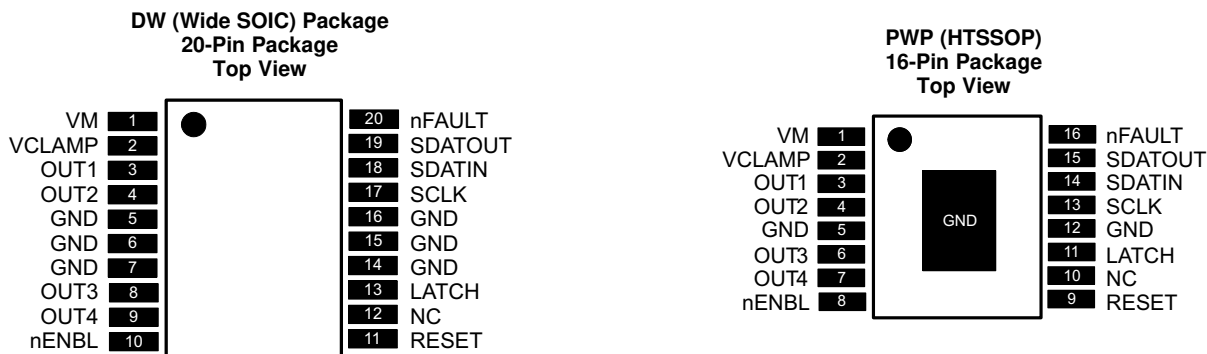
Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2014) to Revision F **Page**

• Changed Catch Diodes to Clamp Diodes in *Features* 1

• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Product Folder Links: *DRV8804*

5 Pin Configuration and Functions

DW (Wide SOIC) Package
20-Pin Package
Top View

VM	1	20	nFAULT
VCLAMP	2	19	SDATOUT
OUT1	3	18	SDATIN
OUT2	4	17	SCLK
GND	5	16	GND
GND	6	15	GND
GND	7	14	GND
OUT3	8	13	LATCH
OUT4	9	12	NC
nENBL	10	11	RESET

PWP (HTSSOP)
16-Pin Package
Top View

VM	1	16	nFAULT
VCLAMP	2	15	SDATOUT
OUT1	3	14	SDATIN
OUT2	4	13	SCLK
GND	5	12	GND
OUT3	6	11	LATCH
OUT4	7	10	NC
nENBL	8	9	RESET

GND

Pin Functions

PIN			I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	SOIC	HTSSOP			
POWER AND GROUND					
GND	5, 6, 7, 14, 15, 16	5, 12, PPAD	—	Device ground	All pins must be connected to GND.
VM	1	1	—	Device power supply	Connect to motor supply (8.2 V - 60 V).
CONTROL					
LATCH	13	11	I	Latch input	Rising edge latches shift register to output stage – internal pulldown
nENBL	10	8	I	Enable input	Active low enables outputs – internal pulldown
RESET	11	9	I	Reset input	Active-high reset input initializes internal logic – internal pulldown
SCLK	17	13	I	Serial clock	Serial clock input – internal pulldown
SDATIN	18	14	I	Serial data input	Serial data input – internal pulldown
SDATOUT	19	15	O	Serial data output	Serial data output; push-pull structure; see serial interface section for details
STATUS					
nFAULT	20	16	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent)
OUTPUT					
OUT1	3	3	O	Output 1	Connect to load 1
OUT2	4	4	O	Output 2	Connect to load 2
OUT3	8	6	O	Output 3	Connect to load 3
OUT4	9	7	O	Output 4	Connect to load 4
VCLAMP	2	2	—	Output clamp voltage	Connect to VM supply, or zener diode to VM supply

(1) Directions: I = input, O = output, OD = open-drain output

Product Folder Links: *DRV8804*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
VM	Power supply voltage	−0.3	65	V
VOUTx	Output voltage	−0.3	65	V
VCLAMP	Clamp voltage	−0.3	65	V
SDATOUT, nFAULT	Output current		20	mA
	Peak clamp diode current		2	A
	DC or RMS clamp diode current		1	A
	Digital input pin voltage	−0.5	7	V
SDATOUT, nFAULT	Digital output pin voltage	−0.5	7	V
	Peak motor drive output current, t < 1 µs	Internally limited		A
	Continuous total power dissipation	See _Thermal Information_		
T_J	Operating virtual junction temperature	−40	150	°C
T_{stg}	Storage temperature	−60	150	°C

(1) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_M	Power supply voltage	8.2		60	V
V_{CLAMP}	Output clamp voltage[1]	0		60	V
I_{OUT}	Continuous output current, single channel on, T_A = 25°C, SOIC package[2]			1.5	A
	Continuous output current, four channels on, T_A = 25°C, SOIC package[2]			0.8	
	Continuous output current, single channel on, T_A = 25°C, HTSSOP package[2]			2	
	Continuous output current, four channels on, T_A = 25°C, HTSSOP package[2]			1	

(1) V_{CLAMP} is used only to supply the clamp diodes. It is not a power supply input.
(2) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC[1]		DRV8804		UNIT
		DW (SOIC)	PWP (HTSSOP)	
		20 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.7	39.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	24.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	20.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.9	20.1	°C/W

(1) For more information about traditional and new thermal metrics, see the _Semiconductor and IC Package Thermal Metrics_ application report, SPRA953.

Thermal Information (continued)

THERMAL METRIC[1]		DRV8804		UNIT
		DW (SOIC)	PWP (HTSSOP)	
		20 PINS	16 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.3	°C/W

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

|	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V		1.6	2.1	mA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising			8.2	V
LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	VIN = 0	−20		20	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
R_{PD}	Pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
SDATOUT OUTPUT (PUSH-PULL OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
V_{OH}	Output high voltage	I_O = 100 µA, V_M = 11 V - 60 V, peak			6.5	V
		I_O = 100 µA, V_M = 11 V - 60 V, steady state	3.3	4.5	5.6	
		I_O = 100 µA, V_M = 8.2 V - 11 V, steady state	2.5			
I_{SRC}	Output source current	V_M = 24 V			1	mA
I_{SNK}	Output sink current	V_M = 24 V			5	mA
LOW-SIDE FETS						
$R_{DS(ON)}$	FET on resistance	V_M = 24 V, I_O = 700 mA, T_J = 25°C		0.5		Ω
		V_M = 24 V, I_O = 700 mA, T_J = 85°C		0.75	0.8	
I_{OFF}	Off-state leakage current		−50		50	µA
HIGH-SIDE DIODES						
V_F	Diode forward voltage	V_M = 24 V, I_O = 700 mA, T_J = 25°C		1.2		V
I_{OFF}	Off-state leakage current	V_M = 24 V, T_J = 25°C	−50		50	µA
OUTPUTS						
t_R	Rise time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
t_F	Fall time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2.3		3.8	A
t_{OCP}	Overcurrent protection deglitch time			3.5		µs
t_{RETRY}	Overcurrent protection retry time			1.2		ms
t_{TSD}	Thermal shutdown temperature	Die temperature[1]	150	160	180	°C

(1) Not production tested.

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
1	t_{CYC}	Clock cycle time	62			ns
2	t_{CLKH}	Clock high time	25			ns
3	t_{CLKL}	Clock low time	25			ns
4	$t_{SU(SDATIN)}$	Setup time, SDATIN to SCLK	5			ns
5	$t_{H(SDATIN)}$	Hold time, SDATIN to SCLK	1			ns
6	$t_{D(SDATOUT)}$	Delay time, SCLK to SDATOUT, no external pullup resistor, C_{OUT} = 100 pF		50	100	ns
7	$t_{W(LATCH)}$	Pulse width, LATCH	200			ns
8	$t_{OE(ENABLE)}$	Enable time, nENBL to output low		60		ns
9	$t_{D(LATCH)}$	Delay time, LATCH to output change		200		ns
—	t_{RESET}	RESET pulse width	20			µs
10	$t_{D(RESET)}$	Reset delay before clock	20			µs
11	$t_{STARTUP}$	Start-up delay VM applied before clock	55			µs

(1)   Not production tested.
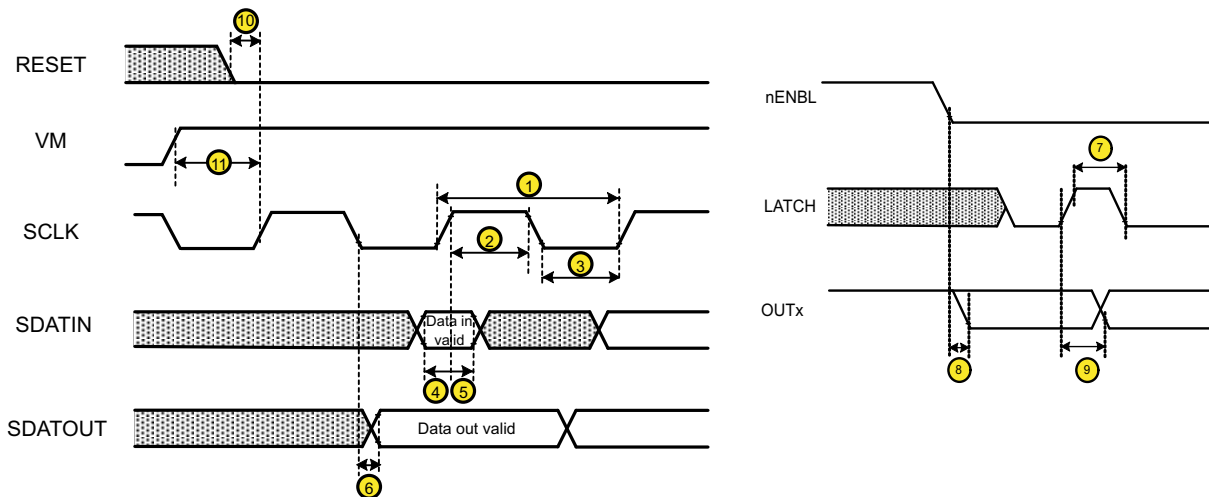
More than 400 ns of delay should exist between the final SCLK rising edge and the LATCH rising edge. This ensures that the last data bit is shifted into the device properly.

Figure 1. DRV8804 Timing Requirements
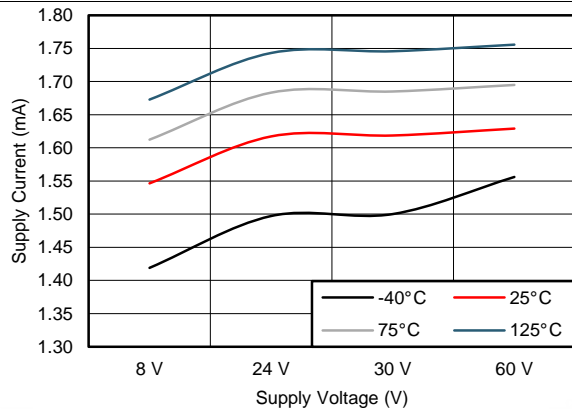
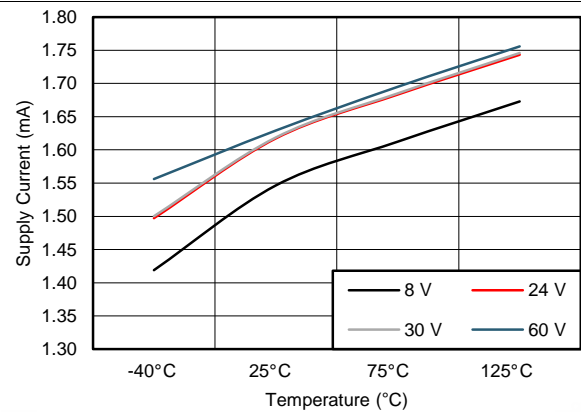## 6.7 Typical Characteristics

Figure 2. Supply Current over V_M

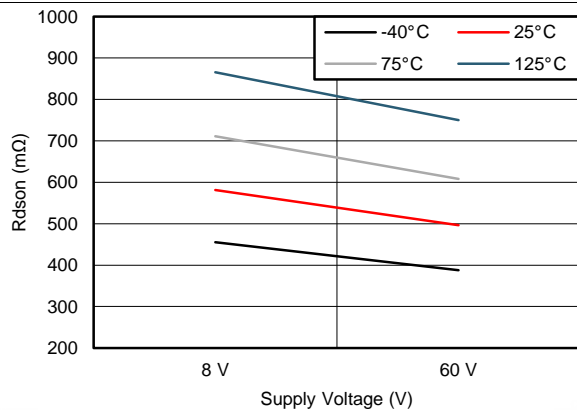Figure 3. Supply Current Over Temperature

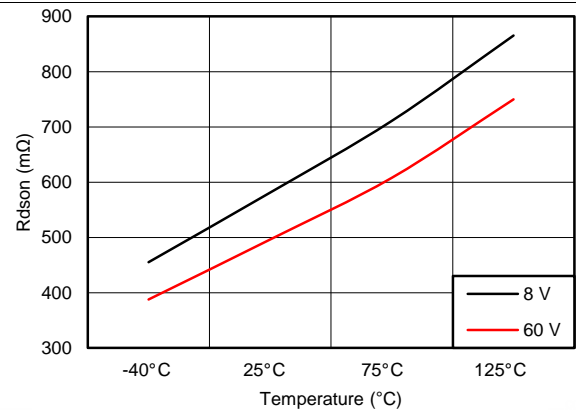

Figure 4. $R_{DS(on)}$ Over VM

Figure 5. $R_{DS(on)}$ Over Temperature

7 Detailed Description

7.1 Overview

The DRV8804 is an integrated 4-channel low side driver solution for a low side switch application. A serial interface controls the low-side driver outputs and allows for multiple drivers to be chained together and save space on communication lines. The four low-side driver outputs consist of four N-channel MOSFETs that have a typical $R_{DS(on)}$ of 500 mΩ. A single motor supply input V_M serves as device power and is internally regulated to power the low side gate drive. The device outputs can be disabled by bringing nENBL pin logic high. This device has several safety features including integrated overcurrent protection that limits the motor current to a fixed maximum above which the device will shut down. Thermal shutdown protection enables the device to automatically shut down if the die temperature exceeds a TTSD limit and will restart once the die reaches a safe temperature. UVLO protection will disable all circuitry in the device if V_M drops below the undervoltage lockout threshold.

7.2 Functional Block Diagram
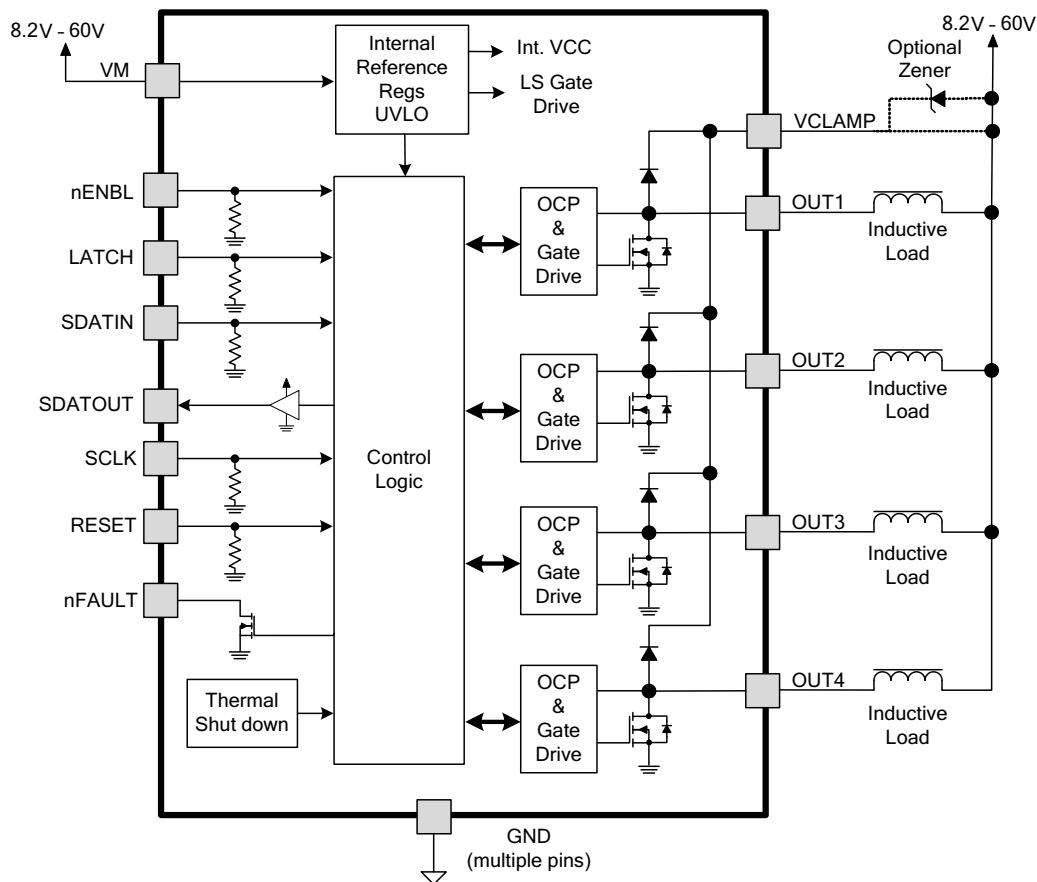
7.3 Feature Description

7.3.1 Output Drivers

The DRV8804 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. It can also be connected to a Zener or TVS diode to V_M, allowing the switch voltage to exceed the main supply voltage V_M. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

7.3.2 Serial Interface Operation

The DRV8804 is controlled with a simple serial interface. Logically, the interface is shown in Figure 6.
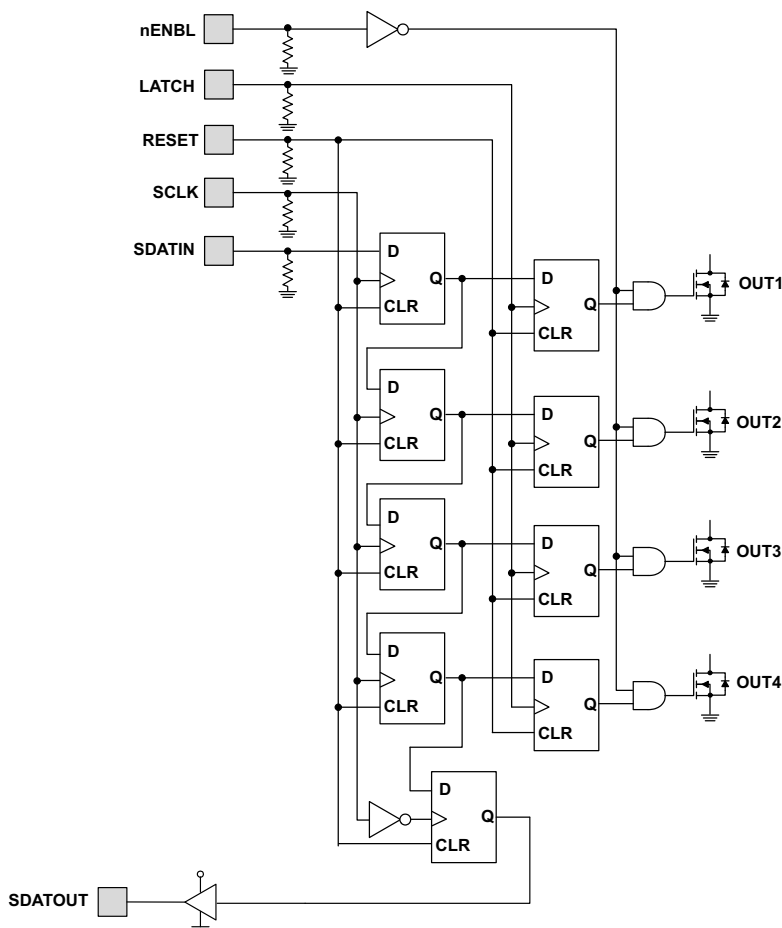

Figure 6. Serial Interface Operation

Data is shifted into a temporary holding shift register in the part using the SDATIN pin, one bit at each rising edge of the SCLK pin. Data is simultaneously shifted out of the SDATOUT pin, allowing multiple devices to be daisy-chained onto one serial port. Note that the SDATOUT pin has a push-pull driver, which can support driving another DRV8804 SDATIN pin at clock frequencies of up to 1 MHz without an external pullup. A pullup resistor can be used between SDATOUT and an external 5-V logic supply to support higher clock frequencies. TI recommends a resistor value greater than 1 kΩ. The SDATOUT pin is capable of approximately 1-mA source and 5-mA sink. To supply logic signals to a lower-voltage microcontroller, use a resistor divider from SDATOUT to GND.

A rising edge on the LATCH pin latches the data from the temporary shift register into the output stage.

Feature Description (continued)

7.3.3 nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. nENBL does not affect the operation of the serial interface logic. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic, including the OCP fault. All serial interface registers are cleared. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so driving RESET at power up is not required.

7.3.4 Protection Circuits

The DRV8804 is fully protected against undervoltage, overcurrent, and overtemperature events.

7.3.4.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the t_{OCP} deglitch time (approximately 3.5 μs), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the t_{RETRY} retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or VM is removed and re-applied.

7.3.4.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

7.3.4.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout (UVLO) threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when V_M rises above the UVLO threshold.

7.4 Device Functional Modes

When the nENBL pin of the DRV8804 is pulled logic low, the open-drain FET outputs are enabled. Having the device be enabled at logic low allows for the use of long data lines in a high noise environment that do not unintentionally enable the device with coupled noise. The device will still shift data through the SDATIN / SDATOUT lines and SCLK line regardless of the state of the nENBL pin.

Once data has been moved into each of the four shift register lines the LATCH pin can be pulled high to output the state of the four shift registers. Once LATCH is pulled high the state of the four shift registers is placed in a logical AND with the inverse state of the nENBL pin. If the nENBL pin is logic low input and the LATCH pin is logic high the open-drain output of that driver channel will be turned on.

If the device detects that V_M has dropped below the UVLO threshold, it will immediately enter a state where all the internal logic is disabled. The device stays in a disabled state until V_M rises above the UVLO threshold and all internal logic is then reset. During an Overcurrent Protection (OCP) event the device removes gate drive for one t_{RETRY} interval and the nFAULT pin is driven low. The fault is cleared immediately if RESET is activated or V_M is removed and re-applied.

Product Folder Links: *DRV8804*

8   Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1   Application Information

The DRV8804 can be used to drive one unipolar stepper motor.
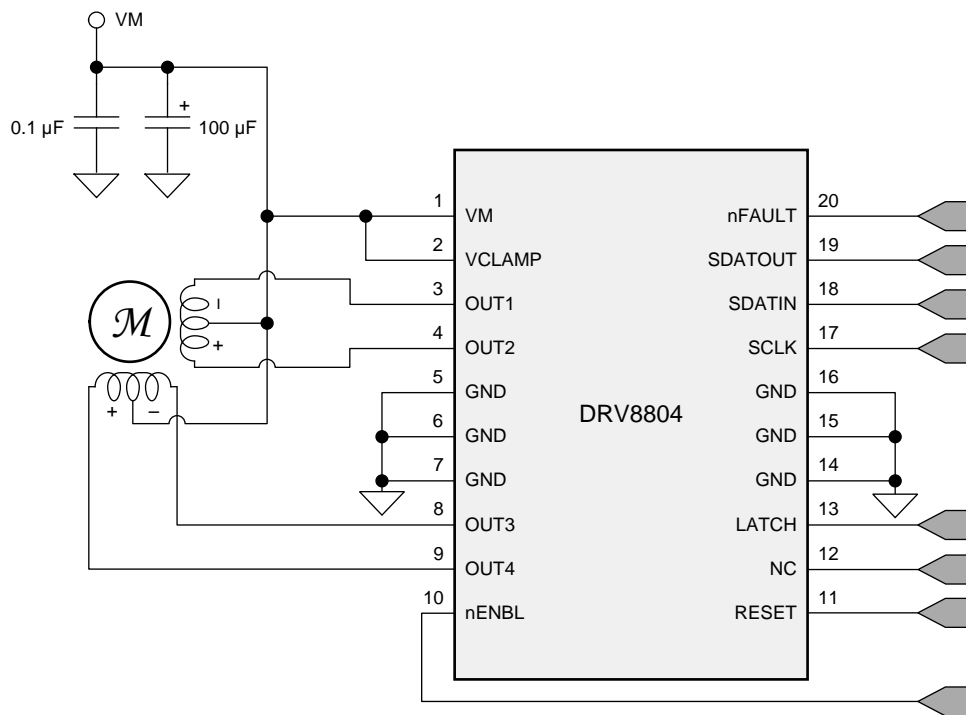
8.2   Typical Application

Figure 7.   Typical Application Schematic

8.2.1   Design Requirements

Table 1 lists the design parameters for this design example.

Table 1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	V_M	24 V
Motor Winding Resistance	R_L	7.4 Ω/phase
Motor Full Step Angle	θ_{step}	1.8°/step
Motor Rated Current	I_{RATED}	0.75 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired torque. A higher voltage shortens the current rise time in the coils of the stepper motor allowing the motor to produce a greater average torque. Using a higher voltage also allows the motor to operate at a faster speed than a lower voltage.
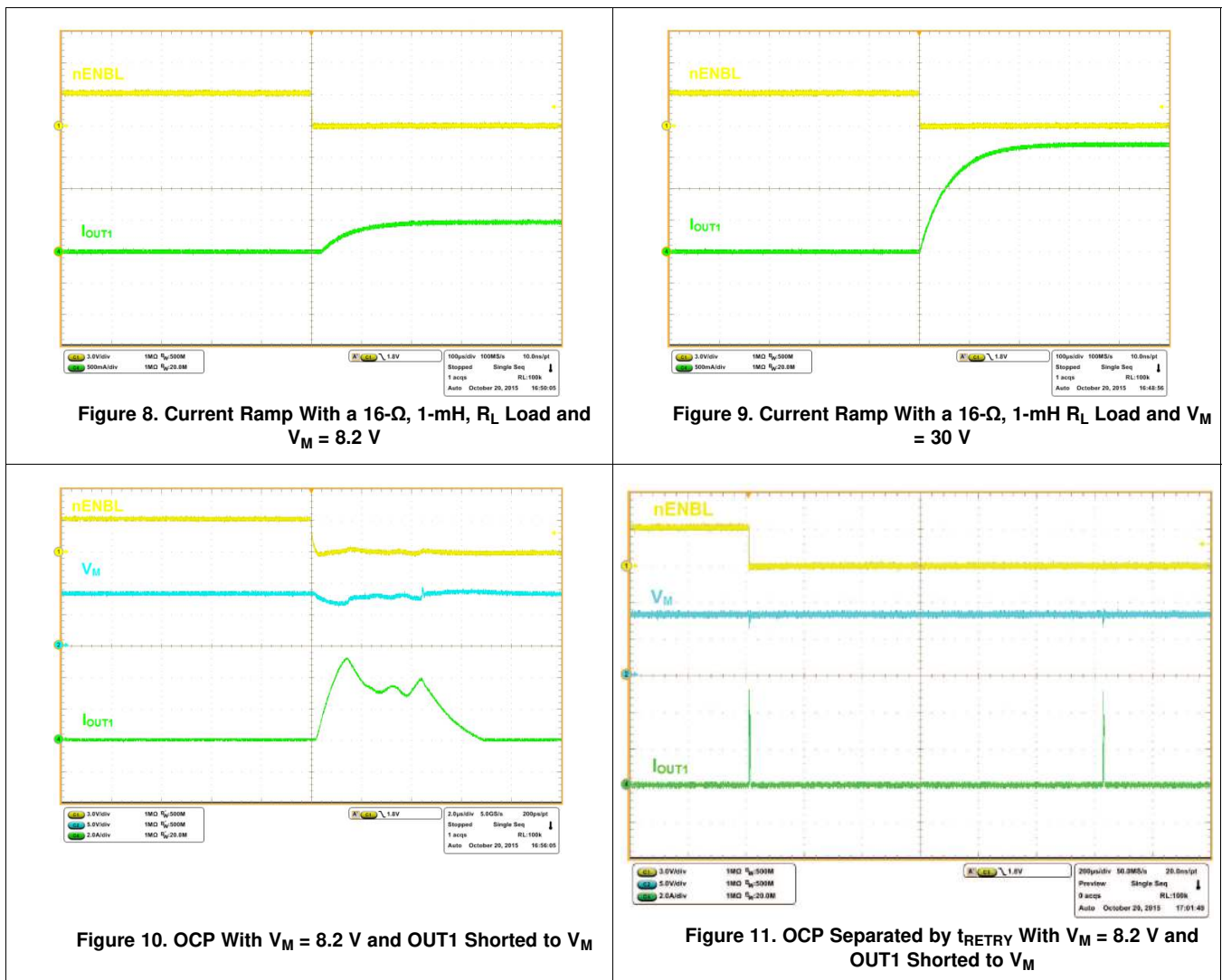
8.2.2.2 Drive Current

The current path starts from the supply V_M, moves through the inductive winding load and low-side sinking NMOS power FET. Power dissipation losses in one sink NMOS power FET are shown in Equation 1.

$$P = I^2 \times R_{DS\,(on)} \tag{1}$$

The DRV8804 has been measured to be capable of 1.5-A Single Channel or 800-mA Four Channels with the DW package and 2-A Single Channel or 1-A Four Channels with the PWP package at 25°C on standard FR-4 PCBs. The maximum RMS current will vary based on PCB design and the ambient temperature..

8.2.3 Application Curves

Figure 8. Current Ramp With a 16-Ω, 1-mH, R_L Load and V_M = 8.2 V

Figure 9. Current Ramp With a 16-Ω, 1-mH R_L Load and V_M = 30 V

Figure 10. OCP With V_M = 8.2 V and OUT1 Shorted to V_M

Figure 11. OCP Separated by t_{RETRY} With V_M = 8.2 V and OUT1 Shorted to V_M

Product Folder Links: *DRV8804*

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:
- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The type of motor used (Brushed DC, Brushless DC, Stepper).

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.
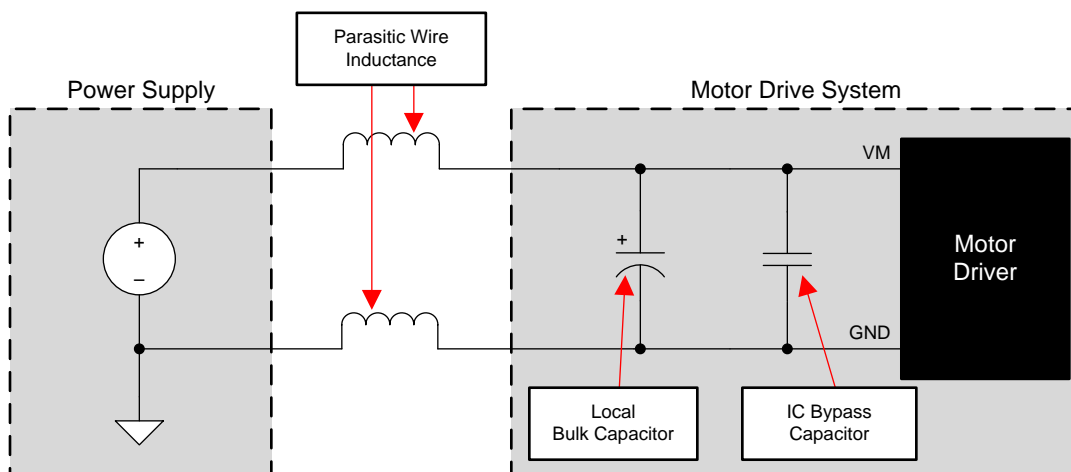

Figure 12. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

- Small-value capacitors should be ceramic, and placed closely to device pins.
- The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.
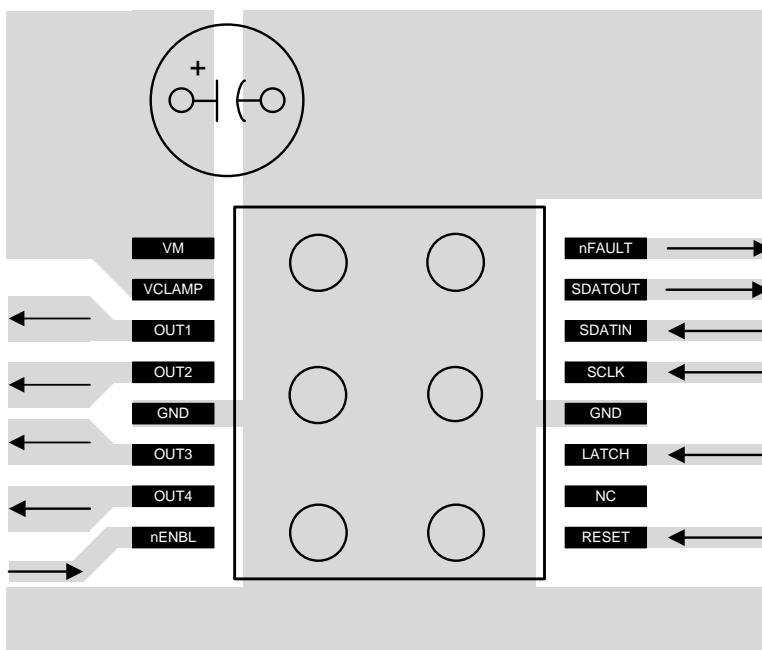
10.2 Layout Example

Figure 13. Layout Recommendation

10.3 Thermal Considerations

The DRV8804 has thermal shutdown (TSD) as described in *Thermal Shutdown (TSD)*. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

Power dissipation in the DRV8804 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation of each FET when running a static load can be roughly estimated by Equation 2.

$$P = R_{DS(ON)} \bullet (I_{OUT})^2$$

where

- P is the power dissipation of one FET
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is equal to the average current drawn by the load   (2)

Product Folder Links: *DRV8804*

Thermal Considerations (continued)

Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also must be taken into consideration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.3.2 Heatsinking

The DRV8804DW package uses a standard SOIC outline, but has the center pins internally fused to the die pad to more efficiently remove heat from the device. The two center leads on each side of the package should be connected together to as large a copper area on the PCB as is possible to remove heat from the device. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

The DRV8804PWP package uses an HTSSOP package with an exposed PowerPAD™. The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see TI Application Report, *PowerPAD Thermally Enhanced Package* (SLMA002), and TI Application Brief, *PowerPAD Made Easy* (SLMA004), available at www.ti.com.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:
- *PowerPAD Thermally Enhanced Package*, SLMA002
- *PowerPAD Made Easy*, SLMA004

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8804DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8804DW	Samples
DRV8804DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8804DW	Samples
DRV8804PWP	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8804	Samples
DRV8804PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8804	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8804DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
DRV8804PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8804DWR	SOIC	DW	20	2000	367.0	367.0	45.0
DRV8804PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PACKAGE MATERIALS INFORMATION

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8804DW	DW	SOIC	20	25	507	12.83	5080	6.6
DRV8804PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5
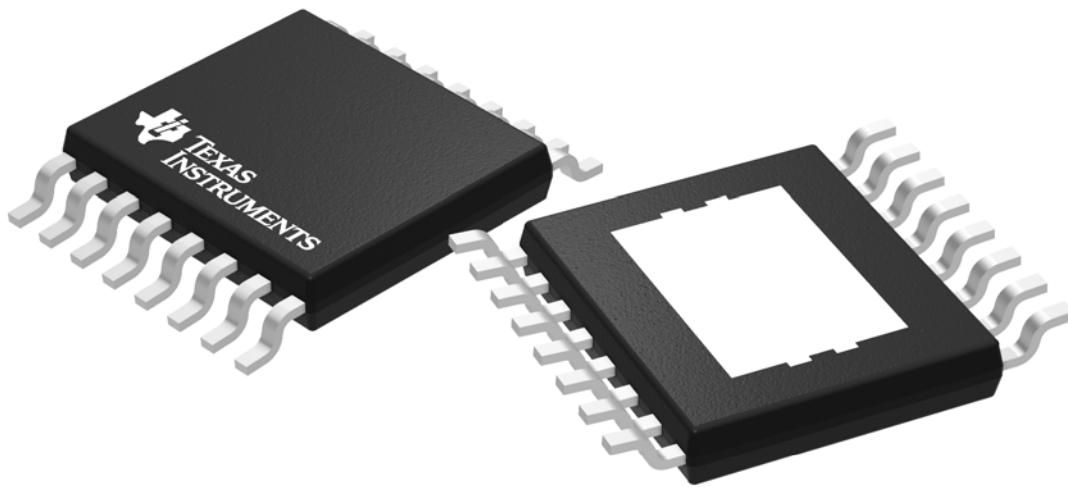
Images above are just a representation of the package family, actual package may vary.
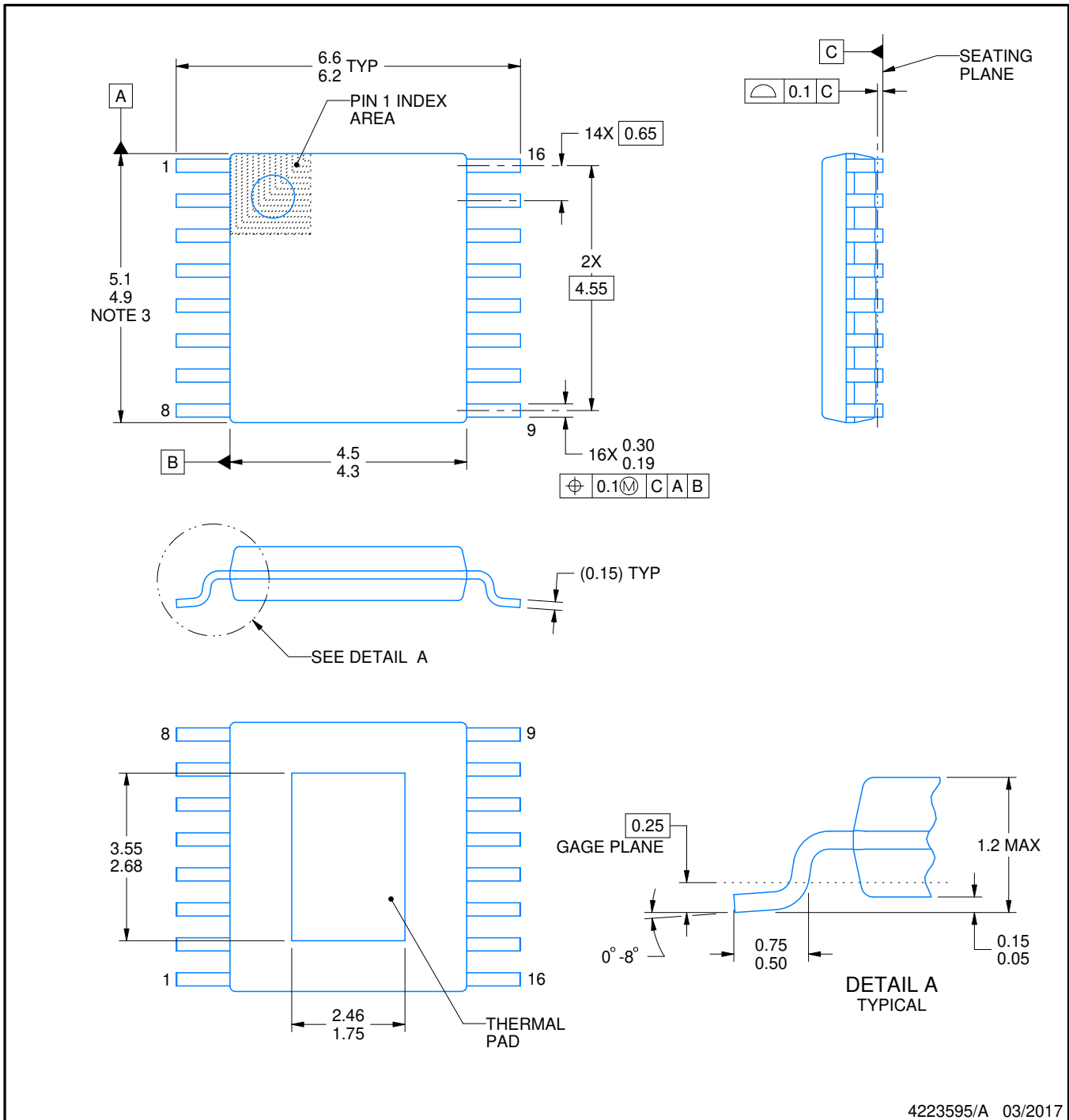Refer to the product data sheet for package details.

TEXAS INSTRUMENTS

6.6 TYP
6.2

A

PIN 1 INDEX
AREA

14X 0.65

16

C

SEATING
PLANE

0.1 C

1

2X

4.55

5.1
4.9
NOTE 3

8

9

B

4.5
4.3

16X 0.30
0.19

⊕ 0.1 Ⓜ C A B

SEE DETAIL A

(0.15) TYP

8

9

0.25

GAGE PLANE

1.2 MAX

3.55
2.68

0°-8°

0.75
0.50

0.15
0.05

1

16

DETAIL A
TYPICAL

2.46
1.75

THERMAL
PAD

4223595/A   03/2017

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
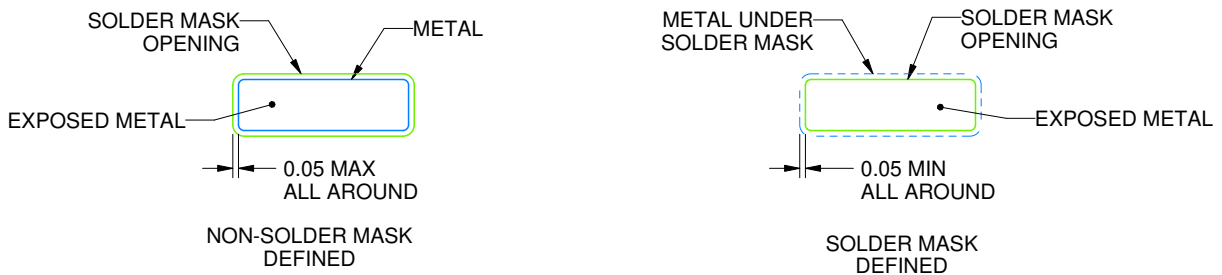4. Reference JEDEC registration MO-153.

TEXAS INSTRUMENTS
www.ti.com

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height
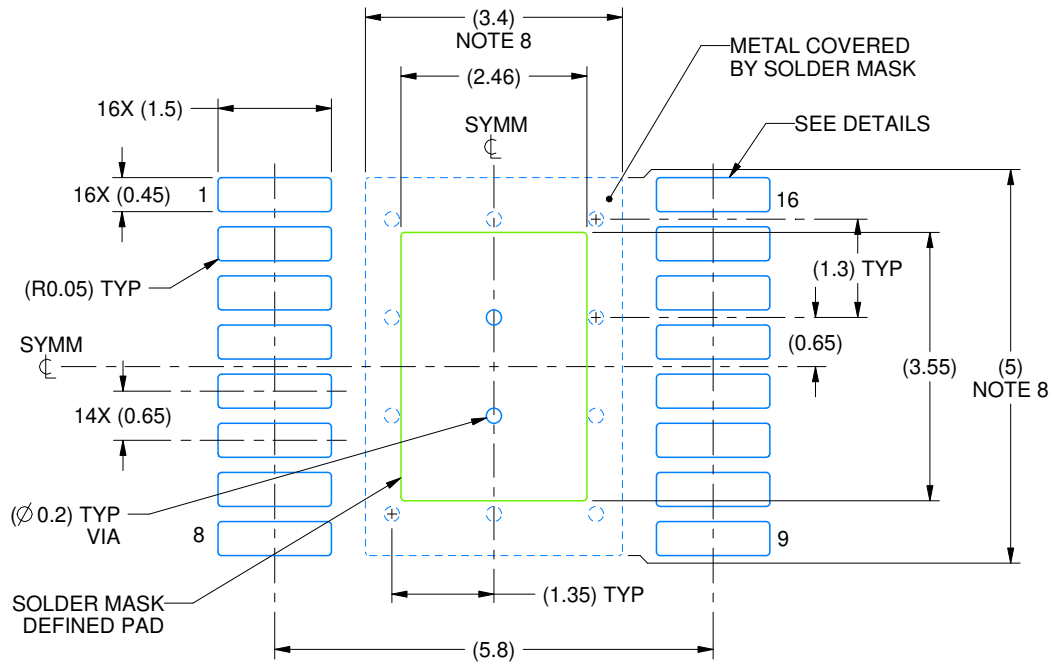
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

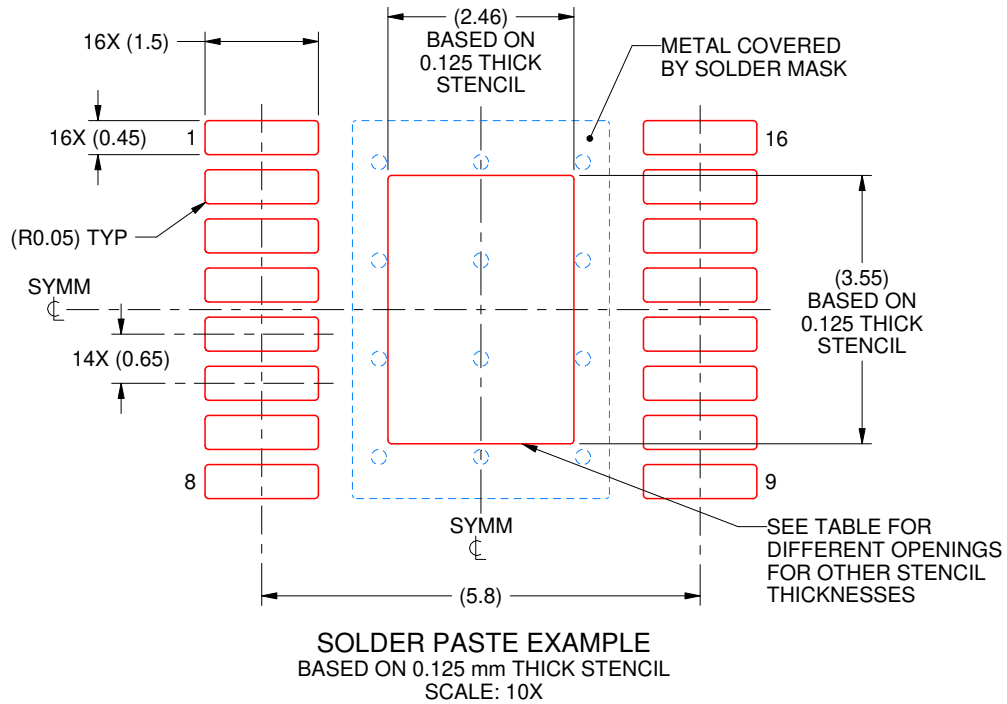SOLDER MASK DETAILS

4223595/A   03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

16X (1.5)

16X (0.45)   1

(R0.05) TYP

SYMM ₵

14X (0.65)

8

(2.46)
BASED ON
0.125 THICK
STENCIL

METAL COVERED
BY SOLDER MASK

16

(3.55)
BASED ON
0.125 THICK
STENCIL

9

SYMM ₵

SEE TABLE FOR
DIFFERENT OPENINGS
FOR OTHER STENCIL
THICKNESSES

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

4223595/A   03/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
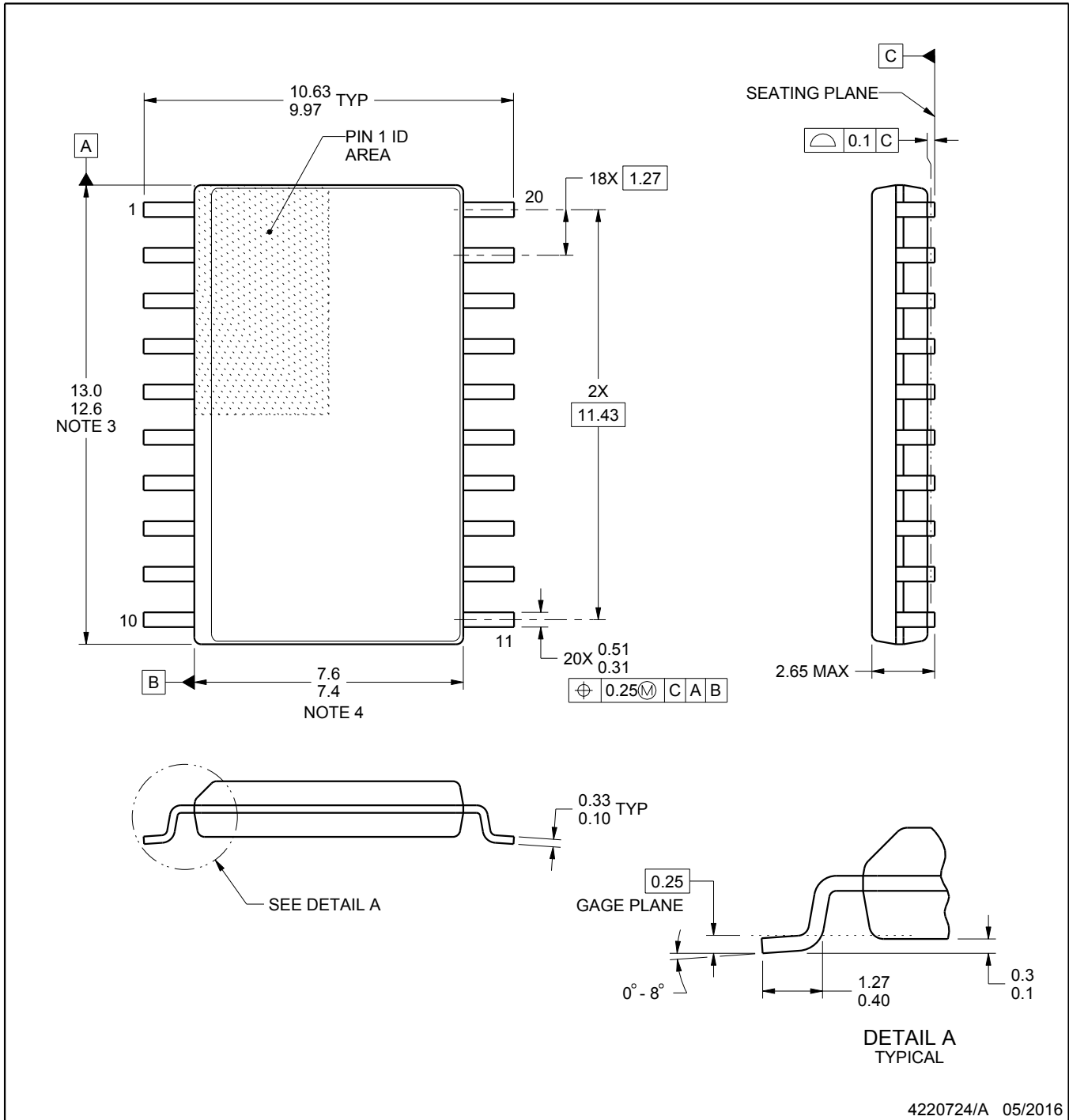11. Board assembly site may have different recommendations for stencil design.

DW0020A

SOIC - 2.65 mm max height

SEATING PLANE

$\boxed{C}$

$\boxed{\square \quad 0.1 \quad C}$

10.63 / 9.97 TYP

A

PIN 1 ID AREA

20

18X $\boxed{1.27}$

1

13.0 / 12.6 NOTE 3

2X $\boxed{11.43}$

10

11

2.65 MAX

B

7.6 / 7.4 NOTE 4

20X 0.51 / 0.31

$\boxed{\oplus \quad 0.25 \ⓂM \quad C \quad A \quad B}$

SEE DETAIL A

0.33 / 0.10 TYP

$\boxed{0.25}$

GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1
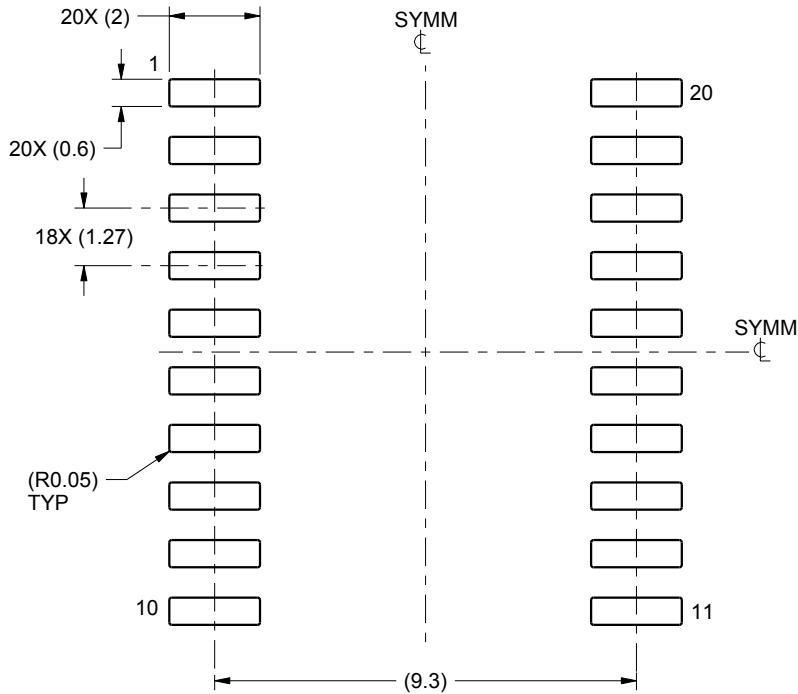
DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
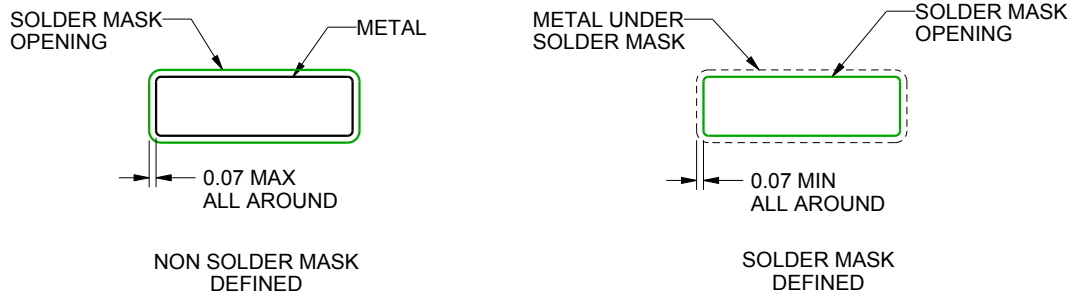5. Reference JEDEC registration MS-013.

TEXAS
INSTRUMENTS
www.ti.com

20X (2)

SYMM

1

20X (0.6)

20

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
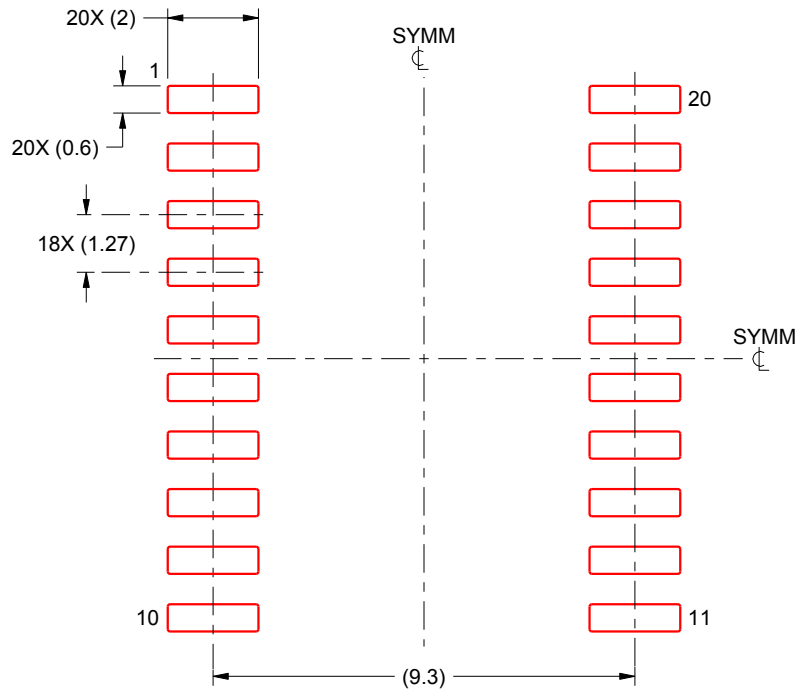
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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