

PSMN2R2-25YLC

N-channel 25 V 2.4 m Ω logic level MOSFET in LFPAK using NextPower technology

Rev. 1 — 2 May 2011

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD and QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching

- Power OR-ing
- Server power supplies
- Sync rectifier

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	-	25	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	[1] -	-	100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	106	W
Tj	junction temperature		-55	-	175	°C
Static char	racteristics					
R _{DSon}	drain-source on-state	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 ^{\circ}\text{C}; \text{see } \frac{\text{Figure } 12}{\text{Figure } 12}$	-	2.6	3.15	mΩ
	resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_i = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 12}{\text{ constant}}$	-	2	2.4	mΩ



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Dynamic ch	aracteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 12 \text{ V}; \text{ see } \frac{\text{Figure 14}}{\text{Figure 15}};$	-	5.2	-	nC
Q _{G(tot)}	total gate charge	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A};$ $V_{DS} = 12 \text{ V}; \text{ see } \frac{\text{Figure 15}}{\text{Figure 14}};$	-	18	-	nC

[1] Continuous current is limited by package

2. Pinning information

Table 2. Pinning information

		•		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source	mb	D
3	S	source		
4	G	gate	[Q	
mb	D	mounting base; connected to drain	1 2 3 4	mbb076 S
			SOT669 (LFPAK;	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R2-25YLC	LFPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PSMN2R2-25YLC	2C225L

[1] % = placeholder for manufacturing site code.

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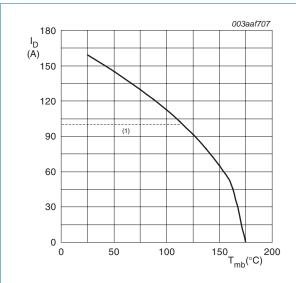
5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	25	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; see <u>Figure 1</u>	<u>[1]</u> _	100	Α
		$V_{GS} = 10 \text{ V}; T_{mb} = 100 ^{\circ}\text{C}; \text{see } \frac{\text{Figure 1}}{}$	<u>[1]</u> -	100	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 ^{\circ}C$; see Figure 4	-	636	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	106	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	430	-	V
Source-drai	n diode				
Is	source current	T _{mb} = 25 °C	-	96	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	636	Α
Avalanche r	uggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 25 V; unclamped; R_{GS} = 50 Ω; see Figure 3	-	60	mJ

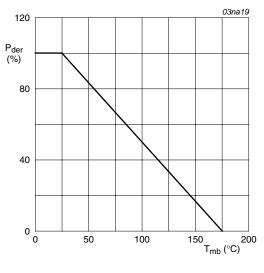
^[1] Continuous current is limited by package.



 $V_{GS} \ge 10V$; (1) Capped at 100A due to package

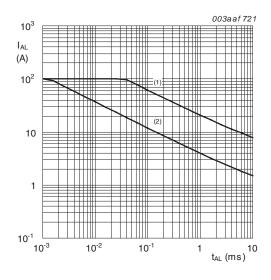
g 1. Continuous drain current as a function of

mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

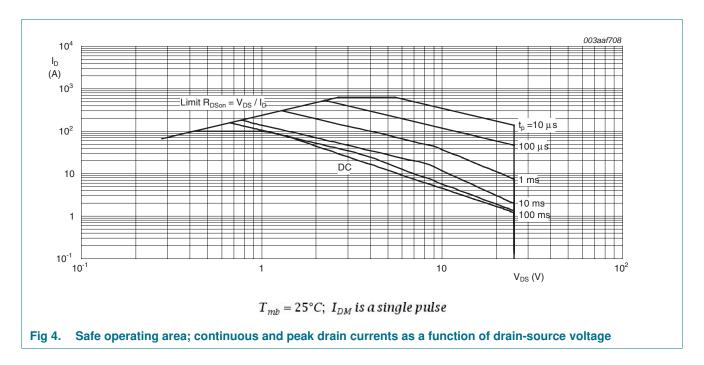
Fig 2. Normalized total power dissipation as a function of mounting base temperature



(1) $T_{j \text{ (init)}} = 25^{\circ}C$; (2) $T_{j \text{ (init)}} = 100^{\circ}C$

Single pulse avalanche rating; avalanche current as a function of avalanche time

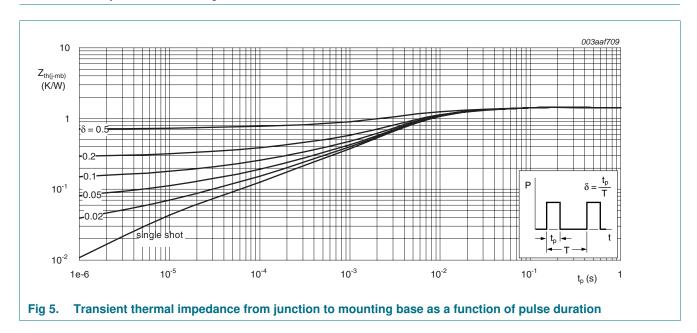
Fig 3.



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	1.25	1.42	K/W



7. Characteristics

Table 7. Characteristics

Table 7.	Characteristics	Conditions	B.41	Trees	Marr	11!
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	racteristics	L 050A. V 0.1/5 T 05.00	05		_	V
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	25	-		-
		$I_D = 250 \mu\text{A}; V_{GS} = 0 V; T_j = -55 ^{\circ}\text{C}$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see <u>Figure 10</u> ; see <u>Figure 11</u>	1.05	1.54	1.95	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ °C}$	0.5	-	-	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ °C}$	-	-	2.25	V
I_{DSS}	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	100	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 12	-	2.6	3.15	mΩ
	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ °C};$ see Figure 13; see Figure 12	-	-	5.05	mΩ	
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 12	-	2	2.4	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C; see Figure 13; see Figure 12	-	-	3.85	mΩ
R _G	gate resistance	f = 1 MHz	-	0.9	1.8	Ω
	characteristics					
Q _{G(tot)} total gate charge	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 12 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 14; see Figure 15	-	39	-	nC
	I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see <u>Figure 15</u> ; see <u>Figure 14</u>	-	18	-	nC	
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	38	-	nC
Q _{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	6.3	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	see Figure 14; see Figure 15	-	4.1	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	2.2	-	nC
Q_{GD}	gate-drain charge		-	5.2	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 12 V; see <u>Figure 14</u> ; see Figure 15	-	2.7	-	V
C _{iss}	input capacitance	V _{DS} = 12 V; V _{GS} = 0 V; f = 1 MHz;	-	2542	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	617	-	pF
C _{rss}	reverse transfer capacitance		-	216	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 12 \text{ V}; R_L = 0.5 \Omega; V_{GS} = 4.5 \text{ V};$	-	24	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega$	_	34	_	ns
t _{d(off)}	turn-off delay time			36	_	ns
t _f	fall time			16	-	ns
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Table 7. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Q _{oss}	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 12 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	16.7	-	nC
Source-drain	diode					
V _{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 17</u>	-	8.0	1.1	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	35	-	ns
Q _r	recovered charge	V _{DS} = 12 V	-	31	-	nC
t _a	reverse recovery rise time	$V_{GS} = 0 \text{ V}; I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{DS} = 12 \text{ V}; see Figure 18$	-	21	-	ns
t _b	reverse recovery fall time		-	14	-	ns

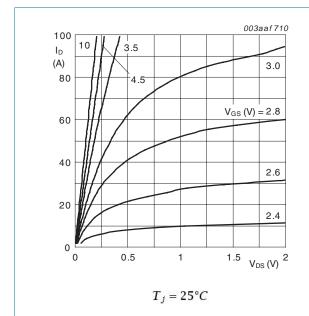


Fig 6. Output characteristics; drain current as a function of drain-source voltage

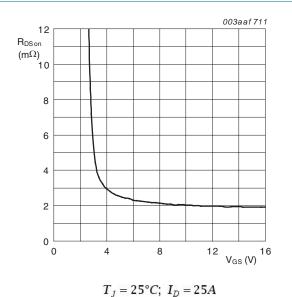


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

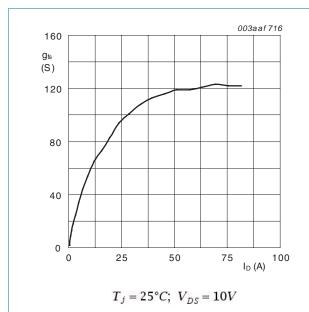


Fig 8. Forward transconductance as a function of drain current; typical values

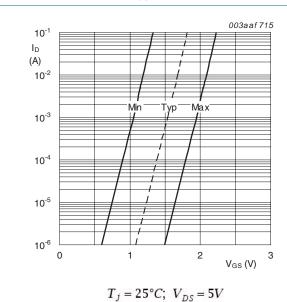


Fig 10. Sub-threshold drain current as a function of gate-source voltage

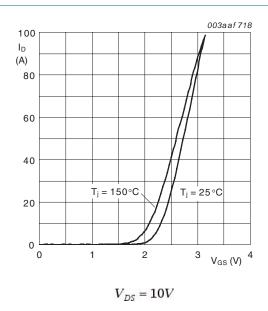


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

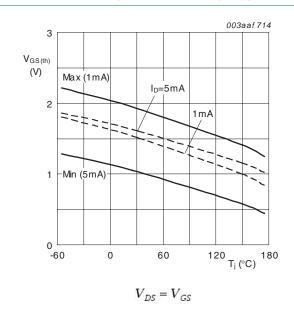


Fig 11. Gate-source threshold voltage as a function of junction temperature

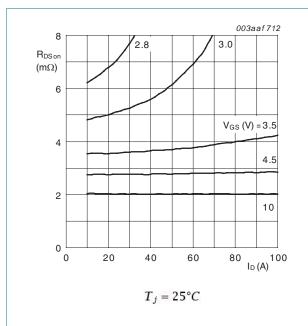


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

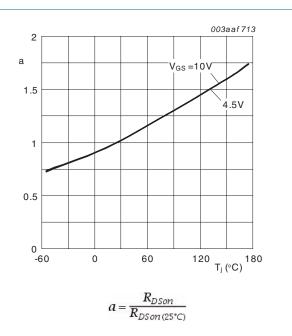


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

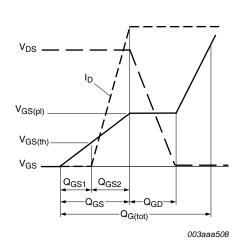
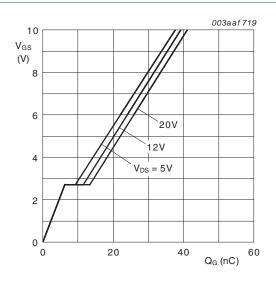


Fig 14. Gate charge waveform definitions



$$T_j = 25^{\circ}C; \ I_D = 25A$$

Fig 15. Gate-source voltage as a function of gate charge; typical values

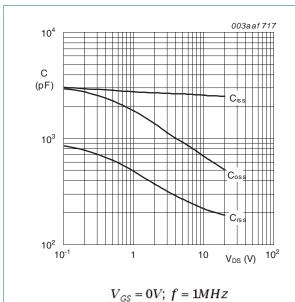


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

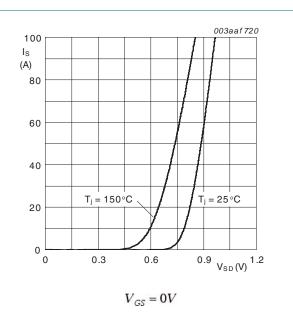


Fig 17. Source current as a function of source-drain voltage; typical values

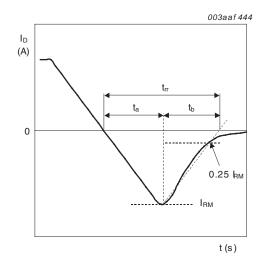


Fig 18. Reverse recovery timing definition

8. Package outline

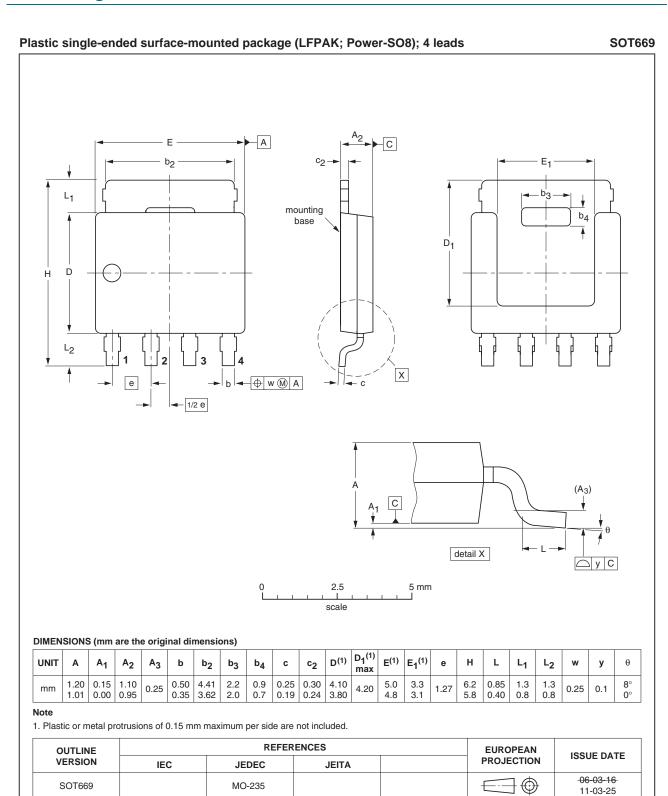


Fig 19. Package outline SOT669 (LFPAK; Power-SO8)

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9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN2R2-25YLC v.1	20110502	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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PSMN2R2-25YLC

N-channel 25 V 2.4 m Ω logic level MOSFET in LFPAK using NextPower

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