

FDBL9403L-F085

Single N-Channel Power MOSFET

40 V, 240 A, 0.72 mΩ

Features

- Small Footprint (TOLL) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	40	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	240	A
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D	357.1	W
		$T_C = 100^\circ\text{C}$		178.6	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	53.3	A
		$T_C = 100^\circ\text{C}$		37.7	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_C = 25^\circ\text{C}$	P_D	3.5	W
		$T_C = 100^\circ\text{C}$		1.7	
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	2113	A	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	100	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 79 \text{ A}, L = 0.2 \text{ mH}$)		E_{AS}	624	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

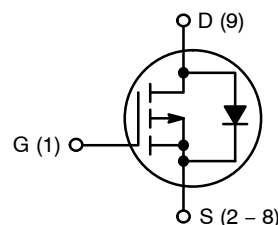
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Current is limited by bondwire configuration.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
40 V	0.72 mΩ @ 10 V	80 A
	0.98 mΩ @ 4.5 V	

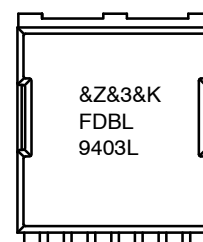


N-CHANNEL MOSFET



H-PSOF8L
CASE 100CU

MARKING DIAGRAM



&Z = Assembly Plant Code
 &3 = Numeric Date Code
 &K = Lot Code
 FDBL9403L = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

FDBL9403L–F085

Table 1. THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	0.42	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 4)	43	

4. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.

Table 2. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	40	–	–	V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient		–	22.5	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$ $V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 175^\circ\text{C}$	–	–	1	μA mA
I_{GSS}	Zero Gate Voltage Drain Current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	–	–	±100	nA

ON CHARACTERISTICS (Note 5)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1	1.75	3	V
$V_{GS(th)}/T_J$	Threshold Temperature Coefficient		–	–5.6	–	mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 80 \text{ A}$	–	0.59	0.72	mΩ
		$V_{GS} = 4.5 \text{ V}, I_D = 40 \text{ A}$	–	0.76	0.98	

CHARGES, CAPACITANCES & GATE RESISTANCE

C_{iss}	Input Capacitance	$V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}, V_{DS} = 20 \text{ V}$	–	14100	–	pF
C_{oss}	Output Capacitance		–	4070	–	
C_{rss}	Reverse Transfer Capacitance		–	300	–	
R_g	Gate Resistance	$V_{GS} = 0.5 \text{ V}, f = 1 \text{ MHz}$	–	3.3	–	Ω
$Q_{g(tot)}$	Total Gate Charge	$V_{GS} = 4.5 \text{ V}, V_{DS} = 32 \text{ V}, I_D = 80 \text{ A}$	–	97	–	nC
		$V_{GS} = 10 \text{ V}, V_{DS} = 32 \text{ V}, I_D = 80 \text{ A}$	–	203	–	
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0 \text{ V to } 1 \text{ V}$	–	13	–	
Q_{gs}	Gate-to-Source Gate Charge	$V_{DD} = 32 \text{ V}, I_D = 80 \text{ A}$	–	40	–	
Q_{gd}	Gate-to-Drain “Miller” Charge		–	27	–	
V_{GP}	Plateau Voltage		–	3	–	V

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20 \text{ V}, I_D = 80 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	–	21	–	ns
t_r	Turn-On Rise Time		–	42	–	
$t_{d(off)}$	Turn-Off Delay Time		–	288	–	
t_f	Turn-Off Fall Time		–	101	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 80 \text{ A}, V_{GS} = 0 \text{ V}$	–	0.79	1.25	V
		$I_{SD} = 40 \text{ A}, V_{GS} = 0 \text{ V}$	–	0.75	1.2	
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, dI_{SD}/dt = 100 \text{ A}/\mu\text{s}, I_S = 80 \text{ A}$	–	96	–	ns
t_a	Charge Time		–	46	–	
t_b	Discharge Time		–	50	–	
Q_{rr}	Reverse Recovery Charge		–	130	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

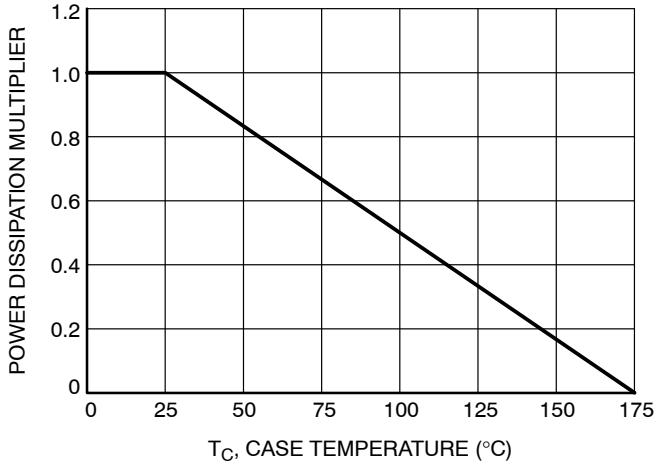


Figure 1. Normalized Power Dissipation vs. Case Temperature

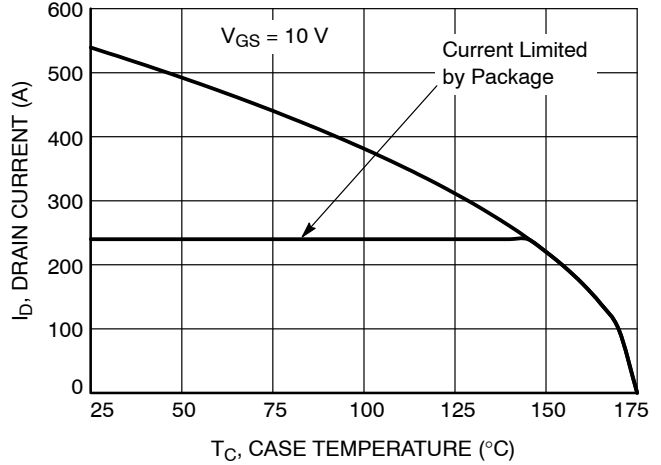


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

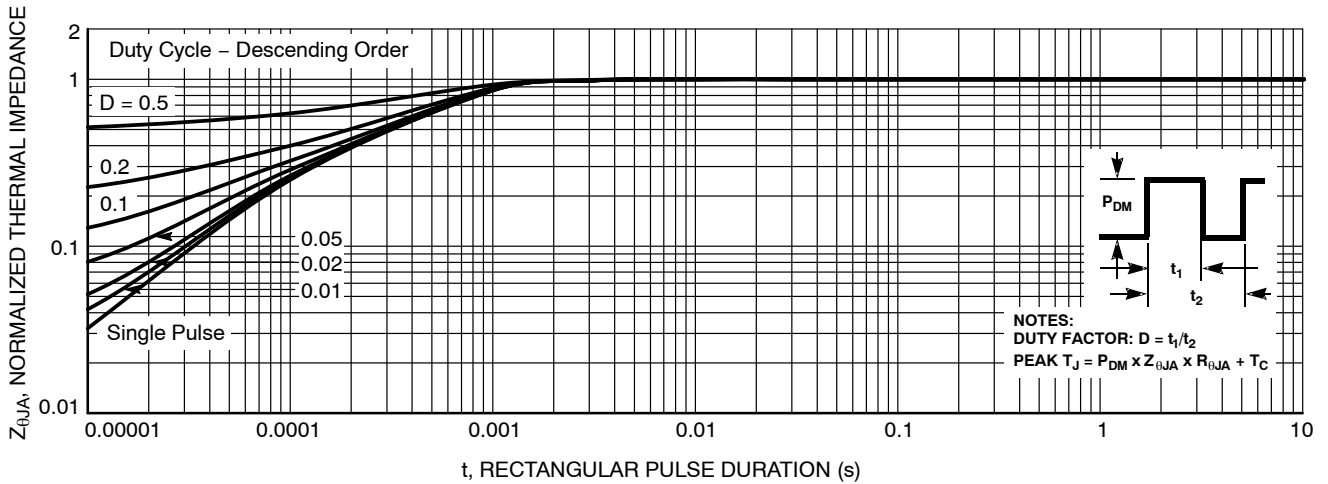


Figure 3. Normalized Maximum Transient Thermal Impedance

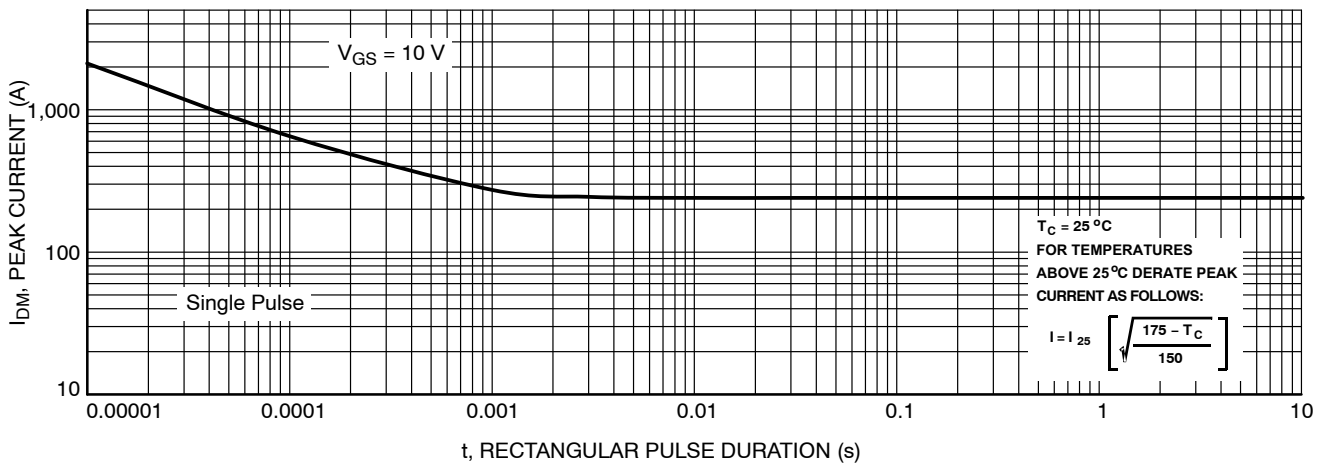


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

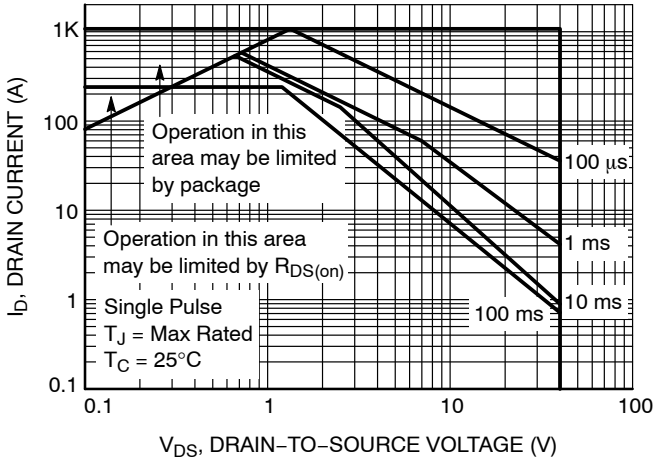


Figure 5. Forward Bias Safe Operating Area

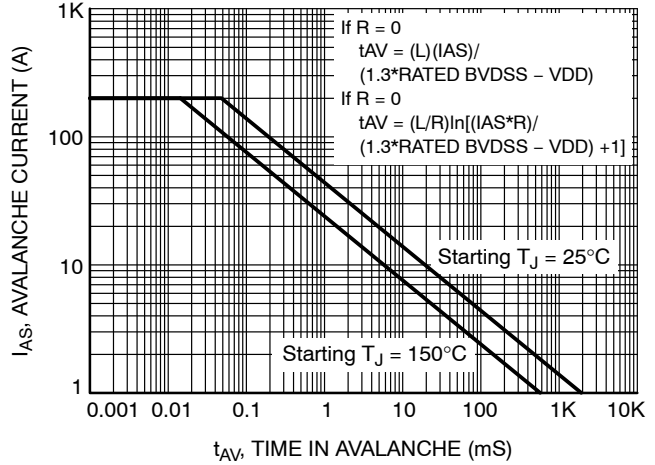


Figure 6. Unclamped Inductive Switching Capability

Note: Refer to ON Semiconductor Application Notes AN7514 and AN7515

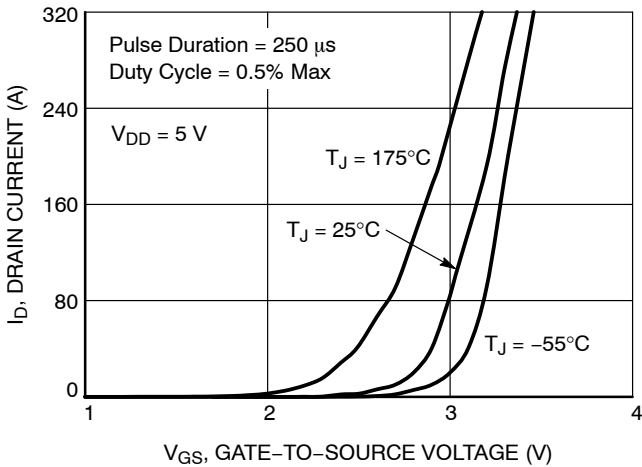


Figure 7. Transfer Characteristics

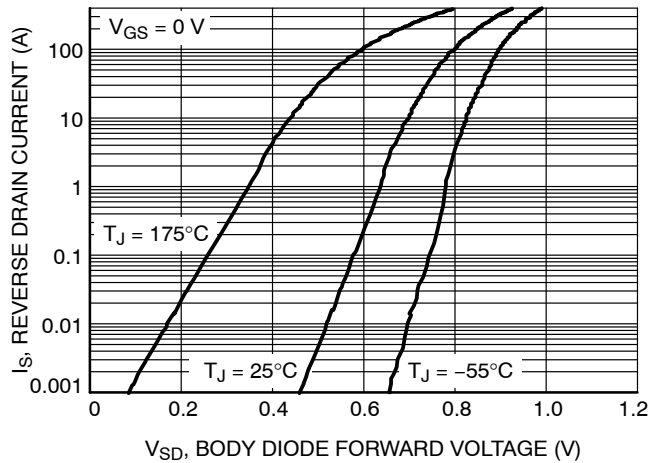


Figure 8. Forward Diode Characteristics

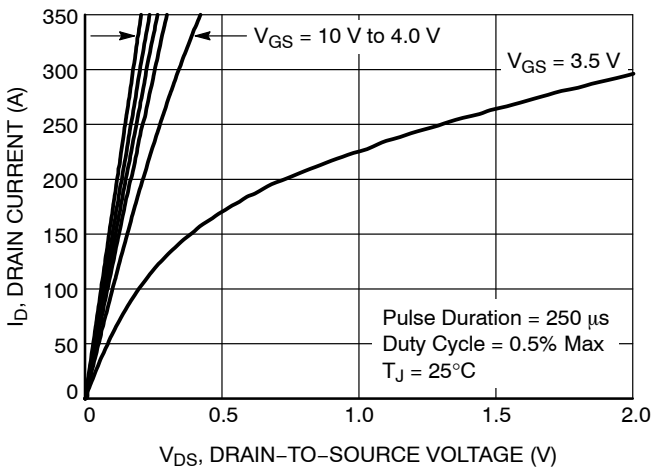


Figure 9. Saturation Characteristics

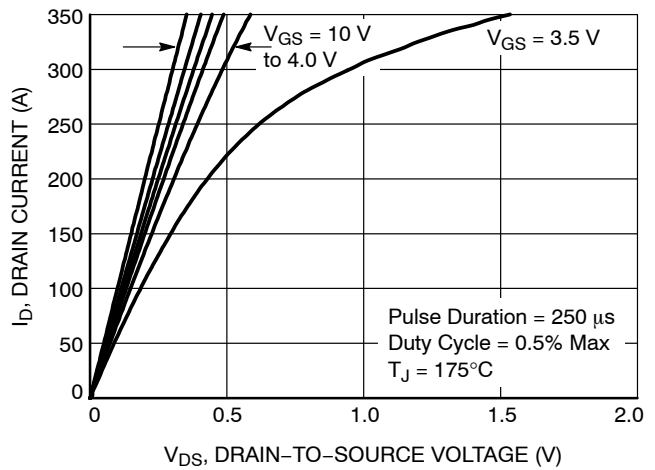


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

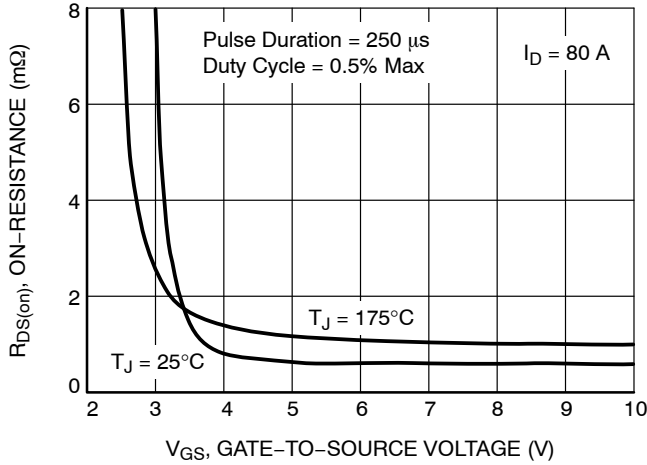


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

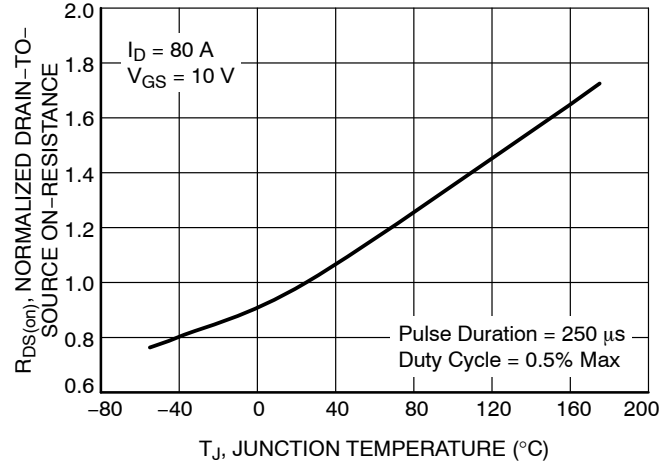


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

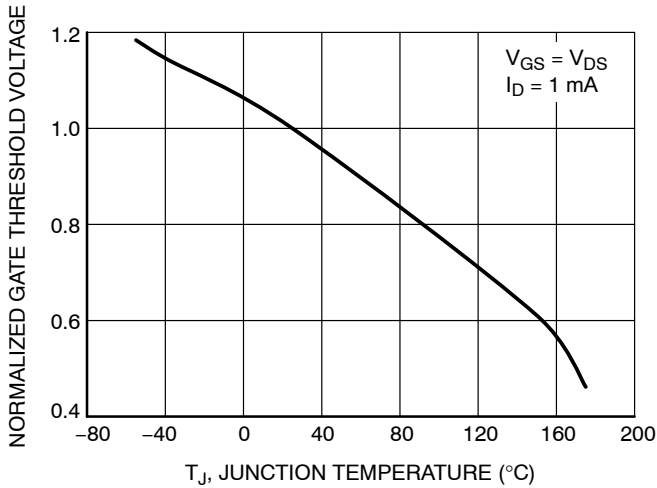


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

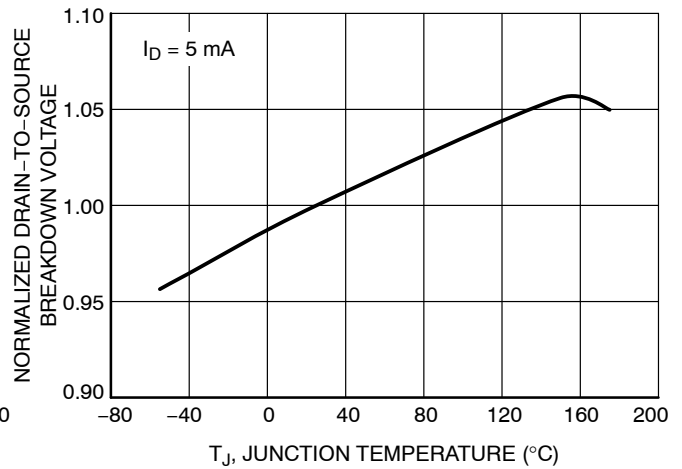


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

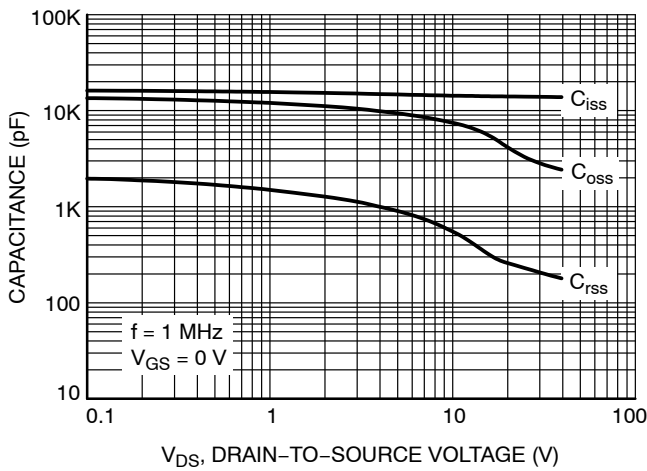


Figure 15. Capacitance vs. Drain-to-Source Voltage

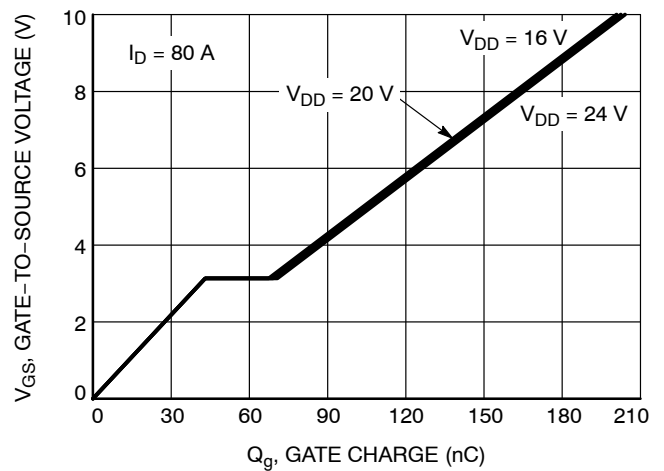


Figure 16. Gate Charge vs. Gate-to-Source Voltage

FDBL9403L-F085

PACKAGE MARKING AND ORDERING INFORMATION

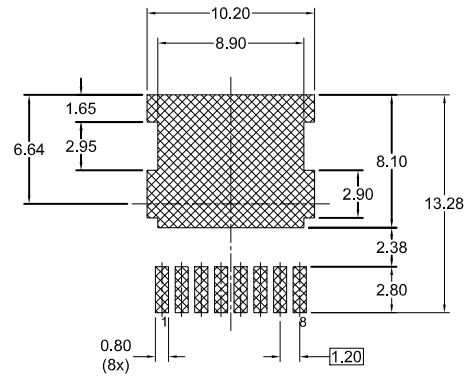
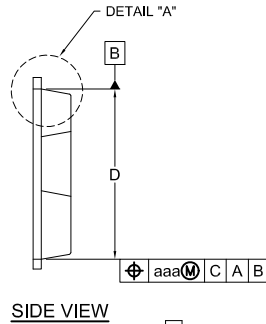
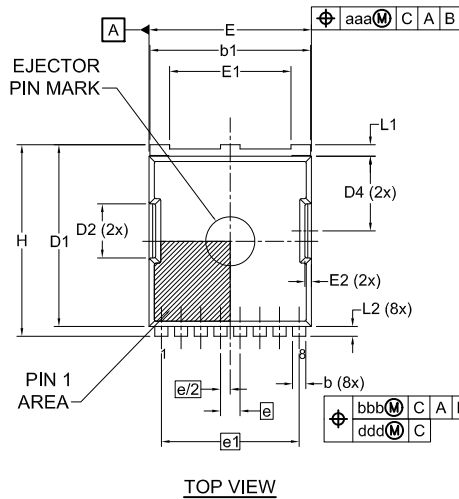
Device	Marking	Package	Reel Size	Tape Width	Quantity
FDBL9403L-F085	FDBL9403L	H-PSOF8L (Pb-Free / Halogen Free)	13"	24 mm	2000 Units

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



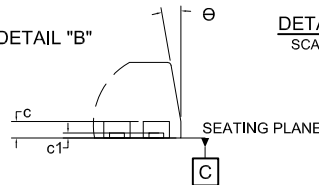
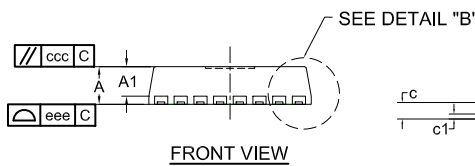
H-PSOF8L 11.68x9.80
CASE 100CU
ISSUE C

DATE 22 MAY 2023



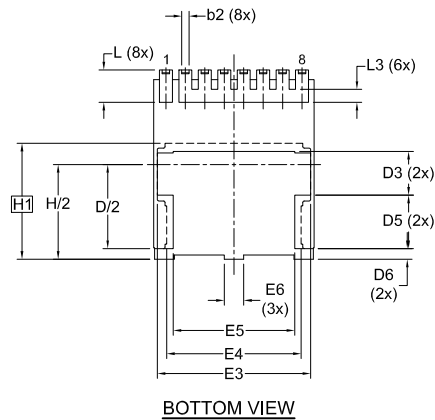
LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

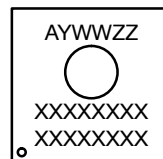


NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	—	—
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
theta	0°	—	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON13813G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	H-PSOF8L 11.68x9.80	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales