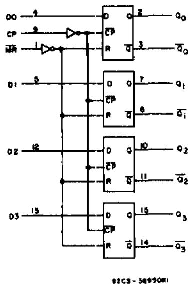
File Number **1474**

CD54/74HC175
CD54/74HCT175

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad D Flip-Flop with Reset

Type Features:

- *Common Clock and Asynchronous Reset on four D-Type Flip-Flops*
- *Positive-edge pulse triggering*
- *Complementary Outputs*
- *Buffered Inputs*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA CD54/74HC175 and the CD54/74HCT175 are high speed Quad D-Type Flip-Flops with individual D-inputs and Q, $\overline{Q}$ complementary outputs. The devices are fabricated using silicon gate CMOS technology. They have the low power consumption advantage of standard CMOS ICs and the ability to drive 10 LSTTL devices.

Information at the D input is transferred to the Q and $\overline{Q}$ outputs on the positive-going edge of the clock pulse. All four Flip-Flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock. All four Q outputs are reset to a logic 0 and all four $\overline{Q}$ outputs to a logic 1.

The CD54HC175 and CD54HCT175 are supplied in 16-lead dual-in-line ceramic packages (F suffix) and the CD74HC175 and CD74HCT175 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

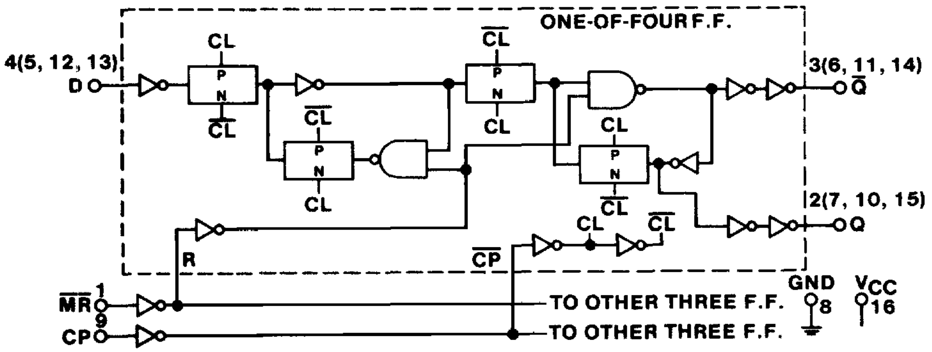


Fig. 1 - Logic block diagram.

92CM-38949R1

CD54/74HC175
CD54/74HCT175

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < V_o < V_{CC} + 0.5V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal conditions should be selected so that operation is always within the following ranges:

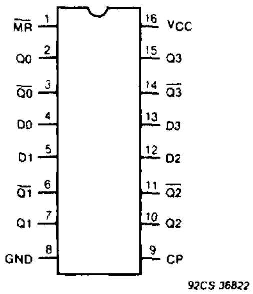
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For TA = Full Package Temperature Range) VCC:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage VIN, VOUT	0	Vcc	V
Operating Temperature TA:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, tr, tf			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Qn	$\overline{Qn}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Qo	$\overline{Qo}$

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↑ = Transition from Low to High Level
Qo, $\overline{Qo}$ = Levels Before the Indicated Steady-State Input Conditions were Established



TERMINAL ASSIGNMENT

CD54/74HC175
CD54/74HCT175

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC175/CD54HC175										CD74HCT175/CD54HCT175									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{MR}$	1.0
D	0.15
CP	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC175
CD54/74HCT175

PRE-REQUISITE FOR SWITCHING FUNCTION 54/74HC SERIES AND 54/74HCT SERIES

CHARACTERISTIC	TEST CONDITION	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
	Vcc V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Pulse	2	80	—	—	—	100	—	—	—	120	—	—	—	
Width t_W	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
Fig. 3	6	14	—	—	—	17	—	—	—	20	—	—	—	
	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{MR}$ Pulse Width t_W	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
Fig. 4	6	14	—	—	—	17	—	—	—	20	—	—	—	
Setup Time Data	2	80	—	—	—	100	—	—	—	120	—	—	—	
to Clock t_{SU}	4.5	16	—	20	—	20	—	25	—	24	—	30	—	ns
Fig. 5	6	14	—	—	—	17	—	—	—	20	—	—	—	
Hold Time Data	2	5	—	—	—	5	—	—	—	5	—	—	—	
to Clock t_H	4.5	5	—	5	—	5	—	5	—	5	—	5	—	ns
Fig. 5	6	5	—	—	—	5	—	—	—	5	—	—	—	
Removal Time	2	5	—	—	—	5	—	—	—	5	—	—	—	
$\overline{MR}$ to Clock t_{REM}	4.5	5	—	5	—	5	—	5	—	5	—	5	—	ns
Fig. 4	6	5	—	—	—	5	—	—	—	5	—	—	—	
	2	6	—	—	—	5	—	—	—	4	—	—	—	
Clock Frequency f_{max}	4.5	30	—	25	—	25	—	20	—	20	—	16	—	MHz
	6	35	—	—	—	29	—	—	—	23	—	—	—	

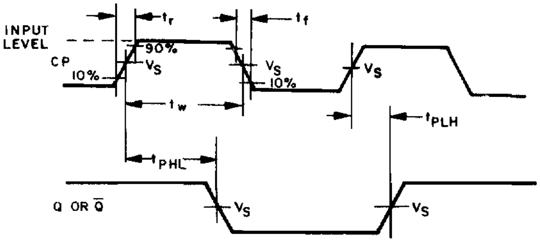
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	TEST CONDITION	LIMITS												UNITS
		25° C				-40° C to +85° C				-55° C to + 125° C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
	V_{CC} V	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
Clock to Q or $\overline{Q}$ t_{PHL}	4.5	—	35	—	33	—	44	—	41	—	53	—	50	ns
Fig. 3	6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
($\overline{MR}$) to Q or $\overline{Q}$ t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
Fig. 4	6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Time t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
Fig. 6	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	Typical HC	Typical HCT	Units
Propagation Delay- Clock to Q or $\overline{Q}$, Fig. 3	t_{PLH} t_{PHL}	15	14	13	ns
Propagation Delay $\overline{MR}$ to Q or $\overline{Q}$, Fig. 4	t_{PHL} t_{PLH}	15	14	17	ns
Power Dissipation Capacitance*	C_{PD}	—	65	67	pF

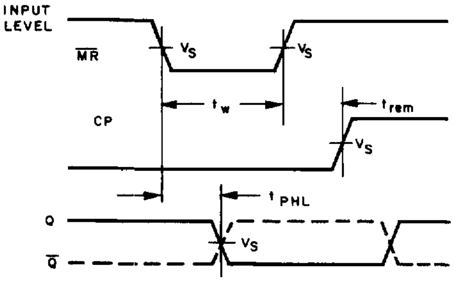
*C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2f_i + \Sigma C_LV_{CC}^2f_o$ where f_i = input frequency, f_o = output frequency,
C_L = output load capacitance, V_{CC} = supply voltage



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

92CS-36951

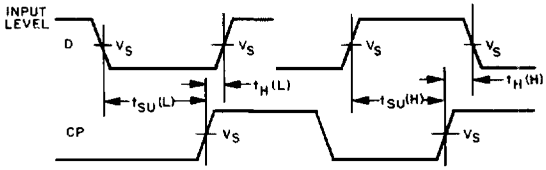
Fig. 3 - Propagation delay times and clock pulse width.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

92CS-36952

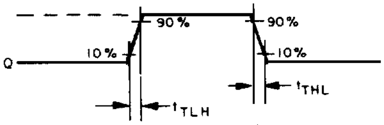
Fig. 4 - Pre-requisite and propagation delay times for master reset.



92CS-36954R1

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
V_S	50% V_{CC}	1.3 V

Fig. 5 - Pre-requisite for clock.



92CS-36953

Fig. 6 - Transition times.