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FAIRCHILD SEMICONDUCTOR®

May 2008

FDB3502

N-Channel Power Trench® MOSFET

75V, 14A, 47mΩ

Features

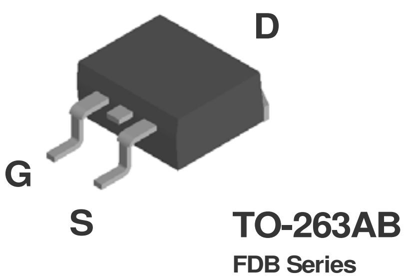
- Max $r_{DS(on)}$ = 47mΩ at V_{GS} = 10V, I_D = 6A
- 100% UIL Tested
- RoHS Compliant

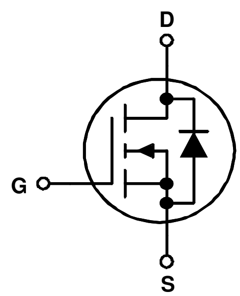
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- Synchronous rectifier





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	75	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) T_C = 25°C	14	A
	-Continuous (Silicon limited) T_C = 25°C	22	
	-Continuous T_A = 25°C (Note 1a)	6	
	-Pulsed	40	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	54	mJ
P_D	Power Dissipation T_C = 25°C	41	W
	Power Dissipation T_A = 25°C (Note 1a)	3.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB3502	FDB3502	TO-263AB	330 mm	24 mm	800 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	75			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		70		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0V, V_{DS} = 60V,			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2.5	3.8	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-10		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 6A		37	47	mΩ
		V_{GS} = 10V, I_D = 6A, T_J = 125°C		63	80	
g_{FS}	Forward Transconductance	V_{DD} = 10V, I_D = 6A		13		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 40V, V_{GS} = 0V, f = 1MHz		615	815	pF
C_{oss}	Output Capacitance			75	105	pF
C_{rss}	Reverse Transfer Capacitance			35	40	pF
R_g	Gate Resistance	f = 1MHz		1.5		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40V, I_D = 6A, V_{GS} = 10V, R_{GEN} = 6Ω		9	17	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			13	22	ns
t_f	Fall Time			3	10	ns
Q_g	Total Gate Charge at 10V	V_{DD} = 40V I_D = 6A		11	15	nC
Q_{gs}	Gate to Source Charge			4		nC
Q_{gd}	Gate to Drain "Miller" Charge			3		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 2.6A (Note 2)		0.78	1.2	V
		V_{GS} = 0V, I_S = 6A (Note 2)		0.83	1.3	
t_{rr}	Reverse Recovery Time	I_F = 6A, di/dt = 100A/μs		25	41	ns
Q_{rr}	Reverse Recovery Charge			17	32	nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

a. 40°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 62.5°C/W when mounted on a minimum pad.

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3: Starting T_J = 25°C, L = 3mH, I_{AS} = 6A, V_{DD} = 75V, V_{GS} = 10V.

Typical Characteristics T_J = 25°C unless otherwise noted

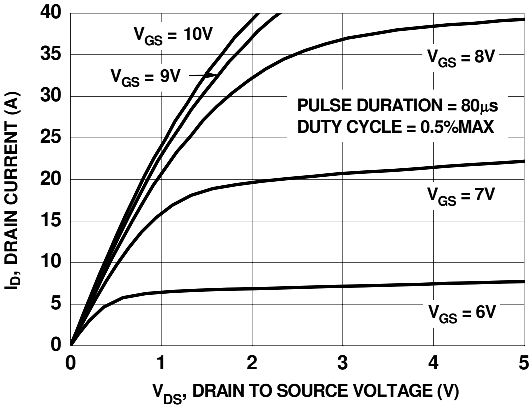


Figure 1. On-Region Characteristics

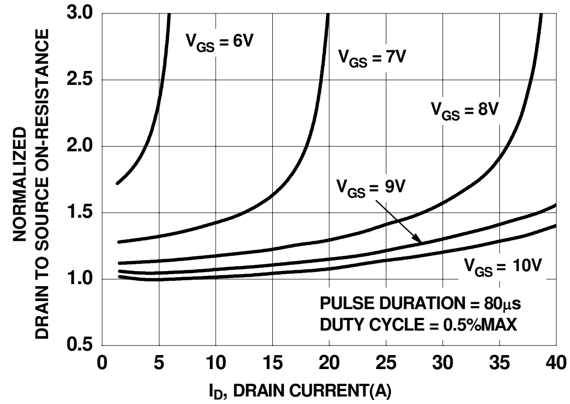


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

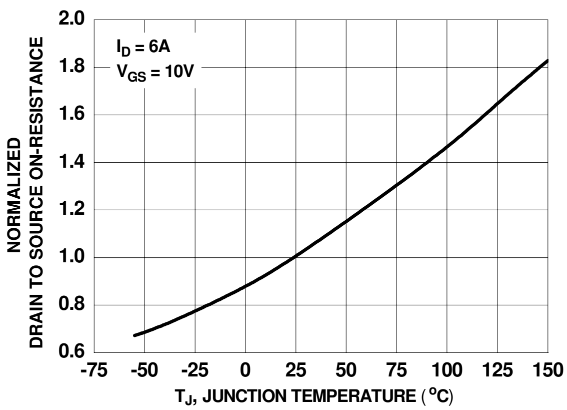


Figure 3. Normalized On- Resistance vs Junction Temperature

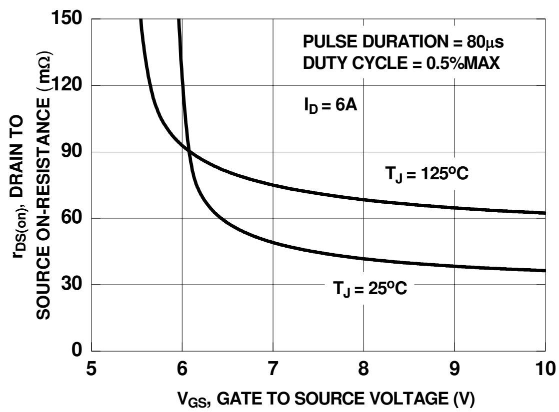


Figure 4. On-Resistance vs Gate to Source Voltage

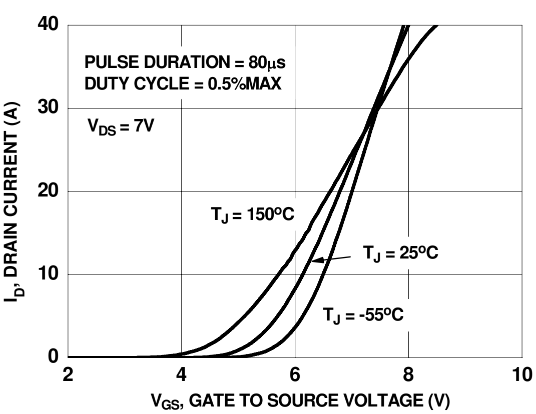


Figure 5. Transfer Characteristics

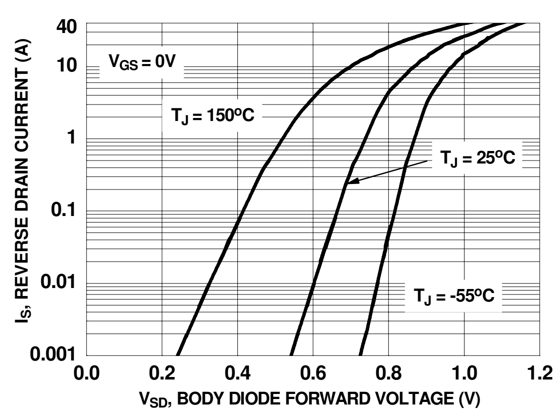


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

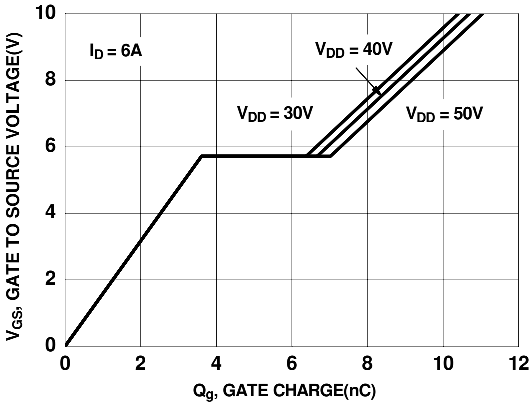


Figure 7. Gate Charge Characteristics

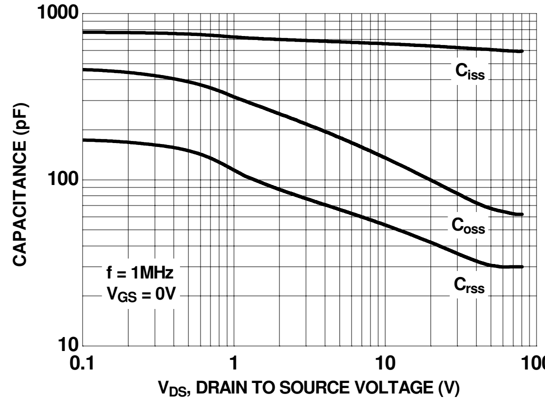


Figure 8. Capacitance vs Drain to Source Voltage

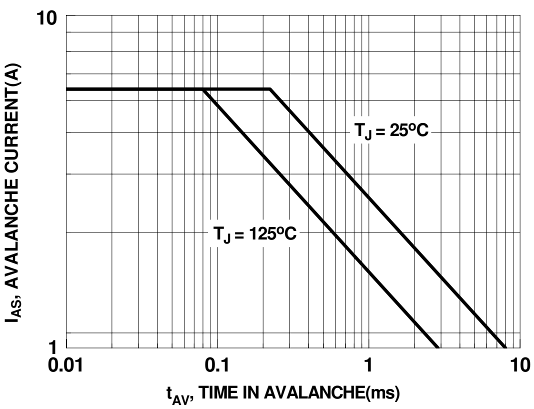


Figure 9. Unclamped Inductive Switching Capability

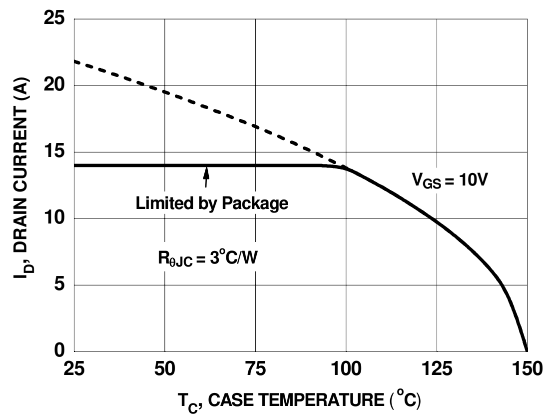


Figure 10. Maximum Continuous Drain Current vs Case Temperature

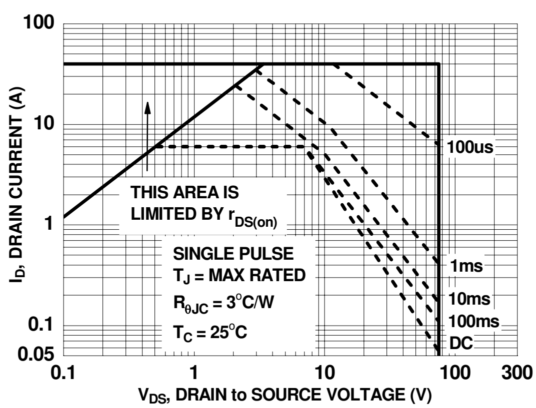


Figure 11. Forward Bias Safe Operating Area

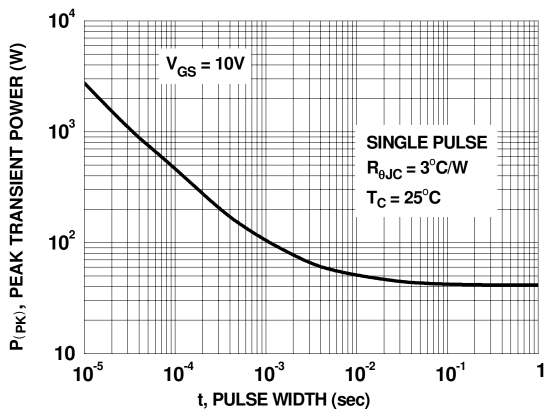


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

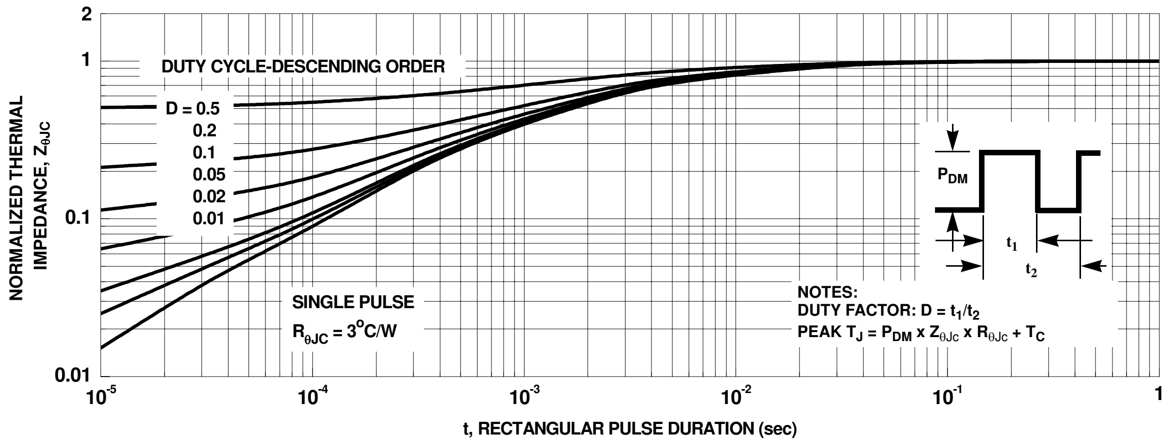


Figure 13. Transient Thermal Response Curve

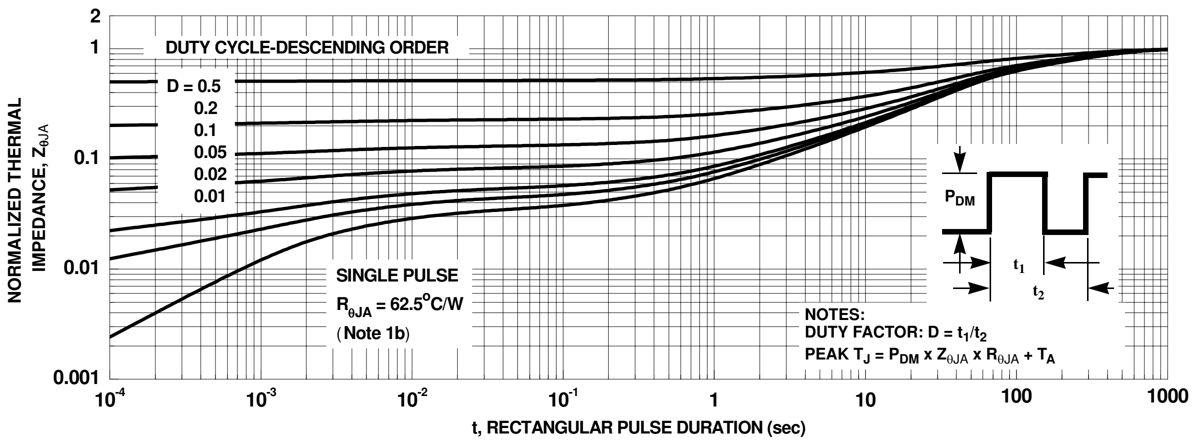


Figure 14. Transient Thermal Response Curve

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