TREX-S2-TMA

Motherboard for Stratix II FPGA Module

Data Book

TREX-S2-TMA

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Chapter 1

Introduction

TREX-S2-TMA is a motherboard developed exclusively for **TREX-S2** module which enables users to use ALL the powerful features of Altera StratixII FPGAs without having to worry about how to design the complex circuitry for power supply and configuration. Also, **TREX-S2-TMA** users can access all the available FPGA IOs of **TREX-S2** without having to worry about how to create and manufacture the complex motherboard.

TREX-S2-TMA package includes **ALL schematic** and **gerber files** so that users can easily create their own motherboards by modifying the TREX-S2-TMA design and layout files.

Users should read the **TREX-S2** Data Book before reading this manual.

Features

Figure 1.1 shows the photo of the **TREX-S2-TMA** motherboard. Figure 1.2 shows the photo **TREX-S2** FPGA module plugged on the **TREX-S2-TMA** motherboard. The important features are listed below:

- ✓ For TREX-S2 FPGA Module
- ✓ Provide twelve 70-pin 2.54mm-pitch connectors to allow users to access all the pins of the TREX-S2 FPGA module.
- ✓ Provide two clock sources (50Mhz and EXTCLK socket for external clock)
- ✓ Two independent programming circuits (JTAG and AS Mode)
- ✓ Four Jumpers to adjust **VCCB to 3.3V or 1.8V to set VCCIO in each bank group.**
- ✓ 8 User LEDs
- ✓ 1 Push Button
- ✓ Provide 5V cooling fun power.
- ✓ Provide RS232 port

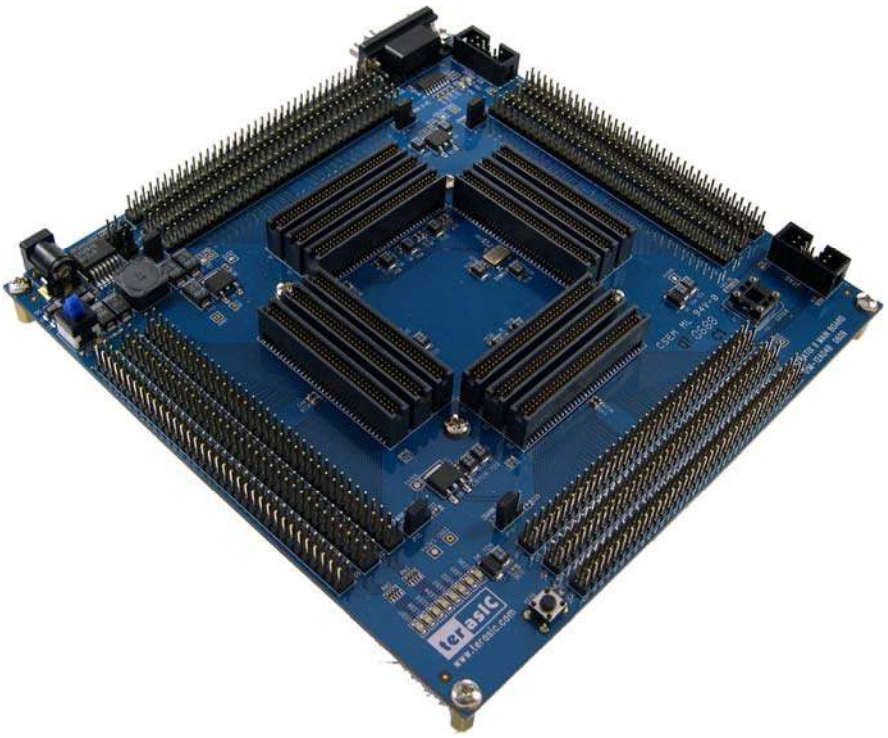


Figure 1.1. The TREX-S2-TMA Motherboard

Figure 1.2. TREX-S2 FPGA module plugged onto the TREX-S2-TMA motherboard

TREX-S2 Motherboard Selection Guide

TREX-S2 module has a series of motherboards designed for various applications. The available product portfolio is listed below. To request the detailed specification of the TREX-S2 motherboard, please send email to support@terasic.com. Figure 1.4 shows the TREX-S2 module with **TREX-S2-TMB** motherboard.

Product Code	Applications	Listing Price	Spec File Name
TREX-S2-TMA	**Prototyping**	**$325**	**TREXS2_TMA.pdf**
TREX-S2-TMB	**Prototyping with DDRII, SRAM, SDRAM**	**$395**	**TREXS2_TMB.pdf**

Figure 1.3 Terasic TREX-S2 Motherboard Part Number

Figure 1.4 Terasic TREX-S2 Module with TREX-S2-TMB Motherboard

Getting Help

Here are some places to get help if you encounter any problem:

- ✓ Email to support@terasic.com
- ✓ Taiwan & China: +886-3-550-8800
- ✓ Korea : +82-2-512-7661
- ✓ Japan: +81-428-77-7000
- ✓ English Support Line: +1-403-512-1336

Chapter 2

Architecture

This chapter describes the architecture of the **TREX-S2-TMA** motherboard including block diagram, connectors, and clocking system.

The Block Diagram

The block diagram of the **TREX-S2-TMA** module is described in Figure 2.1.

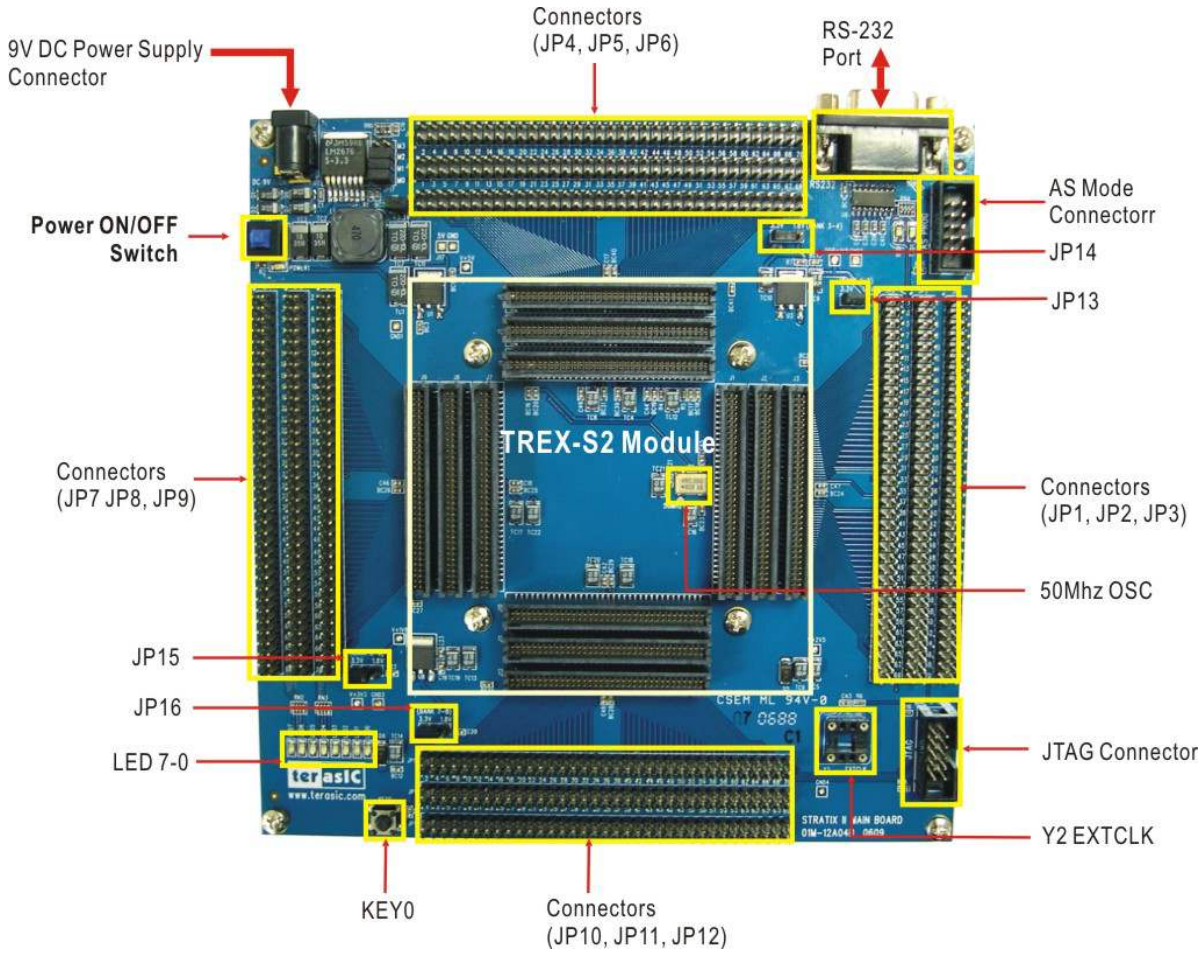


Figure 2.1 Terasic TREX-S2-TMA Module Block Diagram

Connectors

Figure 2.2 shows the connector diagram of the TREX-S2-TMA motherboard. Note that each pin in **JPN** connector is connected to the same pin in the **JN** connector of the **TREX-S2** module, where N = 1~12.

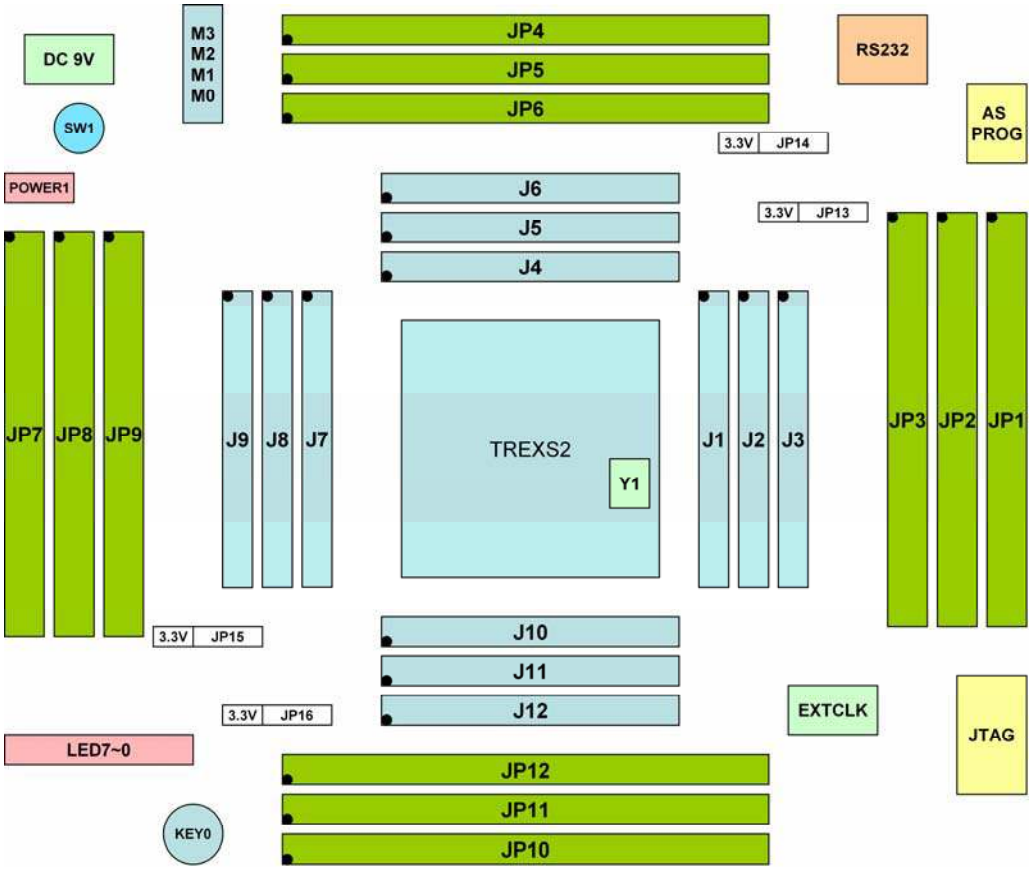


Figure 2.2. TREX-S2-TMA Motherboard Connector

Important Pin Assignment

Power ON/OFF and Power Indicator

- ✓ Power Jack (DC 9V) is for 9V DC Input
- ✓ Power Switch (SW1) is for power ON/OFF control.
- ✓ Power LED (POWER1) is for indicating the power status.

Clocking Source

Name	StratixII Pin Number
50MHZ	T30
EXTCLK	T32

Configuration Mode

- ✓ Support JTAG and AS Mode
- ✓ All the signals for JTAG and AS Mode are also shown in the surrounding connectors (J1-J12)

JTAG Mode

Name	StratixII Pin	Schematic Name	Connector
TCK	AF24	TRGTCK	J12(59)
TMS	AE24	TRGTMS	J12(60)
TDI	AL31	TRGTDI	J12(67)
TDO	C3	TRGTDO	J5(4)
TRST	AK30	TRGRESET	J12(68)

AS Mode

Name	StratixII Pin	Schematic Name	Connector
DCLK	B31	TRGDCLK	J6(68)
NCE	C30	TRGNCE	J6(67)
NCSO	G19	TRGNCSO	J5(43)
ASDO	F17	TRGASDO	J5(39)
DATA0	H19	TRGDATA0	J6(44)

User LEDs (LED 7 – 0)

- ✓ User can drive **0** to the corresponding pin to turn ON the LED.

Name	StratixII
LED0	AF2
LED1	AF1
LED2	AG2
LED3	AG1
LED4	AH2
LED5	AH1
LED6	AJ2
LED7	AJ1

Pushbutton – KEY0

✓ The pushbutton is an active-low device – logic level 0 is obtained when the KEY is pressed.

Name	StratixII
KEY0	AK4

RS-232 Port

✓ The RS232 circuit is built on the motherboard to provide users a tool to communicate with the user logic in FPGA.

Name	StratixII
TXD	E30
RXD	E29

JP1 – JP12

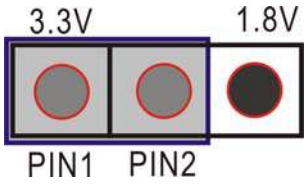
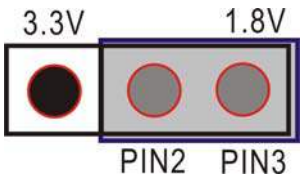
✓ Please refer to **TREX-S2** spec for the pin assignment of connector **J1 – J12**.

Connector Name	TREX-S1 Connector
JP1	J1
JP2	J2
JP3	J3
JP4	J4
JP5	J5
JP6	J6
JP7	J7
JP8	J8
JP9	J9
JP10	J10
JP11	J11
JP12	J12

Jumper Setting

JP13 - VCCIO (Bank 1 & 2) Selection

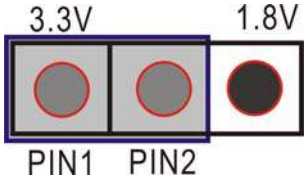
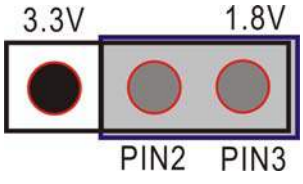
✓ JP13 is used to set the VCCIO (Bank Voltage) of Bank 1 and Bank 2.

Name	I/O Banks	VCCIO (Pin 1,2 short)	VCCIO (Pin 2,3 short)
VCCB12	1 & 2	3.3V 	1.8V 

NOTE on VREF: VREF pins of BANK 1 and BANK 2 are unconnected.

JP14 - VCCIO (Bank 3 & 4) Selection

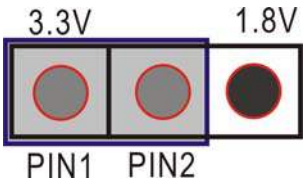
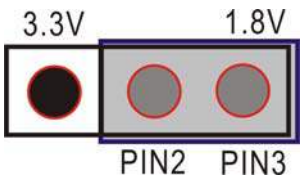
✓ JP14 is used to set the VCCIO (Bank Voltage) of Bank 3 and Bank 4.

Name	I/O Banks	VCCIO (Pin 1,2 short)	VCCIO (Pin 2,3 short)
VCCB34	3 & 4	3.3V 	1.8V 

NOTE on VREF: VREF pins of the BANK 3 and BANK 4 are fixed to the half level of the VCCIO. This feature enables users to connect differential devices like DDR memory devices.

JP15 - VCCIO (Bank 5 & 6) Selection

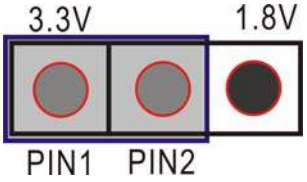
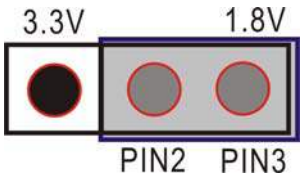
✓ JP15 is used to set the VCCIO (Bank Voltage) of Bank 5 and Bank 6

Name	I/O Banks	VCCIO (Pin 1,2 short)	VCCIO (Pin 2,3 short)
VCCB56	5 & 6	3.3V  	1.8V 

NOTE on VREF: VREF pins of BANK 5 and BANK 6 are unconnected.

JP16 - VCCIO (Bank 7 & 8) Selection

✓ JP15 is used to set the VCCIO (Bank Voltage) of Bank 5 and Bank 6

Name	I/O Banks	VCCIO (Pin 1,2 short)	VCCIO (Pin 2,3 short)
VCCB78	7 & 8	3.3V  	1.8V 

NOTE on VREF: VREF pins of BANK 7 and BANK 8 are unconnected.

MSEL (M3 M2 M1 M0)

✓ JP17 is to set the configuration scheme of the FPGA. The follow table is copied from Altera Stratix II handbook. Users can refer to the original document for detailed information. Note that **M3 – M0** represents **MSEL3 – MSEL0**, respectively.

To avoid any problems with detecting an incorrect configuration scheme, hard-wire the MSEL[] pins to V_{CCPD} and GND, without any pull-up or pull-down resistors. Do not drive the MSEL[] pins by a microprocessor or another device.

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0
Fast passive parallel (FPP)	0	0	0	0
Passive parallel asynchronous (PPA)	0	0	0	1
Passive serial (PS)	0	0	1	0
Remote system upgrade FPP *(1)*	0	1	0	0
Remote system upgrade PPA *(1)*	0	1	0	1
Remote system upgrade PS *(1)*	0	1	1	0
Fast AS (40 MHz) *(2)*	1	0	0	0
Remote system upgrade fast AS (40 MHz) *(2)*	1	0	0	1
FPP with decompression and/or design security feature enabled *(3)*	1	0	1	1
Remote system upgrade FPP with decompression and/or design security feature enabled *(1)*, *(3)*	1	1	0	0
AS (20 MHz) *(2)*	1	1	0	1
Remote system upgrade AS (20 MHz) *(2)*	1	1	1	0
JTAG-based configuration *(5)*	*(4)*	*(4)*	*(4)*	*(4)*

(1) These schemes require that you drive the RUnLU pin to specify either remote update or local update. For more information about remote system upgrades in Stratix II devices, refer to the chapter *Remote System Upgrades With Stratix II & Stratix II GX Devices* in Volume 2 of the *Stratix II Device Handbook* or the *Stratis II GX Device Handbook*.

(2) Only the EPCS16 and EPCS64 devices support up to a 40 MHz DCLK. Other EPCS devices support up to a 20 MHz DCLK. Refer to the *Serial Configuration Devices Data Sheet* for more information.

(3) These modes are only supported when using a MAX II device or a microprocessor with flash memory for configuration. In these modes, the host system must output a DCLK that is 4× the data rate.

(4) Do not leave the MSEL pins floating. Connect them to V_{CCPD} or ground. These pins support the non-JTAG configuration scheme used in production. If only JTAG configuration is used, you should connect the MSEL pins to ground.

(5) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

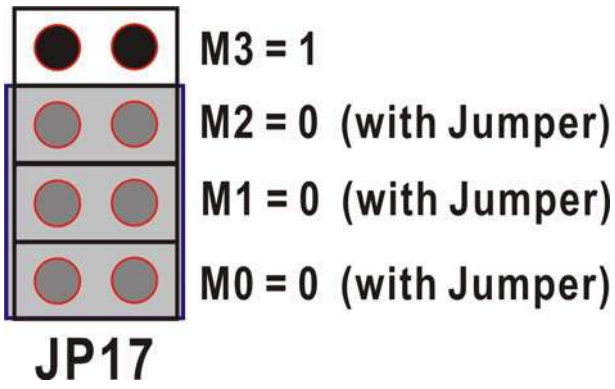


Figure 2.3. JP17 Jumper setup for **Fast AS Mode**

M0, M1 and M2=0 when jumper is connected.

M3=1 when jumper is unconnected.

Chapter 3

Electrical and Mechanical Specifications

This chapter describes the important Electrical and Mechanical specifications of TREX-S2-TMA, including how to plug or unplug the TREX-S2 from its associated main boards.

Operation and Environment Condition

This section describes the electrical specifications of **TREX-S2-TMA**

- ✓ Power Consumption: The TREX-S2-TMA power consumption is dominated by the TREX-S2 module power consumption. Please refer to the TREX-S2 user manual chapter 3.
- ✓ Power Supplier Mechanism
  - DC_9V: Provide form external adapter. The maximum value for this current is 2.6A. (1.3A for EP2S60, 2.6A for EP2S180)
  - VCC33: Generate form DC to DC circuit. The maximum value for this current is 10A. (3A for EP2S60, 10A for EP2S180)
  - VCC18: Generate form linear regulator. The maximum value for this current is 1A x 2.
  - VCC5: Generate form linear regulator. The maximum value for this current is 1A.

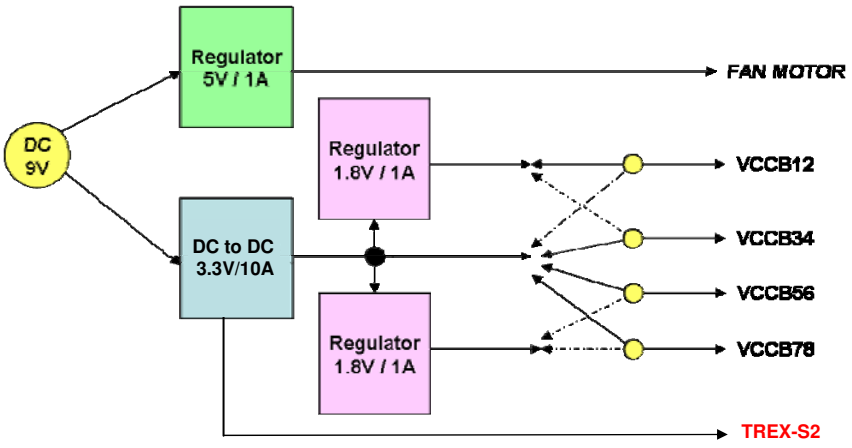


Figure 3.1 The Bank Voltage Selection Scheme

TREX-S2-TMA Schematic and Layout File

The CD-ROM attached includes the following files for users to create their own motherboards by modifying the schematic and layout files of the **TREX-S2-TMA** motherboard. This is to help users to achieve their goals within the shortest time frame.

■ **CD-ROM Content**

Type and Name	CD-ROM Folder Name
TREX-S2-TMA User Manual	**TMA_user_manual**
Schematic File	**TMA_schematic**
Layout File	**TMA_layout**
Quartus II Porject – Default Demo	**TMA_default_demo**
Quartus II Project – Loopback	**TMA_loopback**

How to plug and unplug the TREX-S2 Module

TREX-S2 has 12 connectors for connecting itself to a motherboard. It is very difficult to unplug the module once it is installed on the motherboard. Therefore, we designed a tool to allow users to easily unplug the module from the motherboard. Please refer to Figure 3.2 for the FPGA Module Opener.

✓ Note that when you design your own motherboards, you need to reserve enough empty space around the connectors for the opener's stand. Please use the attached layout files in CD-ROM as the starting point.

✓ **Please refer to the TS2withMotherboard.pdf to get more detailed steps about how to connect and detach the TREX-S2 FPGA module with TREX-S2-TMA/TMB motherboard.**

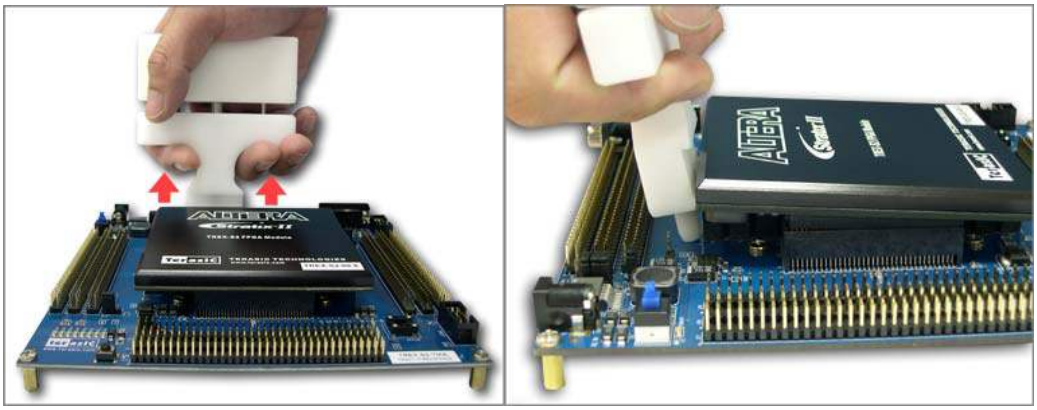


Figure 3.2 Use the Terasic FPGA Module Opener to unplug the TREX-S2 module

Chapter 4

Appendix

Part Number of Component on Board

Please send email to **support@terasic.com** for detailed BOM information if you cannot find

For EP2S60 (v1.2 PCB)

Component Type	Manufacturer	Vender Part Number	Reference
Regulator	UTC	78D05AL	U1
Regulator	NS	LM2676SX-3.3	U2
Regulator	AME	AME1117ECCTZ	U3,U8
IC	MAXIM	MAX232CSET	U6
Oscillator	MEC	3SWO-AT-50.000	Y1
Socket	LEAMAX	21218/4PNE	Y2
Connector	SAMTEC	TFC-135-32-L-D-LC	J1~J12

For EP2S60 and EP2S180 (v1.3 PCB)

Component Type	Manufacturer	Vender Part Number	Reference
Regulator	UTC	78D05AL	REG1
Regulator	LINEAR	LTM6400EV	REG2
Regulator	AME	AME1117ECCTZ	REG3, REG4
IC	MAXIM	MAX232CSET	U1
Socket	LEAMAX	21218/4PNE	Y1
Oscillator	MEC	3SWO-AT-50.000	Y2
Connector	SAMTEC	TFC-135-32-L-D-LC	J1~J12

Revision History

Date	Change Log
Mar 23, 2006 (SP)	Initial Version
Aug 15, 2006 (JC)	Update for v1.3 PCB.

Always Visit TREX-S2 Webpage for New Motherboard

We will be continuing creating various main board and labs on our DE2 webpage.

Please visit TREXS2.terasic.com for more information.