

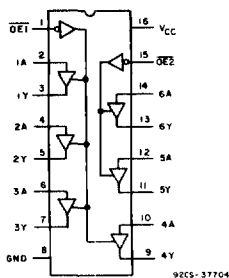
File Number 1538

Advance Information/
Preliminary Data

CD54/74HC367, CD54/74HCT367 CD54/74HC368, CD54/74HCT368

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM



CD54/74HC367, HCT367

Hex Buffer/Line Driver, 3-State

Non-Inverting and Inverting

Type Features:

- Buffered inputs
- High current bus driver outputs
- Two independent 3-state enable controls
- Typical propagation delay $t_{PHL}, t_{PLH} = 8 \text{ ns} @ V_{CC} = 5 \text{ V}, C_L = 15 \text{ pF}$

The RCA-CD54/74HC367, 368 and CD54/74HCT367, 368 silicon gate CMOS 3-state buffers are general-purpose high-speed non-inverting and inverting buffers. They have high drive current outputs which enable high-speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The CD54/74HC, HCT367 are non-inverting buffers, whereas the CD54/74HC, HCT368 are inverting buffers. These devices have two output enables, one enable (OE1) controls 4 gates and the other (OE2) controls the remaining 2 gates.

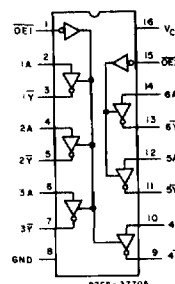
The CD54/74HCT367 and CD54/74HCT368 logic families are speed, function, and pin compatible with the standard 54LS/74LS logic family.

The CD54HC367 and CD54HCT367 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC367 and CD74HCT367 are in 16-lead dual-in-line plastic packages (E suffix), also in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to +85° C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 30\%, N_{IH} = 30\%; @ V_{CC} = 5 \text{ V}$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8 \text{ V Max.}, V_{IH} = 2 \text{ V Min.}$
CMOS Input Compatibility
 $I_{IL}, I_{IH} \leq 1 \mu\text{A} @ V_{OL}, V_{OH}$

FUNCTIONAL DIAGRAM



CD54/74HC368, HCT368

CD54/74HC367, CD54/74HCT367 CD54/74HC368, CD54/74HCT368

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{cc}): (Voltages referenced to ground)	-0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{ik} (FOR $V_i < -0.5$ V OR $V_i > V_{cc} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{ok} (FOR $V_o < -0.5$ V OR $V_o > V_{cc} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{cc} + 0.5$ V)	± 35 mA
DC V_{cc} OR GROUND CURRENT (I_{cc})	± 70 mA
POWER DISSIPATION PER PACKAGE (P_b):	
For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E)	500 mW
For $T_A = -60$ to -85° C (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -55$ to -100° C (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to -125° C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ$ C to 70 mW
OPERATING TEMPERATURE RANGE (T_A)	
PACKAGE TYPE F, H	-55 to $+125^\circ$ C
PACKAGE TYPE E, M	-40 to $+85^\circ$ C
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ$ C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 in. (1.59 \pm 0.79 mm) from case for 10 s max	-265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	$+300^\circ$ C

TRUTH TABLES

Inputs		Outputs
\overline{OE}	A	Y
L	L	L
L	H	H
H	X	(Z)

CD54/74HC, HCT367

Inputs		Outputs
\overline{OE}	A	Y
L	L	H
L	H	L
H	X	(Z)

CD54/74HC, HCT368

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.
(Z) = High impedance (off) state.

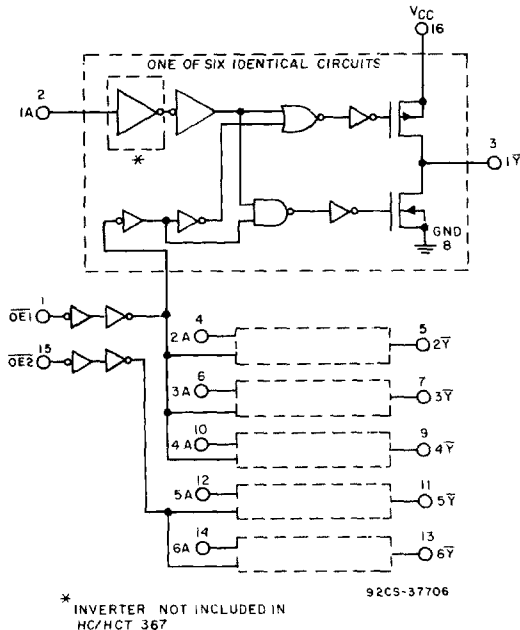


Fig. 1 - Logic diagram for HC/HCT367 and HC/HCT368.
(Outputs for HC/HCT367 are complements of those shown, i.e., 1Y, 2Y, etc.).

CD54/74HC367, CD54/74HCT367 CD54/74HC368, CD54/74HCT368

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC367/368/CD54HC367/368										CD74HCT367/368/CD54HCT367/368								UNITS			
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE			TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE			54HCT TYPE		
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C			V _I V	V _{CC} V	+25°C			-40/ +85°C			-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max	Min			Typ	Max	Min	Max	Min		Max		
High-Level Input Voltage	V _{IH}		2	1.5	—	—	1.5	—	1.5	—	—	4.5		2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	to										
			6	4.2	—	—	4.2	—	4.2	—	—	5.5										
Low-Level Input Voltage	V _{IL}		2	—	—	0.5	—	0.5	—	0.5	—	4.5		—	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	to										
			6	—	—	1.8	—	1.8	—	1.8	—	5.5										
High-Level Output Voltage	V _{OH}	V _{IL} or -0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or	V _{IL}	4.5	4.4	—	—	4.4	—	4.4	—	V	
CMOS Loads		V _{IH}	6	5.9	—	—	5.9	—	5.9	—	V _{IH}											
TTL Loads (Bus Driver)		V _{IL} or -6	4.5	3.98	—	—	3.84	—	3.7	—	V _{IL} or	4.5	3.98	—	—	3.84	—	3.7	—	V		
		V _{IH}	7.8	6	5.48	—	5.34	—	5.2	—	V _{IH}											
Low-Level Output Voltage	V _{OL}	V _{IL} or 0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or	V _{IL}	4.5	—	—	0.1	—	0.1	—	0.1	V	
CMOS Loads		V _{IH}	6	—	—	0.1	—	0.1	—	0.1	V _{IH}											
TTL Loads (Bus Driver)		V _{IL} or 6	4.5	—	—	0.26	—	0.33	—	0.4	V _{IL} or	4.5	—	—	0.26	—	0.33	—	0.4	V		
		V _{IH}	7.8	6	—	—	0.26	—	0.33	—	V _{IH}											
Input Leakage Current	I _I	V _{CC} or Gnd	6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA		
Quiescent Device Current	I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA	
Additional Quiescent Device Current per Input Pin: 1 Unit Load	ΔI _{CC} *										V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA		
3-State Leakage Current	I _{OZ}	V _{IL} or V _{IH}	V _O = V _{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V _{IL} or V _{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA	

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
OE1	0.6
ALL OTHERS	0.55

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC367, CD54/74HCT367 CD54/74HC368, CD54/74HCT368

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A =Full Package Temperature Range) V _{CC} * CD54/74HC Types CD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V _I , V _O	0	V _{CC}	V
Operating Temperature T _A : CD74 Types CD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall Times t _r , t _f at 2 V at 4.5 V at 6 V	0 0 0	1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, C_L=15 pF, T_A=25° C, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	TYPICAL				UNITS
		367		368		
		HC	HCT	HC	HCT	
Propagation Delay Data to Output	t _{PHL} t _{PLH}	8	9	9	11	ns
Output Enable and Disable to Outputs	t _{PZH} , t _{PZL} , t _{PHZ} , t _{PLZ}	12	14	12	14	ns
Power Dissipation Capacitance *	C _{PD}	40	42	40	42	pF

*C_{PD} is used to determine the dynamic power consumption, per buffer.

PD = V_{CC}² f_i (C_{PD} + C_L) where:

f_i = input frequency

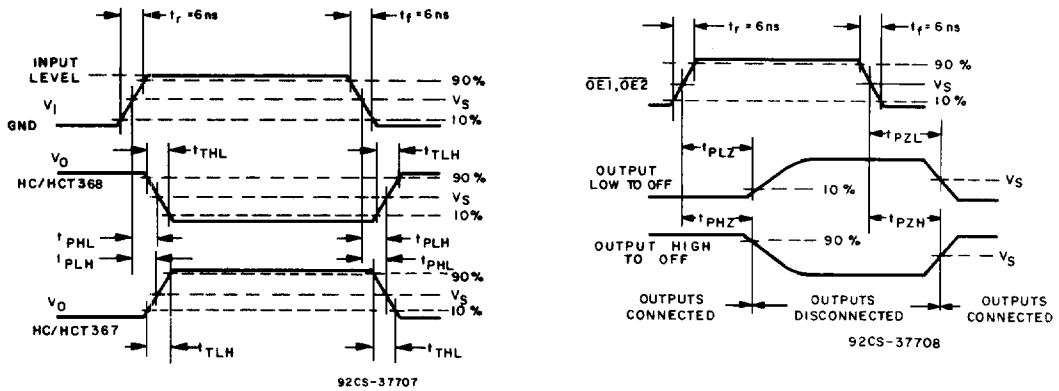
C_L = output load capacitance

V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r, t_f=6 ns)

CHARACTERISTIC	SYMBOL	V _{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay Data to Outputs HC/HCT367	t _{PLH} t _{PHL}	2 4.5 6	— — —	105 21 18	— — —	— — —	— — —	130 26 24	— — —	— — —	31 32 27	— — —	— — —	38	ns
Propagation Delay Data to Outputs HC/HCT368	t _{PLH} t _{PHL}	2 4.5 6	— — —	105 21 18	— — —	— — —	— — —	130 26 24	— — —	— — —	130 38 27	— — —	— — —	160 32 27	ns
Propagation Delay Output Enable & Disable to Outputs	t _{PZH} , t _{PZL} , t _{PHZ} , t _{PLZ}	2 4.5 6	— — —	150 30 26	— — —	— — —	— — —	190 38 33	— — —	— — —	44 45 38	— — —	— — —	225 53	ns
Output Transition Time	t _{TLH} t _{THL}	2 4.5 6	— — —	60 12 10	— — —	— — —	— — —	75 15 13	— — —	— — —	90 18 15	— — —	— — —	18	ns
Input Capacitance	C _I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C _O		—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC367, CD54/74HCT367 CD54/74HC368, CD54/74HCT368



Input Level	54/74HC	54/74HCT
	VCC	3 V
Switching Voltage, Vs	50% VCC	1.3 V

Fig. 2 - Transition times and propagation delay times.

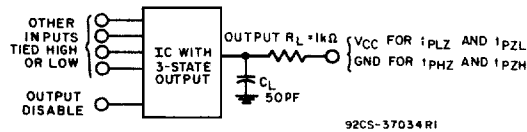


Fig. 3 - Three-state propagation delay test circuit.