October 1988
Revised March 2000

DM9368
7-Segment Decoder/Driver/Latch with Constant Current Source Outputs

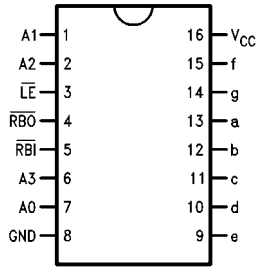
General Description

The DM9368 is a 7-segment decoder driver incorporating input latches and constant current output circuits to drive common cathode type LED displays directly.

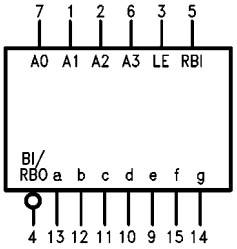
Ordering Code:

Order Number	Package Number	Package Description
DM9638N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagram



Logic Symbol



V_{CC} = Pin 16
GND = PIN 8

Pin Descriptions

Pin Name	Description
A0–A3	Address (Data) Inputs
$\overline{RBO}$	Ripple Blanking Output (Active LOW)
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
a–g	Segment Drivers-Outputs
$\overline{LE}$	Latch Enable Input (Active LOW)

Truth Table

BINARY STATE	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	A3	A2	A1	A0	a	b	c	d	e	f	g	$\overline{RBO}$	
—	H	*	X	X	X	X	← STABLE →							H	STABLE
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	BLANK
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	L	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	H	H	A
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	C
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	E
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	F
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L**	BLANK

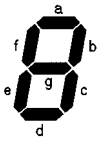
*The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

*The $\overline{RBO}$ used as an input overrides all other input conditions.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial



Functional Description

The DM9368 is a 7-segment decoder driver designed to drive 7-segment common cathode LED displays. The DM9368 drives any common cathode LED display rated at a nominal 20 mA at 1.7V per segment without need for current limiting resistors.

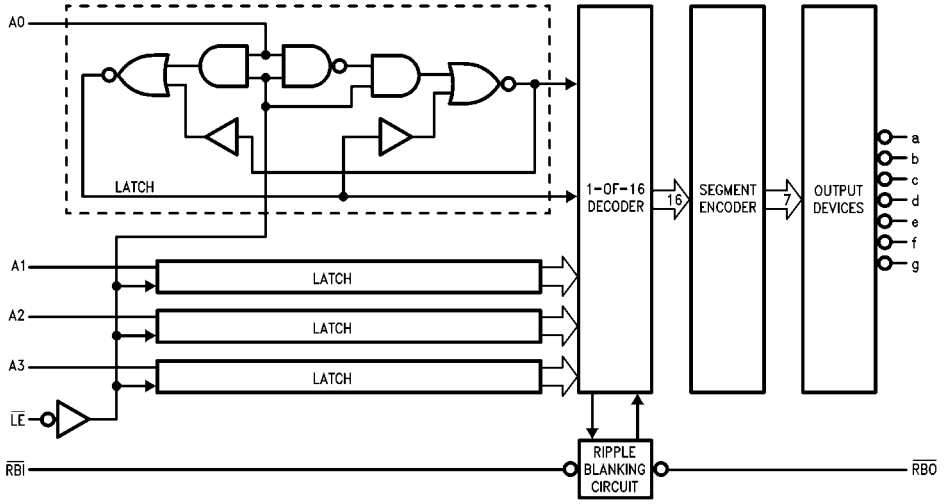
This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a hexadecimal decode format which produces numeric codes “0” thru “9” and alpha codes “A” through “F” using upper and lower case fonts.

Latches on the four data inputs are controlled by an active LOW latch enable $\overline{LE}$. When the $\overline{LE}$ is LOW, the state of the outputs is determined by the input data. When the $\overline{LE}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{LE}$ pulse width necessary to accept and store data is typically 30 ns which allows data to be strobed into the DM9368 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

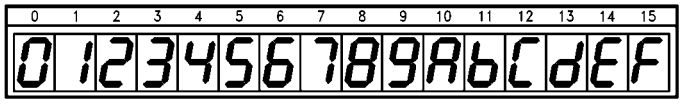
Another feature of the DM9368 is that the unit loading on the data inputs is very low (–100 µA Max) when the latch enable is HIGH. This allows DM9368s to be driven from an MOS device in multiplex mode without the need for drivers on the data lines.

The DM9368 also has provision for automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeros. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

Logic Diagram

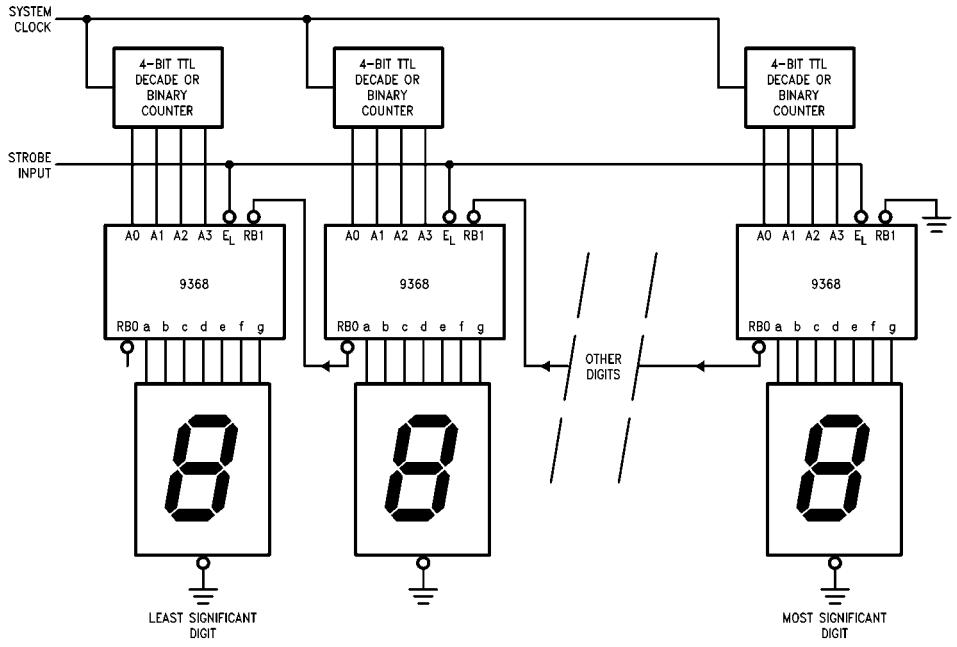


Numerical Designations



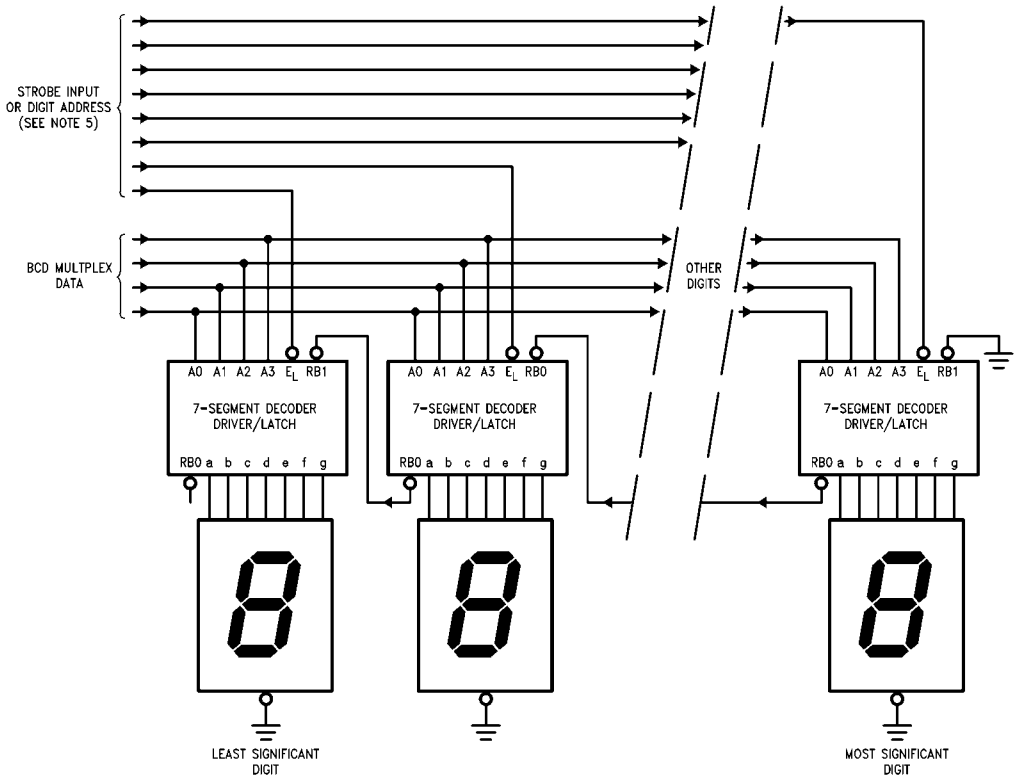
Parallel Data Display System with Ripply Blanking

Common Cathode LED Display



Display Demultiplexing System with Ripple Blanking

Common Cathode LED Display



Note: Digit address data must be non-overlapping. Standard TTL decoders like the 9301, 9311, 7442 or 74155 must be strobed, since the address decoding glitches could cause erroneous data to be strobed into the latches.

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current		−80		µA
I_{OL}	LOW Level Output Current $\overline{RBO}$			3.2	mA
T_A	Free Air Operating Temperature	0		70	°C
$t_S(H)$	Setup Time HIGH A_n to $\overline{LE}$	30			ns
$t_H(H)$	Hold Time HIGH A_n to $\overline{LE}$	0			ns
$t_S(L)$	Setup Time LOW A_n to $\overline{LE}$	20			ns
$t_H(L)$	Hold Time LOW A_n to $\overline{LE}$	0			ns
$t_W(L)$	$\overline{LE}$ Pulse Width LOW	45			ns
I_{OH}	Segment Output HIGH Current	−16		−22	mA
I_{OL}	Segment Output LOW Current	−250		250	µA

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−18		−57	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs OPEN, Data & Latch Inputs = 0V			67	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

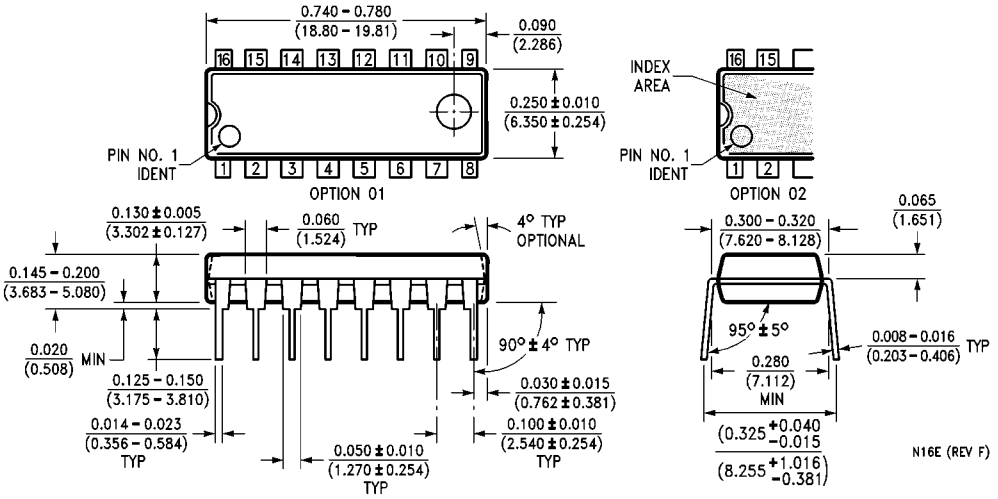
Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	C_L = 15 pF, R_L = 100Ω		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to a–g		50 75	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to a–g		70 90	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E