

# MC74HC161A, MC74HC163A



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## Presettable Counters High-Performance Silicon-Gate CMOS

The MC74HC161A and HC163A are identical in pinout to the LS161 and LS163. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

The HC161A and HC163A are programmable 4-bit binary counters with asynchronous and synchronous reset, respectively.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 192 FETs or 48 Equivalent Gates

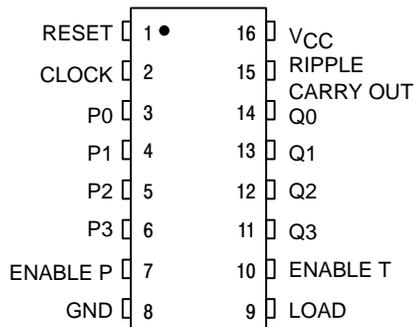


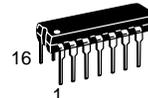
Figure 1. Pin Assignment

### FUNCTION TABLE

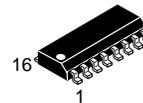
Inputs					Output
Clock	Reset*	Load	Enable P	Enable T	Q
	L	X	X	X	Reset
	H	L	X	X	Load Preset Data
	H	H	H	H	Count
	H	H	L	X	No Count
	H	H	X	L	No Count

\*HC163A only. HC161A is an Asynchronous Reset Device  
H = high level, L = low level, X = don't care

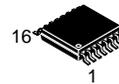
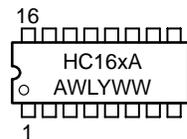
### MARKING DIAGRAMS



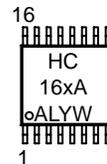
PDIP-16  
N SUFFIX  
CASE 648



SO-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



x = 1 or 3  
A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC74HC161AN	PDIP-16	2000/Box
MC74HC161AD	SOIC-16	48/Rail
MC74HC161ADR2	SOIC-16	2500/Reel
MC74HC161ADT	TSSOP-16	96/Rail
MC74HC161ADTR2	TSSOP-16	2500/Reel
MC74HC163AN	PDIP-16	2000/Box
MC74HC163AD	SOIC-16	48/Rail
MC74HC163ADR2	SOIC-16	2500/Reel
MC74HC163ADT	TSSOP-16	96/Rail
MC74HC163ADTR2	TSSOP-16	2500/Reel

## MC74HC161A, MC74HC163A

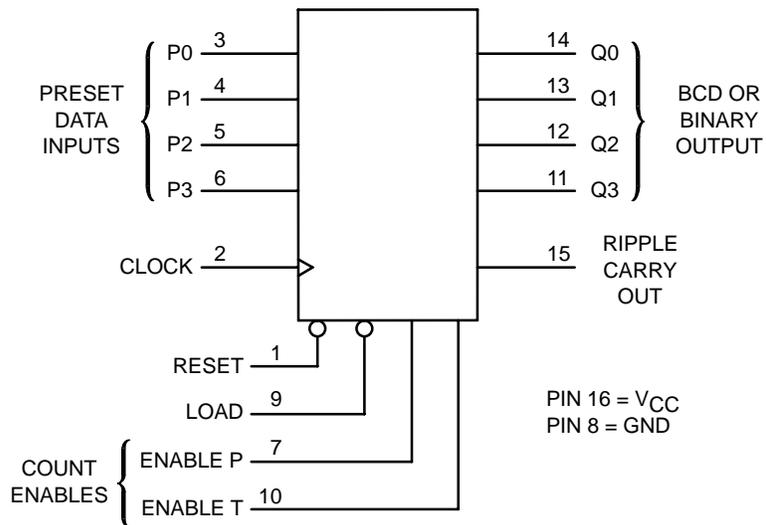


Figure 2. Logic Diagram

### DEVICE/MODE TABLE

Device	Count Mode	Reset Mode
HC161A	Binary	Asynchronous
HC163A	Binary	Synchronous

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## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>O</sub>	DC Output Voltage (Note 2)	-0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	DC Input Diode Current	±20	mA
I <sub>OK</sub>	DC Output Diode Current	±25	mA
I <sub>O</sub>	DC Output Sink Current	±25	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±50	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±50	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	C
T <sub>J</sub>	Junction Temperature Under Bias	+150	C
θ <sub>JA</sub>	Thermal Resistance	PDIP SOIC TSSOP 78 112 148	C/W
P <sub>D</sub>	Power Dissipation in Still Air at 85 C	PDIP SOIC TSSOP 750 500 450	mW
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 30% – 35% UL-94-V0 (0.125 in)	
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5) > 2000 > 200 > 1000	V
I <sub>LATCH-UP</sub>	Latch-Up Performance	Above V <sub>CC</sub> and Below GND at 85 C (Note 6)	±300 mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
2. I<sub>O</sub> absolute maximum rating must be observed.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 4)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 3.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 600 500 400	ns

7. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55 to 25 C	≤ 85 C	≤ 125 C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 3.6 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	2.48	2.34	2.2	
			4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 3.6 mA  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	3.0	0.26	0.33	0.4	
			4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4.0	40	160	μA

8. Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

Symbol	Parameter	Figure	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25 C	≤ 85 C	≤ 125 C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle) (Note 9)	4, 10	2.0	6	5	4	MHz
			3.0	15	12	10	
			4.5	30	24	20	
			6.0	35	28	24	
t <sub>PLH</sub>	Maximum Propagation Delay, Clock to Q	4, 10	2.0	120	160	200	ns
			3.0	75	120	150	
			4.5	20	23	28	
			6.0	16	20	22	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q (HC161A Only)	4, 10	2.0	145	185	220	ns
			3.0	100	135	150	
			4.5	22	25	30	
			6.0	18	20	23	
t <sub>PLH</sub>	Maximum Propagation Delay, Enable T to Ripple Carry Out	6, 10	2.0	110	150	190	ns
			3.0	60	115	140	
			4.5	16	18	20	
			6.0	14	15	17	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Ripple Carry Out (HC161A Only)	6, 10	2.0	135	175	210	ns
			3.0	100	130	160	
			4.5	18	20	22	
			6.0	15	16	20	
t <sub>PLH</sub>	Maximum Propagation Delay, Clock to Ripple Carry Out	4, 10	2.0	120	160	200	ns
			3.0	75	135	150	
			4.5	22	27	30	
			6.0	18	22	25	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Ripple Carry Out (HC161A Only)	4, 10	2.0	145	185	220	ns
			3.0	100	135	150	
			4.5	22	28	35	
			6.0	20	24	28	
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Ripple Carry Out (HC161A Only)	5, 10	2.0	155	190	230	ns
			3.0	120	140	155	
			4.5	22	26	30	
			6.0	18	22	25	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output	5, 10	2.0	75	95	110	ns
			3.0	30	40	55	
			4.5	15	19	22	
			6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	4, 10	—	10	10	10	pF

9. Applies to noncascaded/nonsynchronous clocked configurations only with synchronously cascaded counters. (1) Clock to Ripple Carry Out propagation delays. (2) Enable T or Enable P to Clock setup times and (3) Clock to Enable T or Enable P hold times determine f<sub>max</sub>. However, if Ripple Carry out of each stage is tied to the Clock of the next stage (nonsynchronously clocked) the f<sub>max</sub> in the table above is applicable. See Applications information in this data sheet.

10. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Gate) (Note 11)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	
			45

11. Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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**TIMING REQUIREMENTS** ( $C_L = 50$  pF, Input  $t_r = t_f = 6.0$  ns)

Symbol	Parameter	Figure	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25 C	≤ 85 C	≤ 125 C	
t <sub>su</sub>	Minimum Setup Time, Preset Data Inputs to Clock	8	2.0	40	60	80	ns
			3.0	20	30	40	
			4.5	15	20	30	
			6.0	12	18	20	
t <sub>su</sub>	Minimum Setup Time, Load to Clock	8	2.0	60	75	90	ns
			3.0	25	30	40	
			4.5	15	20	30	
			6.0	12	18	20	
t <sub>su</sub>	Minimum Setup Time, Reset to Clock (HC163A Only)	7	2.0	60	75	90	ns
			3.0	25	30	40	
			4.5	20	25	35	
			6.0	17	23	25	
t <sub>su</sub>	Minimum Setup Time, Enable T or Enable P to Clock	9	2.0	80	95	110	ns
			3.0	35	40	50	
			4.5	20	25	35	
			6.0	17	23	25	
t <sub>h</sub>	Minimum Hold Time, Clock to Load or Preset Data Inputs	8	2.0	3	3	3	ns
			3.0	3	3	3	
			4.5	3	3	3	
			6.0	3	3	3	
t <sub>h</sub>	Minimum Hold Time, Clock to Reset (HC163A Only)	7	2.0	3	3	3	ns
			3.0	3	3	3	
			4.5	3	3	3	
			6.0	3	3	3	
t <sub>h</sub>	Minimum Hold Time, Clock to Enable T or Enable P	9	2.0	3	3	3	ns
			3.0	3	3	3	
			4.5	3	3	3	
			6.0	3	3	3	
t <sub>rec</sub>	Minimum Recovery Time, Reset Inactive to Clock (HC161A Only)	5	2.0	80	95	110	ns
			3.0	35	40	50	
			4.5	15	20	26	
			6.0	12	17	23	
t <sub>rec</sub>	Minimum Recovery Time, Load Inactive to Clock	8	2.0	80	95	110	ns
			3.0	35	40	50	
			4.5	15	20	26	
			6.0	12	17	23	
t <sub>w</sub>	Minimum Pulse Width, Clock	4	2.0	60	75	90	ns
			3.0	25	30	40	
			4.5	12	15	18	
			6.0	10	13	15	
t <sub>w</sub>	Minimum Pulse Width, Reset (HC161A Only)	5	2.0	60	75	90	ns
			3.0	25	30	40	
			4.5	12	15	18	
			6.0	10	13	15	
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times		2.0	1000	1000	1000	ns
			3.0	800	800	800	
			4.5	500	500	500	
			6.0	400	400	400	

# MC74HC161A, MC74HC163A

## FUNCTION DESCRIPTION

The HC161A/163A are programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count-enable controls.

The HC161A and HC163A are binary counters with asynchronous Reset and synchronous Reset, respectively.

### INPUTS

#### Clock (Pin 2)

The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as resetting and loading, occur with the rising edge of the Clock input.

#### Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6)

These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (Pin 3) is the least-significant bit and P3 (Pin 6) is the most-significant bit.

### OUTPUTS

#### Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11)

These are the counter outputs. Q0 (Pin 14) is the least-significant bit and Q3 (Pin 11) is the most-significant bit.

#### Ripple Carry Out (Pin 15)

When the counter is in its maximum state, 1111, this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equation for this output is:

$$\text{Ripple Carry Out} = \text{Enable T} \cdot \text{Q0} \cdot \text{Q1} \cdot \text{Q2} \cdot \text{Q3}$$

### OUTPUT STATE DIAGRAMS

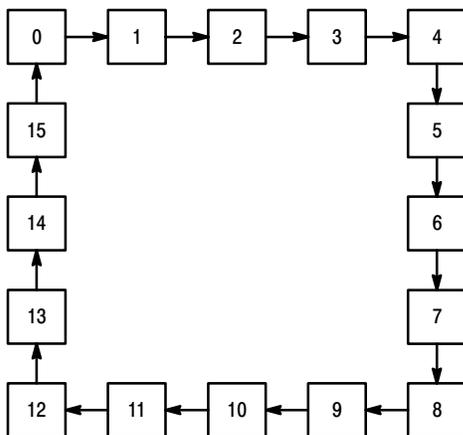


Figure 3. Binary Counters

### CONTROL FUNCTIONS

#### Resetting

A low level on the Reset pin (Pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to a low level. The HC161A resets asynchronously, and the HC163A resets with the rising edge of the Clock input (synchronous reset).

#### Loading

With the rising edge of the Clock, a low level on Load (Pin 9) loads the data from the Preset Data input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

#### Count Enable/Disable

These devices have two count-enable control pins: Enable P (Pin 7) and Enable T (Pin 10). The devices count when these two pins and the Load pin are high. The logic equation is:

$$\text{Count Enable} = \text{Enable P} \cdot \text{Enable T} \cdot \text{Load}$$

The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count-enable control: Enable T is both a count-enable and a Ripple-Carry Output control.

Table 1. Count Enable/Disable

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0 – Q3	Ripple Carry Out
H	H	H	Count	High when Q0–Q3 are maximum*
L	H	H	No Count	
X	L	H	No Count	High when Q0–Q3 are maximum*
X	X	L	No Count	L

\*Q0 through Q3 are maximum when Q3, Q2, Q1, Q0 = 1111.

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## SWITCHING WAVEFORMS

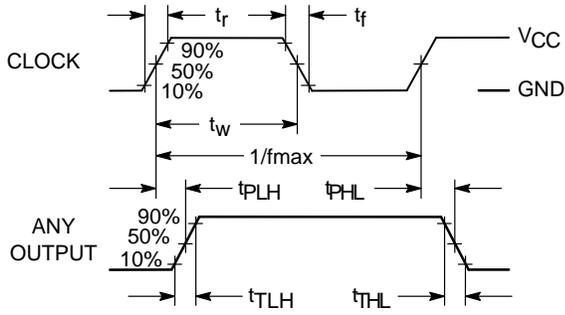


Figure 4.

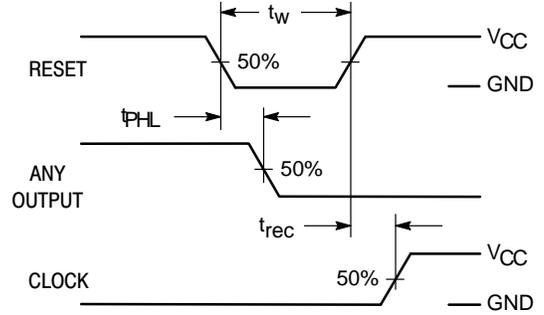


Figure 5.

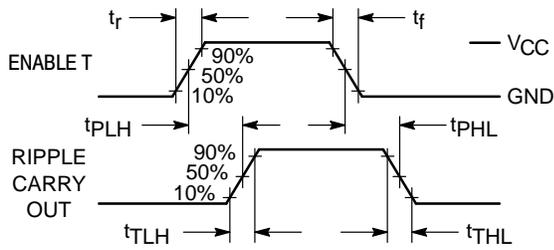


Figure 6.

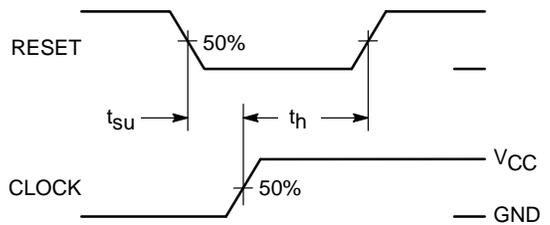


Figure 7. HC163A Only

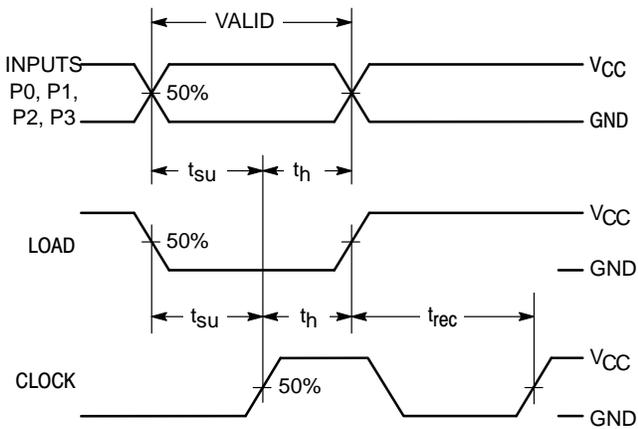


Figure 8.

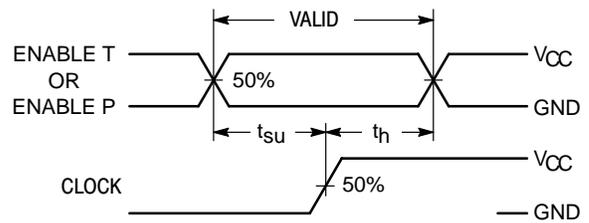
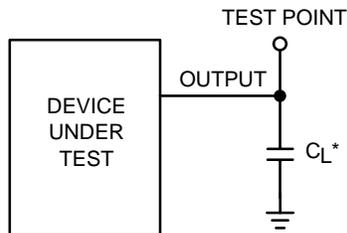


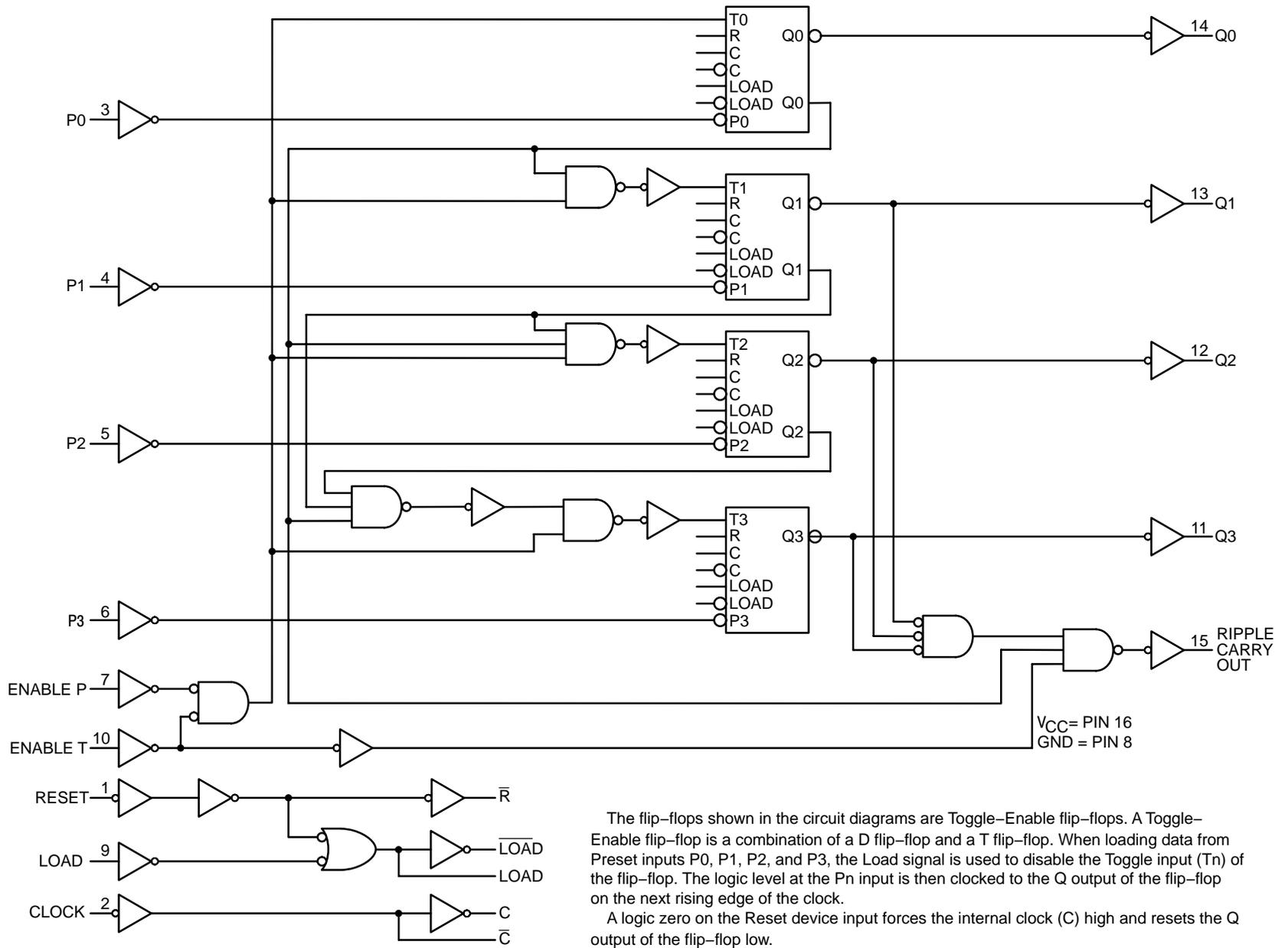
Figure 9.

## TEST CIRCUIT



\*Includes all probe and jig capacitance

Figure 10.



The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (T<sub>n</sub>) of the flip-flop. The logic level at the P<sub>n</sub> input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

Figure 11. 4-Bit Binary Counter with Asynchronous Reset (MC74HC161A)

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Sequence illustrated in waveforms:

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one and two.
4. Inhibit.

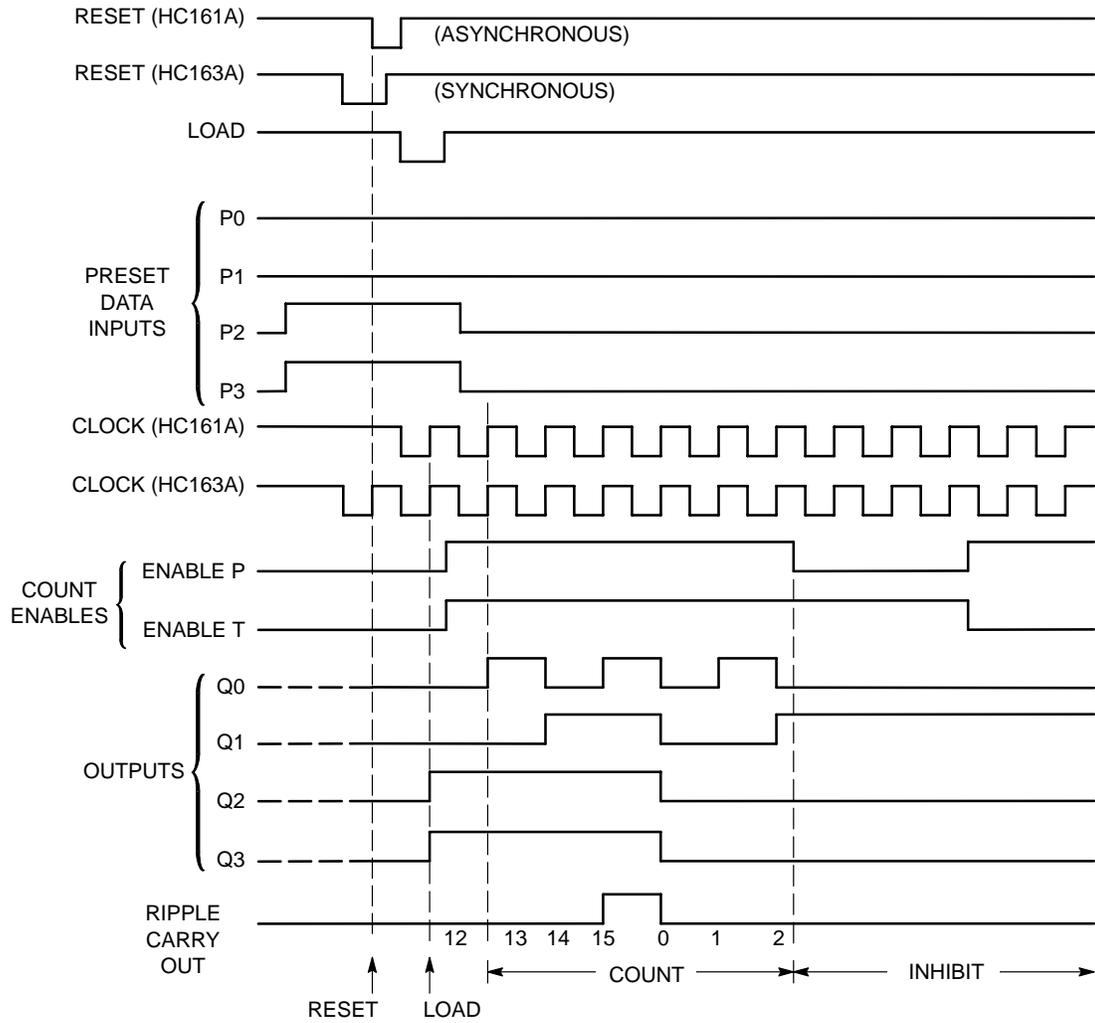
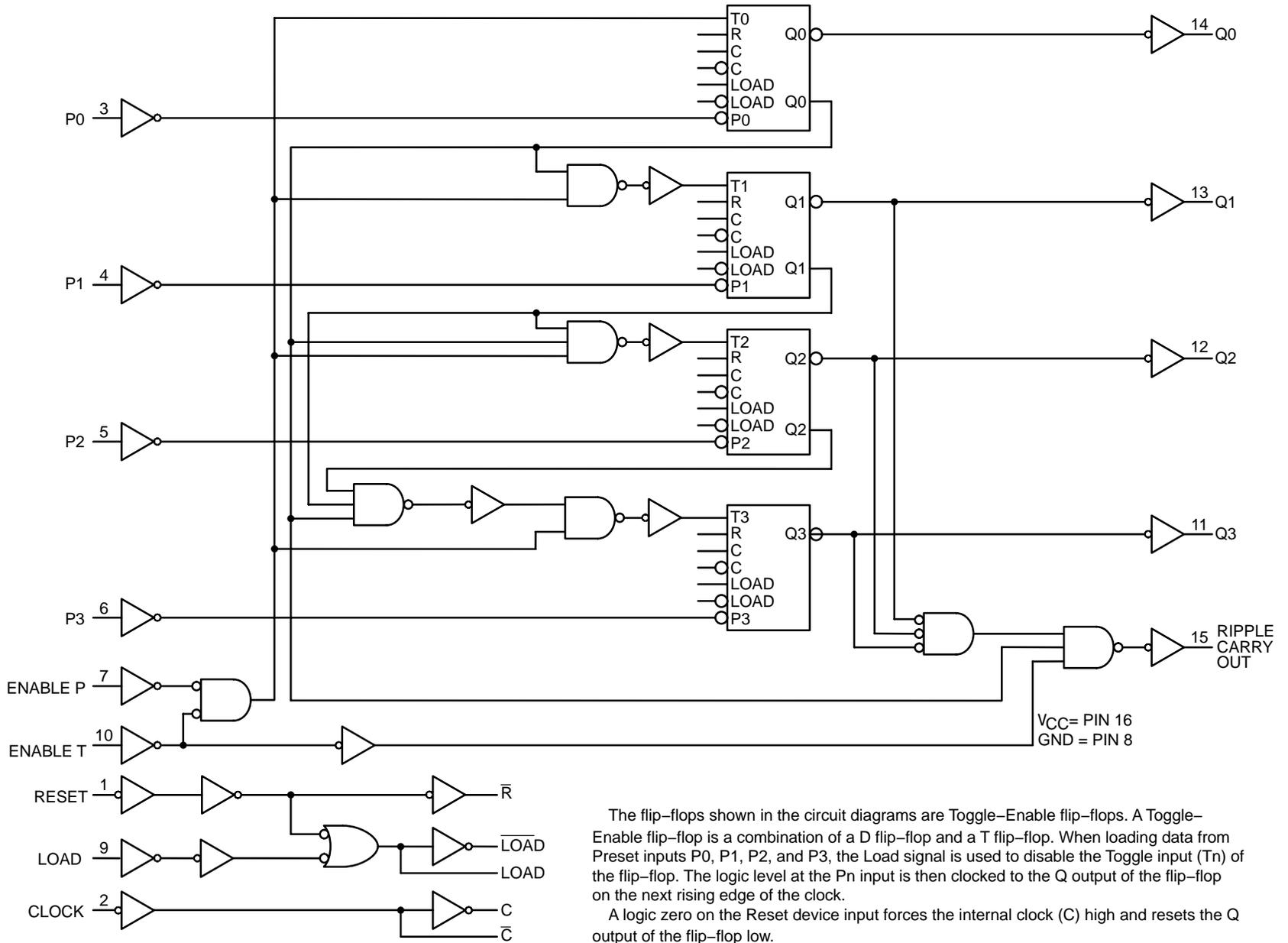


Figure 12. Timing Diagram



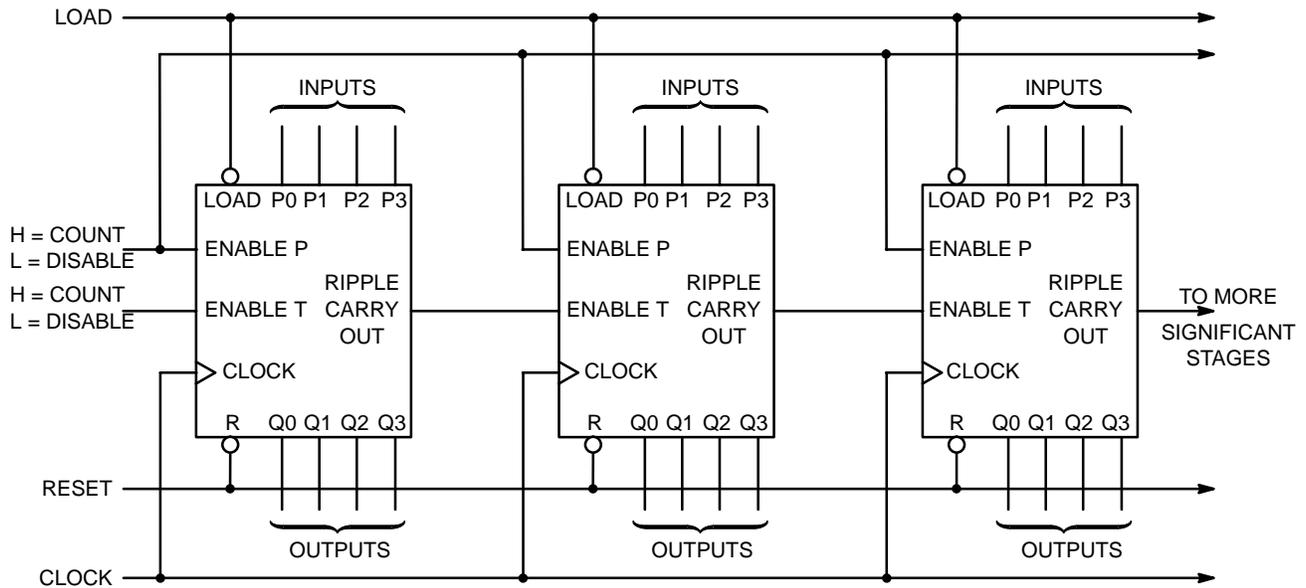
The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

Figure 13. 4-Bit Binary Counter with Synchronous Reset (MC74HC163A)

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## TYPICAL APPLICATIONS CASCADING



NOTE: When used in these cascaded configurations the clock  $f_{max}$  guaranteed limits may not apply. Actual performance will depend on number of stages. This limitation is due to set up times between Enable (Port) and Clock.

Figure 14. N-Bit Synchronous Counters

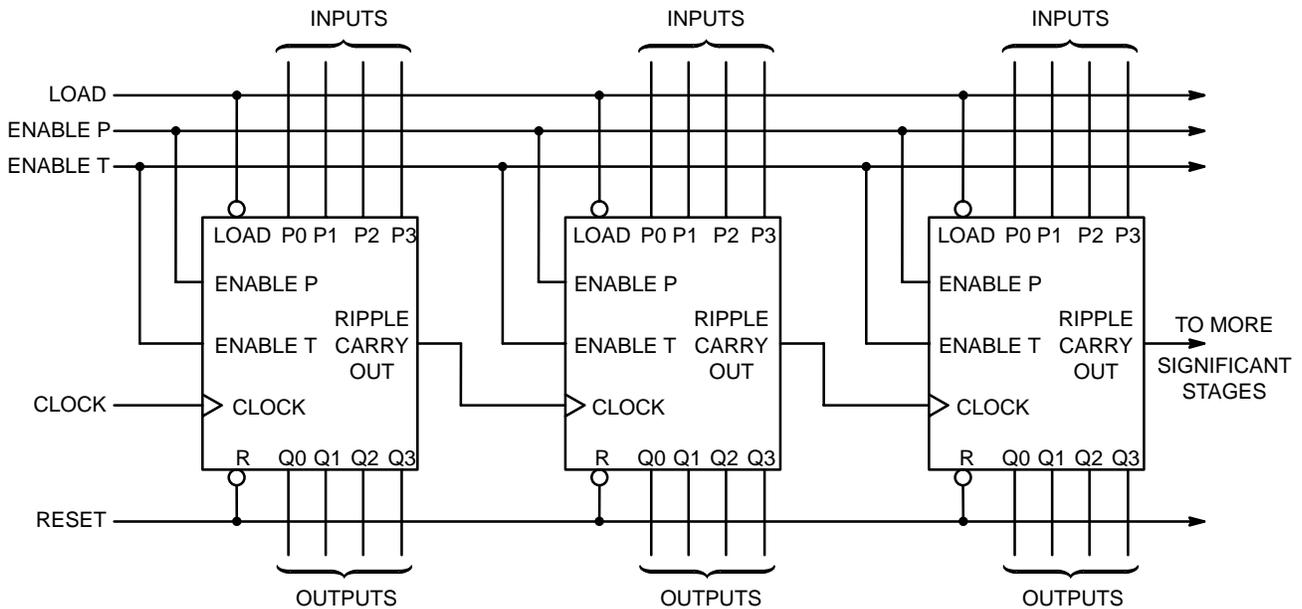


Figure 15. Nibble Ripple Counter

# MC74HC161A, MC74HC163A

## TYPICAL APPLICATIONS VARYING THE MODULUS

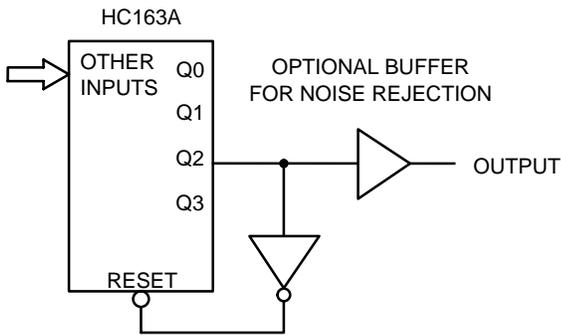


Figure 16. Modulo-5 Counter

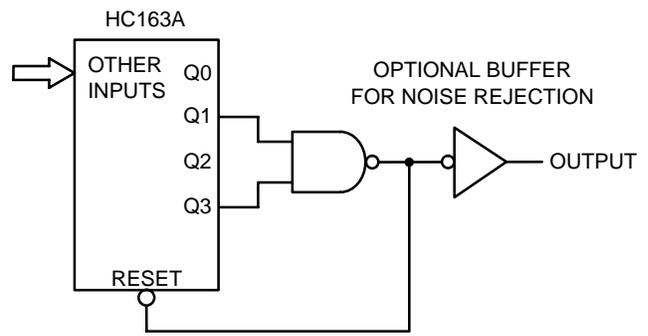


Figure 17. Modulo-11 Counter

The HC163A facilitates designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous Reset.