Single 2-input NOR gate Rev. 12 — 29 November 2016

Product data sheet

General description 1.

The 74LVC1G02 provides the single 2-input NOR function.

Input can be driven from either 3.3 V or 5 V devices. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Features and benefits 2.

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- \pm 24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



3. Ordering information

Table 1. Ordering information

Type number	Package	Package										
	Temperature range	Name	Description	Version								
74LVC1G02GW	–40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1								
74LVC1G02GV	–40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753								
74LVC1G02GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 \times 1.45 \times 0.5 mm	SOT886								
74LVC1G02GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 \times 1 \times 0.5 mm	SOT891								
74LVC1G02GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115								
74LVC1G02GS	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $1.0 \times 1.0 \times 0.35$ mm	SOT1202								
74LVC1G02GX	-40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body $0.8 \times 0.8 \times 0.35$ mm	SOT1226								

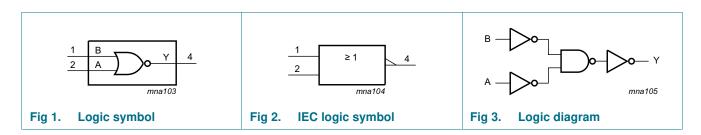
4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G02GW	VB
74LVC1G02GV	V02
74LVC1G02GM	VB
74LVC1G02GF	VB
74LVC1G02GN	VB
74LVC1G02GS	VB
74LVC1G02GX	VB

^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

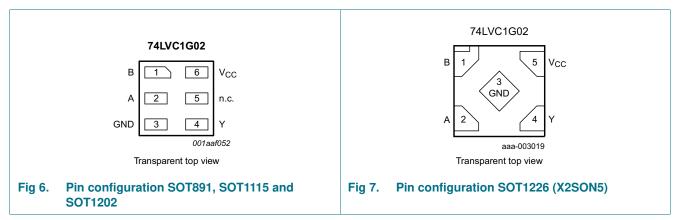
5. Functional diagram



6. Pinning information

6.1 Pinning





6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description	
	TSSOP5 and X2SON5	XSON6	
В	1	1	data input
A	2	2	data input
GND	3	3	ground (0 V)
Υ	4	4	data output
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table[1]

Inputs		Outputs
Α	В	Υ
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

^[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

			_		10	,
Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
VI	input voltage		[1]	-0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
Vo	output voltage	Active mode	[1][2]	-0.5	V _{CC} + 0.5	V
		Power-down mode	[1][2]	-0.5	+6.5	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$		-	±50	mA
I _{CC}	supply current			-	+100	mA
I _{GND}	ground current			-100	-	mA
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[3]	-	250	mW
T _{stg}	storage temperature			-65	+150	°C

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] When $V_{CC} = 0 \text{ V}$ (Power-down mode), the output voltage can be 5.5 V in normal operation.

^[3] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K. For XSON6 and X2SON5 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.65	-	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	Active mode	0	-	V_{CC}	V
		V _{CC} = 0 V; Power-down mode	0	-	5.5	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V _{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °	C to +8	5 °C	-40 °C to	Unit	
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	٧
	input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	٧
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	٧
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	٧
V_{IL}	LOW-level	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	٧
	input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	٧
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	٧
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	٧
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	$I_O = -100 \mu A;$ $V_{CC} = 1.65 V \text{ to } 5.5 V$	V _{CC} - 0.1	-	-	V _{CC} – 0.1	-	V
		$I_O = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	0.95	-	٧
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9	-	-	1.7	-	٧
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	1.9	-	٧
		$I_{O} = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.3	-	-	2.0	-	٧
		$I_{O} = -32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.8	-	-	3.4	-	٧
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	$I_O = 100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.70	٧
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.3	-	0.45	٧
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.80	٧
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	-	0.80	٧
lı	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	μА

Table 7. Static characteristics ... continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °	C to +85	5 °C	–40 °C to	Unit	
			Min	Typ[1]	Max	Min	Max	
I _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 5.5 \text{ V}$	-	±0.1	±2	-	±2	μА
I _{CC}	supply current	$V_I = 5.5 \text{ V or GND}; I_O = 0 \text{ A};$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	0.1	4	-	4	μА
Δl _{CC}	additional supply current	$V_{CC} = 2.3 \text{ V to } 5.5 \text{ V};$ $V_1 = V_{CC} - 0.6 \text{ V};$ $I_O = 0 \text{ A};$ per pin	-	5	500	-	500	μА
Cı	input capacitance	$V_{CC} = 3.3 \text{ V}; V_I = \text{GND to } V_{CC}$	-	5	-	-	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for load circuit see Figure 9.

Symbol	Parameter	Conditions	-40	°C to +85	°C	-40 °C to	Unit	
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	A, B to Y; see Figure 8						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.2	8.0	1.0	10.5	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.2	5.5	0.5	7.0	ns
		V _{CC} = 2.7 V	0.5	2.5	5.5	0.5	7.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.1	4.5	0.5	6.0	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.7	4.0	0.5	5.5	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC};$ [3] $V_{CC} = 3.3 \text{ V}$	-	14	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \sum (C_L \times V_{CC}{}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

 $f_o = output frequency in MHz;$

C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}{}^2 \times f_o) = sum \ of \ outputs.$

12. Waveforms

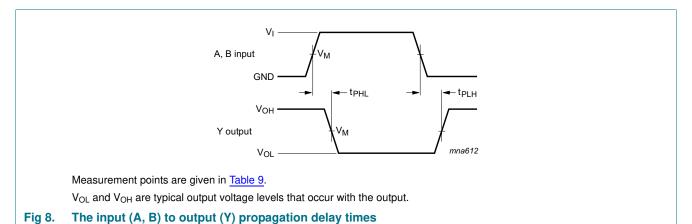
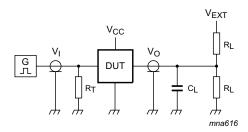


 Table 9.
 Measurement points

Supply voltage	Input	Output
V _{CC}	V _M	V _M
1.65 V to 1.95 V	0.5V _{CC}	0.5V _{CC}
2.3 V to 2.7 V	0.5V _{CC}	0.5V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5V _{CC}	0.5V _{CC}

Nexperia 74LVC1G02

Single 2-input NOR gate



Test data is given in Table 10.

Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 9. Test circuit for measuring switching times

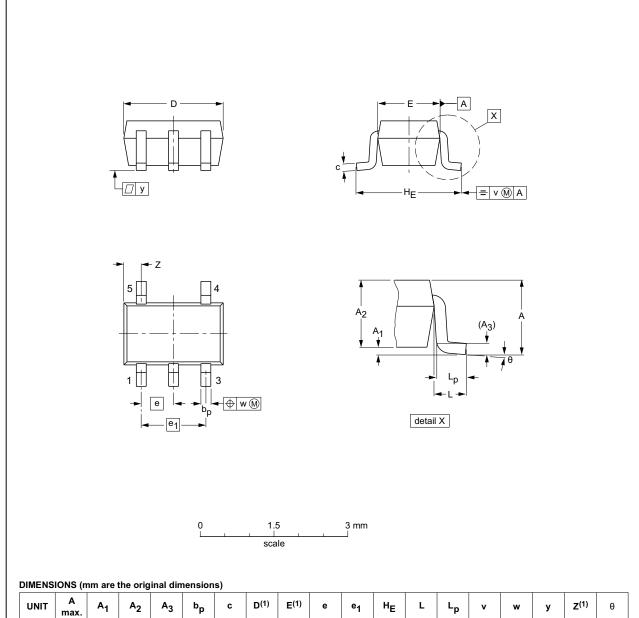
Table 10. Test data

Supply voltage	Input L		Load	V _{EXT}	
V _{CC}	V_{l} $t_{r} = t_{f}$		C _L	R _L	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



UNIT	A max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E(1)	е	e ₁	HE	L	Lp	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN	ISSUE DATE	
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT353-1		MO-203	SC-88A			00-09-01 03-02-19
	•			•		

Fig 10. Package outline SOT353-1 (TSSOP5)

74LVC1G0

Plastic surface-mounted package; 5 leads

SOT753

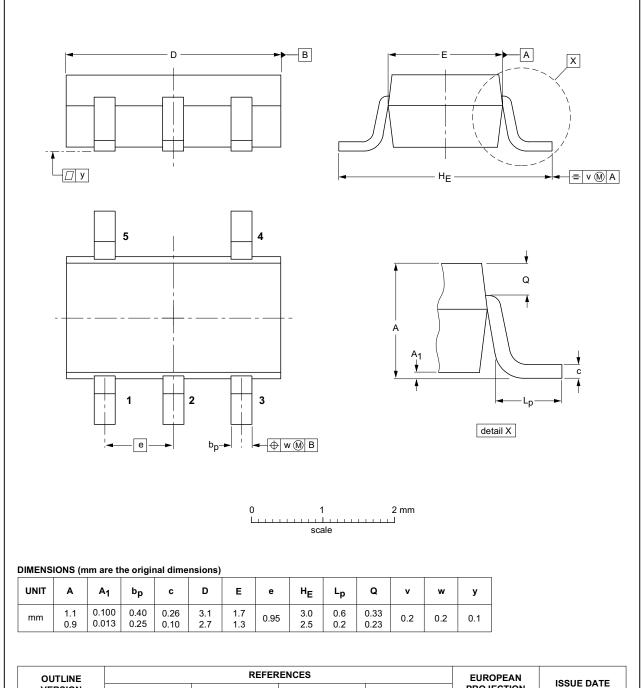


Fig 11. Package outline SOT753 (SC-74A)

IEC

74LVC1G02

JEITA

SC-74A

JEDEC

02-04-16

06-03-16

PROJECTION

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VERSION

SOT753

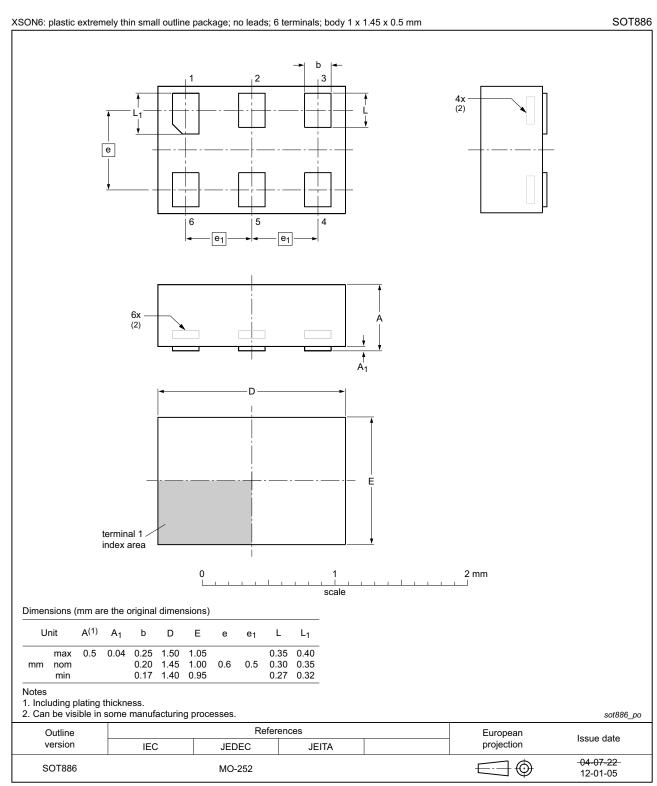


Fig 12. Package outline SOT886 (XSON6)

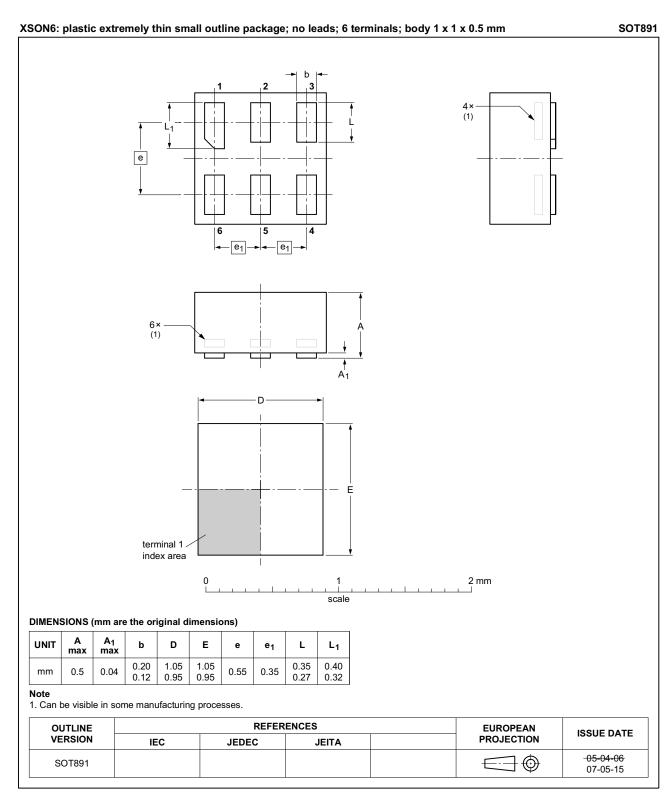


Fig 13. Package outline SOT891 (XSON6)

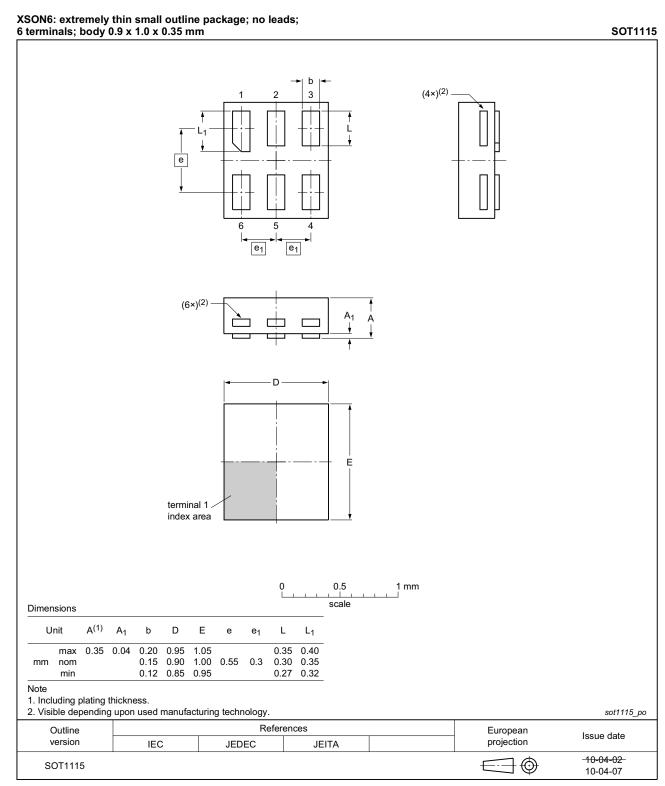


Fig 14. Package outline SOT1115 (XSON6)

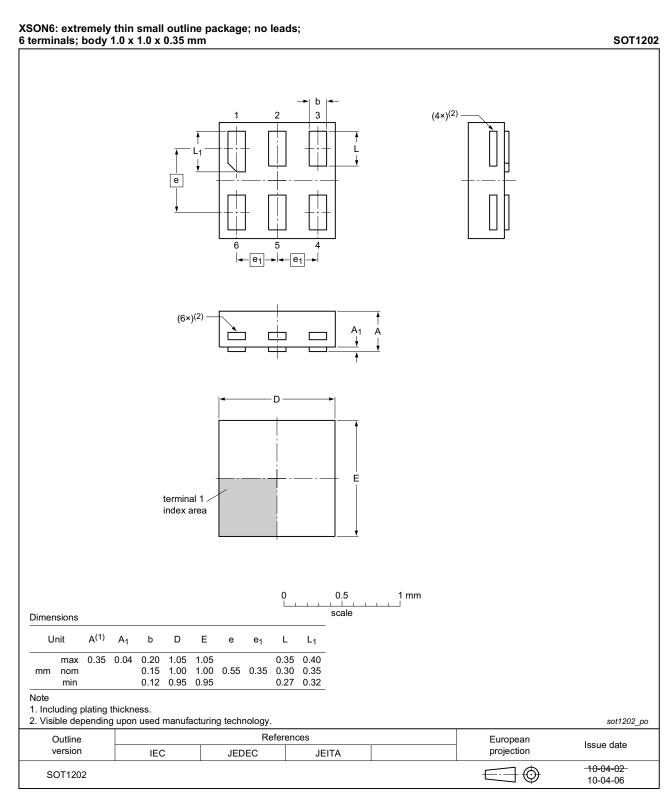


Fig 15. Package outline SOT1202 (XSON6)

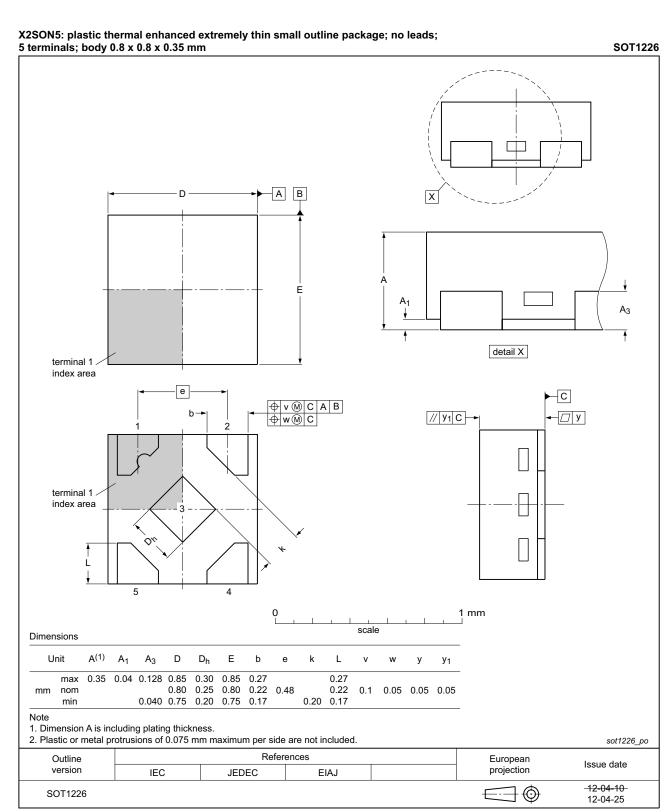


Fig 16. Package outline SOT1226 (X2SON5)

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14. Abbreviations

Table 11. Abbreviations

Acronym	Description	
CMOS	Complementary Metal Oxide Semiconductor	
DUT	Device Under Test	
ESD	ElectroStatic Discharge	
HBM	Human Body Model	
MM	Machine Model	
TTL	Transistor-Transistor Logic	

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G02 v.12	20161129	Product data sheet	-	74LVC1G02 v.11
Modifications:	• <u>Table 7</u> : The	maximum limits for leakage	e current and supply cu	irrent have changed.
74LVC1G02 v.11	20120629	Product data sheet	-	74LVC1G02 v.10
Modifications:	Added type	number 74LVC1G02GX (SC)T1226)	
74LVC1G02 v.10	20120305	Product data sheet	-	74LVC1G02 v.9
Modifications:	Package ou	tline drawing of SOT886 (Fig	gure 12) modified.	
74LVC1G02 v.9	20111209	Product data sheet	-	74LVC1G02 v.8
Modifications:	 Legal pages 	updated.		
74LVC1G02 v.8	20101020	Product data sheet	-	74LVC1G02 v.7
74LVC1G02 v.7	20070718	Product data sheet	-	74LVC1G02 v.6
74LVC1G02 v.6	20060914	Product data sheet	-	74LVC1G02 v.5
74LVC1G02 v.5	20040907	Product specification	-	74LVC1G02 v.4
74LVC1G02 v.4	20021002	Product specification	-	74LVC1G02 v.3
74LVC1G02 v.3	20020515	Product specification	-	74LVC1G02 v.2
74LVC1G02 v.2	20010411	Product specification	-	74LVC1G02 v.1
74LVC1G02 v.1	20001114	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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74LVC1G02

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Nexperia 74LVC1G02

Single 2-input NOR gate

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Single 2-input NOR gate

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