

## ADG781/ADG782/ADG783

### FEATURES

**1.8 V to 5.5 V Single Supply**  
**Low On Resistance (2.5  $\Omega$  Typ)**  
**Low On-Resistance Flatness (0.5  $\Omega$ )**  
**-3 dB Bandwidth > 200 MHz**  
**Rail-to-Rail Operation**  
**20-Lead 4 mm  $\times$  4 mm Chip Scale Package**  
**Fast Switching Times**  
 $t_{ON} = 16$  ns  
 $t_{OFF} = 10$  ns  
**Typical Power Consumption (< 0.01  $\mu$ W)**  
**TTL/CMOS Compatible**  
**For Functionally Equivalent Devices in 16-Lead TSSOP  
and SOIC Packages, See ADG711/ADG712/ADG713**

### APPLICATIONS

**Battery Powered Systems**  
**Communication Systems**  
**Sample Hold Systems**  
**Audio Signal Routing**  
**Video Switching**  
**Mechanical Reed Relay Replacement**

### GENERAL DESCRIPTION

The ADG781, ADG782, and ADG783 are monolithic CMOS devices containing four independently selectable switches. These switches are designed on an advanced submicron process that provides low power dissipation and high switching speed, low on resistance, low leakage currents and high bandwidth.

They are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery powered instruments and with the new generation of DACs and ADCs from Analog Devices. Fast switching times and high bandwidth make the part suitable for video signal switching.

The ADG781, ADG782, and ADG783 contain four independent single-pole/single throw (SPST) switches. The ADG781 and ADG782 differ only in that the digital control logic is inverted. The ADG781 switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the ADG782. The ADG783 contains two switches whose digital control logic is similar to the ADG781, while the logic is inverted on the other two switches.

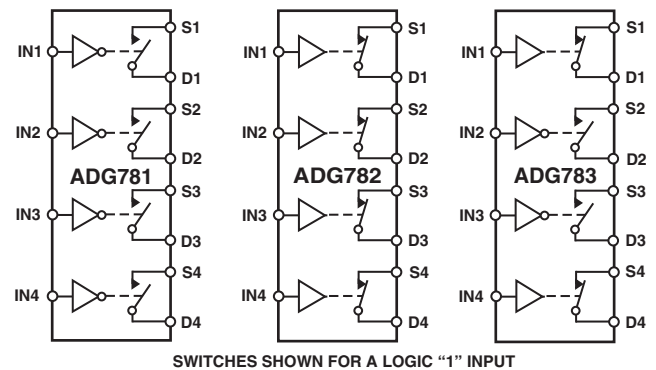
Each switch conducts equally well in both directions when ON. The ADG783 exhibits break-before-make switching action.

The ADG781/ADG782/ADG783 are available in 20-lead chip scale packages.

### REV.C

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### FUNCTIONAL BLOCK DIAGRAMS



### PRODUCT HIGHLIGHTS

- 20-Lead 4 mm  $\times$  4 mm Chip Scale Package (CSP).
- 1.8 V to 5.5 V Single Supply Operation. The ADG781, ADG782, and ADG783 offer high performance and are fully specified and guaranteed with 3 V and 5 V supply rails.
- Very Low  $R_{ON}$  (4.5  $\Omega$  max at 5 V, 8  $\Omega$  max at 3 V). At supply voltage of 1.8 V,  $R_{ON}$  is typically 35  $\Omega$  over the temperature range.
- Low On-Resistance Flatness.
- 3 dB Bandwidth >200 MHz.
- Low Power Dissipation. CMOS construction ensures low power dissipation.
- Fast  $t_{ON}/t_{OFF}$ .
- Break-Before-Make Switching. This prevents channel shorting when the switches are configured as a multiplexer (ADG783 only).

# ADG781/ADG782/ADG783—SPECIFICATIONS

( $V_{DD} = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ . All specifications  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	2.5		$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = -10\text{ mA}$ ; Test Circuit 1
	4		$\Omega$ max	
On-Resistance Match Between Channels ( $\Delta R_{ON}$ )		0.05	$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = -10\text{ mA}$
		0.4	$\Omega$ max	
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.5		$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = -10\text{ mA}$
		1.0	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		nA typ	$V_{DD} = 5.5\text{ V}$ ; $V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2
	$\pm 0.1$	$\pm 0.2$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$		nA typ	$V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; Test Circuit 2
	$\pm 0.1$	$\pm 0.2$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		nA typ	$V_S = V_D = 1\text{ V}$ , or $4.5\text{ V}$ ; Test Circuit 3
	$\pm 0.1$	$\pm 0.2$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	11		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3\text{ V}$ ; Test Circuit 4
		16	ns max	
$t_{OFF}$	6		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3\text{ V}$ ; Test Circuit 4
		10	ns max	
Break-Before-Make Time Delay, $t_D$ (ADG783 Only)	6		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3\text{ V}$ ; Test Circuit 5
		1	ns min	
Charge Injection	3		pC typ	$V_S = 2\text{ V}$ ; $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 6
Off Isolation	-58		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-78		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
Channel-to-Channel Crosstalk	-90		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ ; Test Circuit 8
Bandwidth -3 dB	200		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 9
$C_S$ (OFF)	10		pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	10		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	22		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
		1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SPECIFICATIONS<sup>1</sup>(V<sub>DD</sub> = 3 V ±10%, GND = 0 V. All specifications –40°C to +85°C unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	–40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to V <sub>DD</sub>	V	
On Resistance (R <sub>ON</sub> )	5	5.5	Ω typ	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>S</sub> = –10 mA;
		10	Ω max	Test Circuit 1
On-Resistance Match Between Channels (ΔR <sub>ON</sub> )	0.1	0.5	Ω typ	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>S</sub> = –10 mA
On-Resistance Flatness (R <sub>FLAT(ON)</sub> )		2.5	Ω typ	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>S</sub> = –10 mA
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage I <sub>S</sub> (OFF)	±0.01		nA typ	V <sub>DD</sub> = 3.3 V;
	±0.1	±0.2	nA max	V <sub>S</sub> = 3 V/1 V, V <sub>D</sub> = 1 V/3 V;
Drain OFF Leakage I <sub>D</sub> (OFF)	±0.01		nA typ	Test Circuit 2
	±0.1	±0.2	nA max	V <sub>S</sub> = 3 V/1 V, V <sub>D</sub> = 1 V/3 V;
Channel ON Leakage I <sub>D</sub> , I <sub>S</sub> (ON)	±0.01		nA typ	Test Circuit 2
	±0.1	±0.2	nA max	V <sub>S</sub> = V <sub>D</sub> = 1 V, or 3 V;
				Test Circuit 3
<b>DIGITAL INPUTS</b>				
Input High Voltage, V <sub>INH</sub>		2.0	V min	
Input Low Voltage, V <sub>INL</sub>		0.8	V max	
Input Current				
I <sub>INL</sub> or I <sub>INH</sub>	0.005		μA typ	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
		±0.1	μA max	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
t <sub>ON</sub>	13		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,
		20	ns max	V <sub>S</sub> = 2 V; Test Circuit 4
t <sub>OFF</sub>	7		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,
		12	ns max	V <sub>S</sub> = 2 V; Test Circuit 4
Break-Before-Make Time Delay, t <sub>D</sub> (ADG783 Only)	7		ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF,
Charge Injection	3	1	ns min	V <sub>S1</sub> = V <sub>S2</sub> = 2 V; Test Circuit 5
			pC typ	V <sub>S</sub> = 1.5 V; R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF;
				Test Circuit 6
Off Isolation	–58		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 10 MHz
	–78		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz;
				Test Circuit 7
Channel-to-Channel Crosstalk	–90		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 10 MHz;
				Test Circuit 8
Bandwidth –3 dB	200		MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF; Test Circuit 9
C <sub>S</sub> (OFF)	10		pF typ	f = 1 MHz
C <sub>D</sub> (OFF)	10		pF typ	f = 1 MHz
C <sub>D</sub> , C <sub>S</sub> (ON)	22		pF typ	f = 1 MHz
<b>POWER REQUIREMENTS</b>				
I <sub>DD</sub>	0.001		μA typ	V <sub>DD</sub> = 3.3 V
		1.0	μA max	Digital Inputs = 0 V or 3.3 V

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version: –40°C to +85°C.<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG781/ADG782/ADG783

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = 25°C unless otherwise noted.)

V <sub>DD</sub> to GND	-0.3 V to +6 V
Analog, Digital Inputs <sup>2</sup>	-0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Chip Scale Package	
θ <sub>JA</sub> Thermal Impedance	32°C/W

Lead Temperature, Soldering (10 sec)	300°C
IR Reflow (<20 sec)	235°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

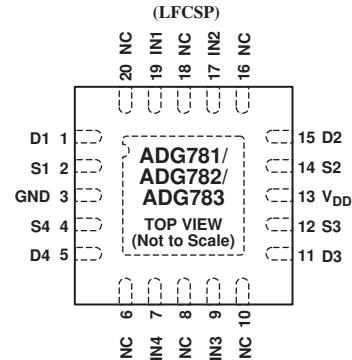
Table I. Truth Table (ADG781/ADG782)

ADG781 In	ADG782 In	Switch Condition
0	1	ON
1	0	OFF

Table II. Truth Table (ADG783)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

## PIN CONFIGURATION



- NOTES  
 1. NC = NO CONNECT.  
 2. EXPOSED PAD TIED TO SUBSTRATE, GND.

## CAUTION

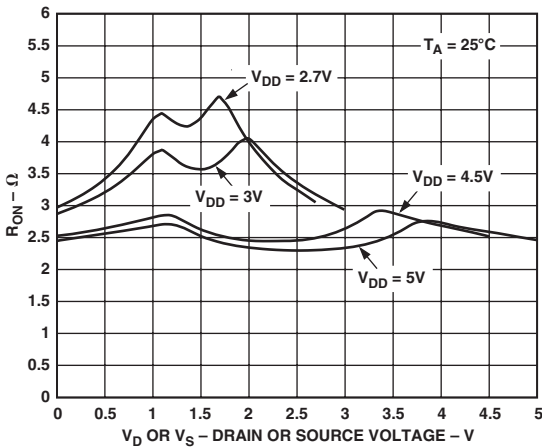
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG781/ADG782/ADG783 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



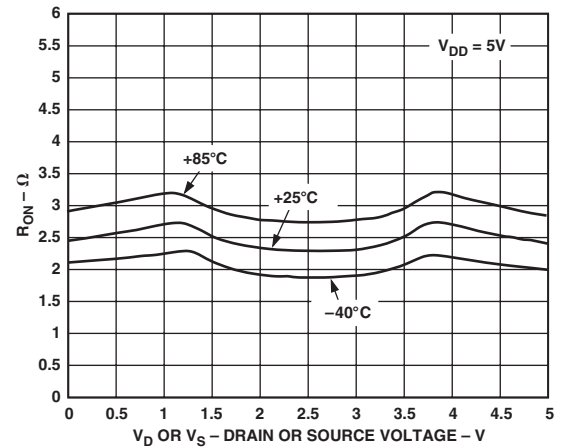
## TERMINOLOGY

$V_{DD}$	Most positive power supply potential.	$C_D, C_S$ (ON)	“ON” switch capacitance.
GND	Ground (0 V) reference.	$t_{ON}$	Delay between applying the digital control input and the output switching on.
S	Source terminal. May be an input or output.	$t_{OFF}$	Delay between applying the digital control input and the output switching off.
D	Drain terminal. May be an input or output.	$t_D$	“OFF” time or “ON” time measured between the 90% points of both switches, when switching from one address state to another (ADG783 only).
IN	Logic control input.	Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
$R_{ON}$	Ohmic resistance between D and S.	Off Isolation	A measure of unwanted signal coupling through an “OFF” switch.
$\Delta R_{ON}$	On-resistance match between any two channels (i.e., $R_{ON}$ max and $R_{ON}$ min).	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.	On Response	The frequency response of the “ON” switch.
$I_S$ (OFF)	Source leakage current with the switch “OFF.”	On Loss	The loss due to the on resistance of the switch.
$I_D$ (OFF)	Drain leakage current with the switch “OFF.”		
$I_D, I_S$ (ON)	Channel leakage current with the switch “ON.”		
$V_D$ ( $V_S$ )	Analog voltage on terminals D, S.		
$C_S$ (OFF)	“OFF” switch source capacitance.		
$C_D$ (OFF)	“OFF” switch drain capacitance.		

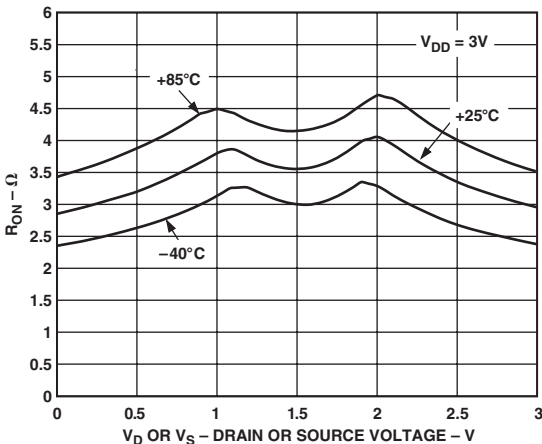
## Typical Performance Characteristics



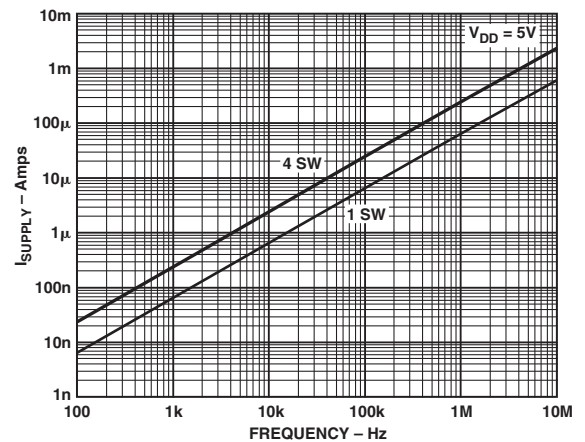
TPC 1. On Resistance as a Function of  $V_D$  ( $V_S$ )



TPC 3. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures  $V_{DD} = 5V$

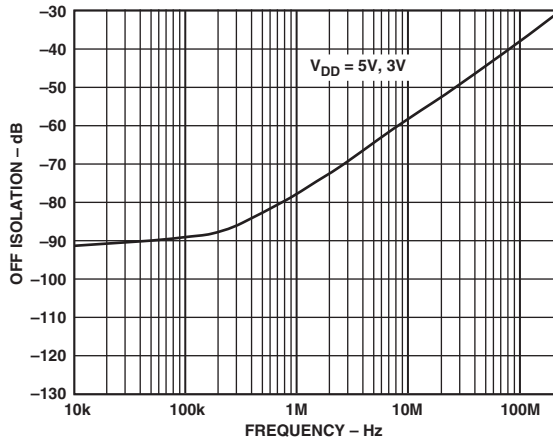


TPC 2. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures  $V_{DD} = 3V$

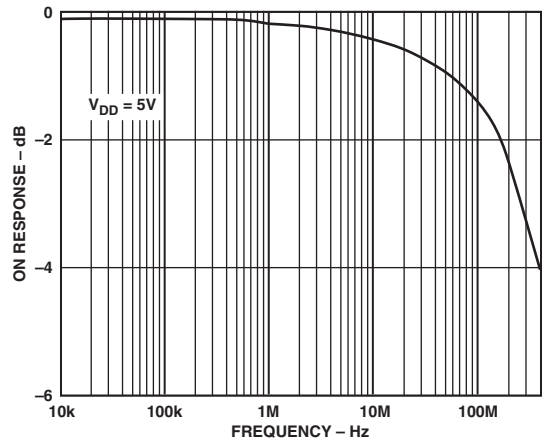


TPC 4. Supply Current vs. Input Switching Frequency

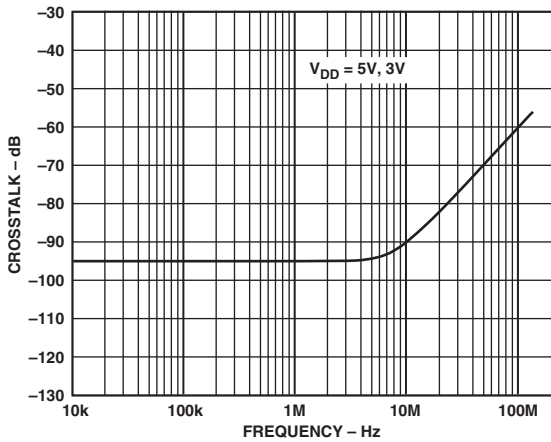
# ADG781/ADG782/ADG783



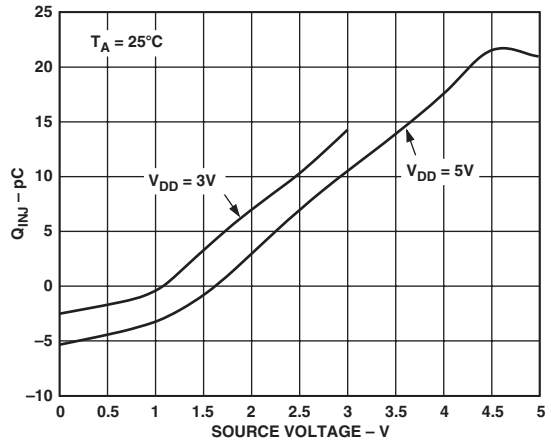
TPC 5. Off Isolation vs. Frequency



TPC 7. On Response vs. Frequency



TPC 6. Crosstalk vs. Frequency



TPC 8. Charge Injection vs. Source Voltage

## APPLICATIONS

Figure 1 illustrates a photodetector circuit with programmable gain. An AD820 is used as the output operational amplifier. With the resistor values shown in the circuit, and using different combinations of the switches, gain in the range of 2 to 16 can be achieved.

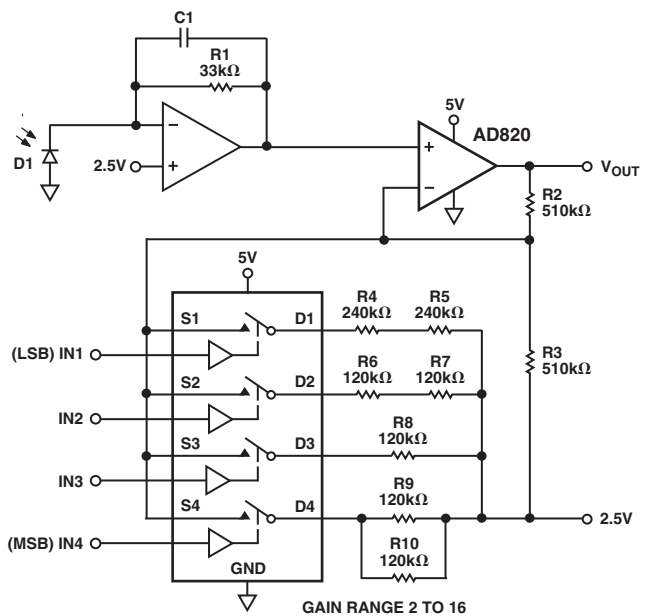
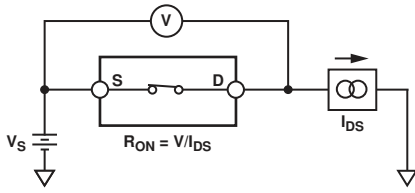
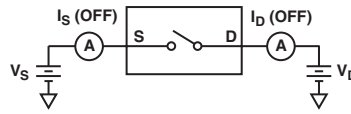


Figure 1. Photodetector Circuit with Programmable Gain

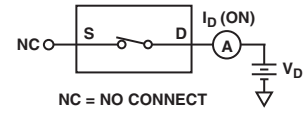
Test Circuits



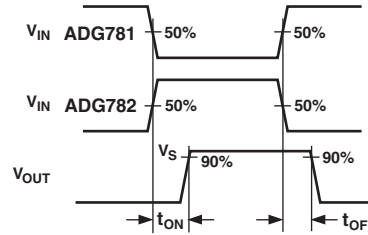
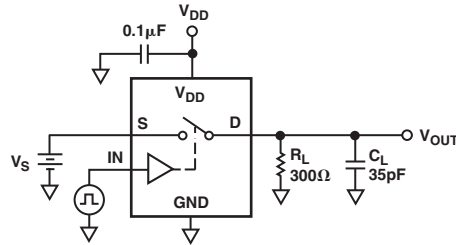
Test Circuit 1. On Resistance



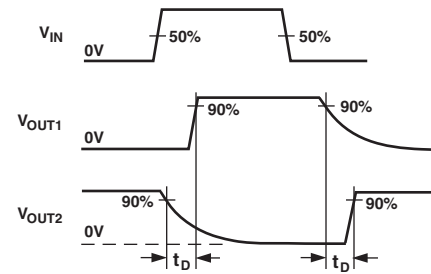
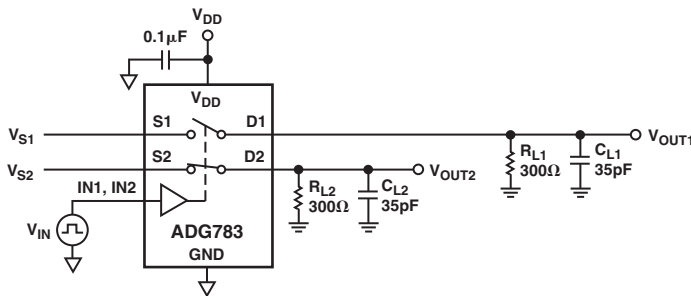
Test Circuit 2. Off Leakage



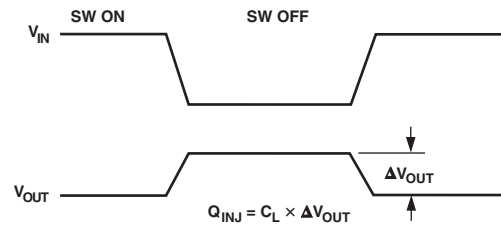
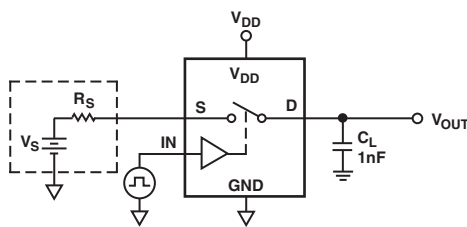
Test Circuit 3. On Leakage



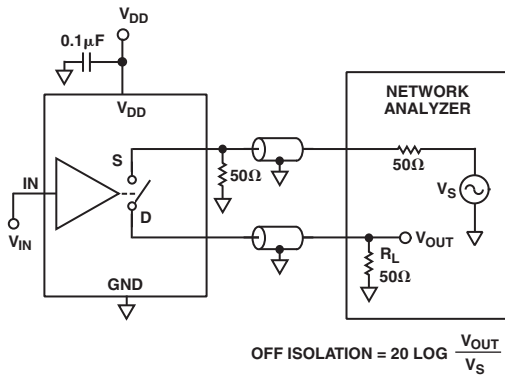
Test Circuit 4. Switching Times



Test Circuit 5. Break-Before-Make Time Delay,  $t_D$

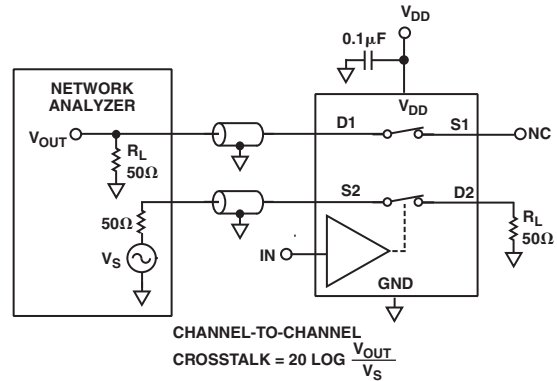


Test Circuit 6. Charge Injection



$$\text{OFF ISOLATION} = 20 \text{ LOG } \frac{V_{\text{OUT}}}{V_S}$$

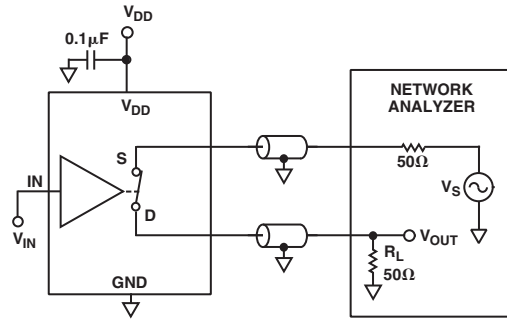
Test Circuit 7. Off Isolation



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \text{ LOG } \frac{V_{\text{OUT}}}{V_S}$$

Test Circuit 8. Channel-to-Channel Crosstalk

# ADG781/ADG782/ADG783

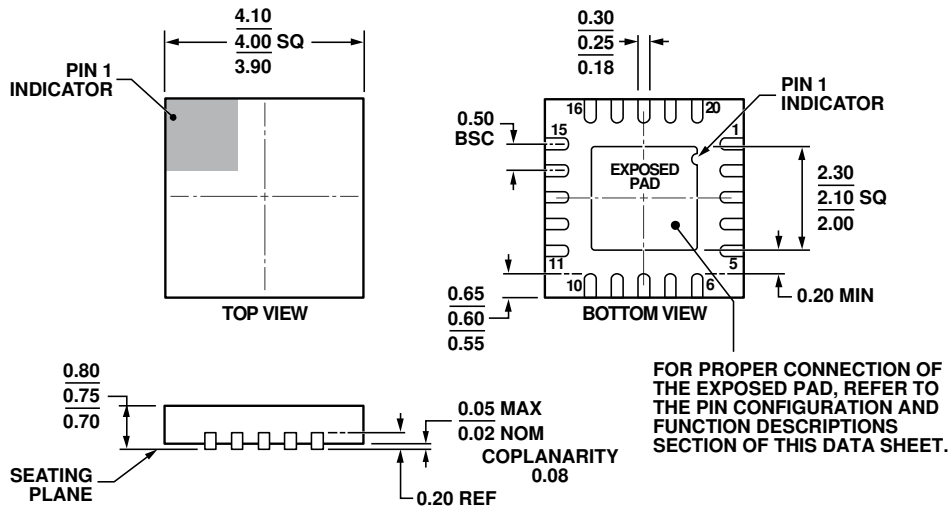


$$\text{INSERTION LOSS} = 20 \text{ LOG} \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

*Test Circuit 9. Bandwidth*



OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 2. 20-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
 4 mm × 4 mm Body, Very Very Thin Quad  
 (CP-20-6)  
 Dimensions shown in millimeters

08-16-2010-B

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG781BCPZ	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG781BCPZ-REEL7	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG782BCPZ	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG782BCPZ-REEL7	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG783BCPZ	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG783BCPZ-REEL	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADG783BCPZ-REEL7	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6

<sup>1</sup> Z = RoHS Compliant Part.

REVISION HISTORY

2/13—Rev. B to Rev. C

- Changed Pin 4 from S3 to S4 .....4
- Changes to Test Circuit 1 .....7
- Changes to Ordering Guide.....9

8/12—Rev. A to Rev. B

- Updated Outline Dimensions.....9
- Changes to Ordering Guide.....9

3/02—Rev. 0 to Rev. A

- Edits to Typical Performance Characteristics .....5-6
- Changes to OUTLINE DIMENSIONS drawing .....8