

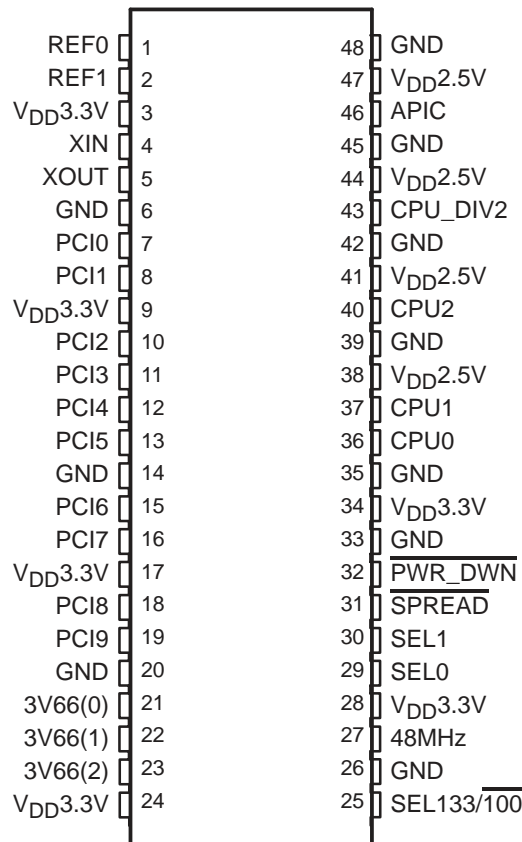
# CDC922

## 133-MHz CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS WITH 3-STATE OUTPUTS

SCAS634—JULY 28, 1999

- Generates Clocks for Pentium™ III Class Microprocessors
- Supports a Single Pentium III Microprocessor
- Uses a 14.318 MHz Crystal Input to Generate Multiple Output Frequencies
- Includes Spread Spectrum Clocking (SSC), 0.34% Downspread for Reduced EMI Performance
- Power Management Control Terminals
- Low Output Skew and Jitter for Clock Distribution
- Operates from Dual 2.5-V and 3.3-V Supplies
- Generates the Following Clocks:
  - 3 CPU (2.5 V, 100/133 MHz)
  - 10 PCI (3.3 V, 33.3 MHz)
  - 1 CPU/2 (2.5 V, 50/66 MHz)
  - 1 APIC (2.5 V, 16.67 MHz)
  - 3 3V66 (3.3 V, 66 MHz)
  - 2 REF (3.3 V, 14.318 MHz)
  - 1 48MHz (3.3 V, 48 MHz)
- Packaged in 48-Pin SSOP Package
- Designed for Use with TI's Direct Rambus™ Clock Generators (CDCR81, CDCR82, CDCR83)

DL PACKAGE  
(TOP VIEW)



### description

The CDC922 is a clock synthesizer/driver that generates CPU, CPU\_DIV2, 3V66, PCI, APIC, 48MHz, and REF system clock signals to support computer systems with a single Pentium III class microprocessor.

All output frequencies are generated from a 14.318-MHz crystal input. Instead of a crystal, a reference clock input can be provided at the XIN input. Two phase-locked loops (PLLs) are used to generate the host frequencies and the 48-MHz clock frequency. On-chip loop filters and internal feedback eliminate the need for external components.

The host and PCI clock outputs provide low-skew and low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected via control inputs SEL0, SEL1, and SEL133/ $\overline{100}$ .

The 48MHz clock can be independently disabled via the control inputs SEL0, SEL1, and SEL133/ $\overline{100}$ . In this state, the 48-MHz PLL is disabled and the 48MHz clock is driven to high impedance to reduce component jitter.

The outputs are either 3.3-V or 2.5-V single-ended CMOS buffers. With a logic high-level on the  $\overline{\text{PWR\_DWN}}$  terminal, the device operates normally, but when a logical low-level input is applied, the device powers down completely with the outputs in a low-level output state.



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# CDC922

## 133-MHz CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS

### WITH 3-STATE OUTPUTS

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#### description (continued)

The CPU bus can operate at 100 MHz or 133 MHz. Output frequency selection is done with corresponding setting for SEL133/100 control input. The PCI bus frequency is fixed to 33 MHz.

Since the CDC922 is based on PLL circuitry, it requires a stabilization time to achieve phase lock of the PLL. This stabilization time is required after power up or after changes to the SEL inputs are made. With use of an external reference clock, this signal must be fixed-frequency and fixed-phase before the stabilization time starts.

#### Function Tables

##### SELECT FUNCTIONS

INPUTS			OUTPUTS							FUNCTION
SEL133/ 100	SEL1	SEL0	CPU	CPU_DIV2	3V66	PCI	48MHz	REF	APIC	
L	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	3-state
L	L	H	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
L	H	L	100 MHz	50 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	48-MHz PLL off
L	H	H	100 MHz	50 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	48-MHz PLL on
H	L	L	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16	Test
H	L	H	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
H	H	L	133 MHz	66 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	48-MHz PLL off
H	H	H	133 MHz	66 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	48-MHz PLL on

##### ENABLE FUNCTIONS

INPUTS	OUTPUTS						INTERNAL	
PWR_DWN	CPU	CPU_DIV2	APIC	3V66	PCI	REF, 48MHz	CRYSTAL	VCOs
L	L	L	L	L	L	L	Off	Off
H	On	On	On	On	On	On	On	On

##### OUTPUT BUFFER SPECIFICATIONS

BUFFER NAME	V <sub>DD</sub> RANGE (V)	IMPEDANCE (Ω)	BUFFER TYPE
CPU, CPU_DIV2, APIC	2.375 – 2.625	13.5 – 45	TYPE 1
48MHz, REF	3.135 – 3.465	20 – 60	TYPE 3
PCI, 3V66	3.135 – 3.465	12 – 55	TYPE 5

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**Terminal Functions**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
3V66 [0–2]	21–23	O	3.3 V, Type 5, 66-MHz clock outputs
48MHz	27	O	3.3 V, Type 3, 48-MHz clock output
APIC	46	O	2.5 V, Type 2, APIC clock output at 16.67 MHz
CPU [0–2]	36, 37, 40	O	2.5 V, Type 1, CPU clock outputs
CPU_DIV2	43	O	2.5 V, Type 1, CPU_DIV2 clock output
GND	6, 14, 20, 26, 33, 35, 39, 42, 45, 48		Ground for PCI, 3V66, 48MHz, CPU, CPU_DIV2, APIC, REF [0–1] outputs and CORE
PCI [0–9]	7, 8, 10–13, 15, 16, 18, 19	O	3.3 V, Type 5, 33-MHz PCI clock outputs
PWR_DWN	32	I	Power down for complete device with outputs forced low
REF0, REF1	1, 2	O	3.3 V, Type 3, 14.318-MHz reference clock outputs
SEL0, SEL1	29, 30	I	LVTTL level logic select terminals for function selection
SEL133/100	25	I	LVTTL level logic select terminal for enabling 100/133 MHz
SPREAD	31	I	Disables SSC function
V <sub>DD</sub> 2.5V	38, 41, 44, 47		Power for CPU, CPU_DIV2, and APIC outputs
V <sub>DD</sub> 3.3V	3, 9, 17, 24, 28, 34		Power for the REF, PCI, 3V66, 48MHz outputs and CORE
XIN	4	I	Crystal input – 14.318 MHz
XOUT	5	O	Crystal output – 14.318 MHz

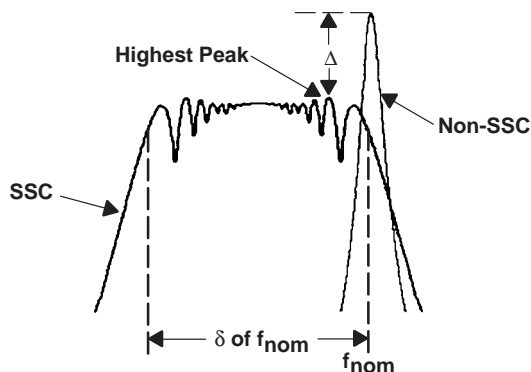


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## spread spectrum clock (SSC) implementation for CDC922

Simultaneously switching at fixed frequency generates a significant power peak at the selected frequency, which in turn will cause EMI disturbance to the environment. The purpose of the internal frequency modulation of the CPU-PLL allows to distribute the energy to many different frequencies which reduces the power peak. A typical characteristic for a single frequency spectrum and a frequency modulated spectrum is shown in Figure 1.

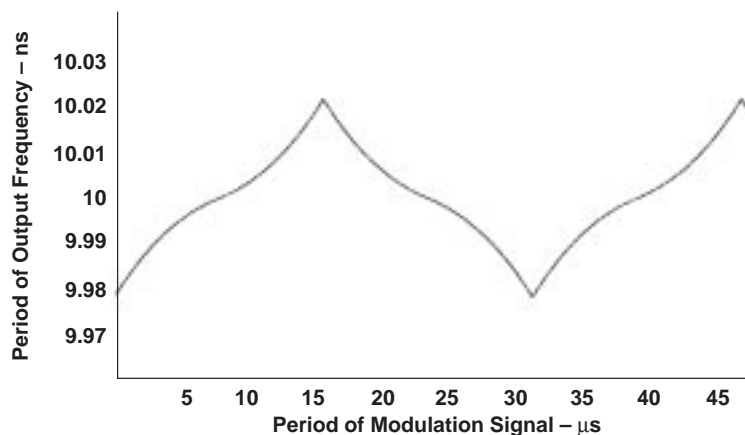


**Figure 1.** Frequency Power Spectrum With and Without the Use of SSC

The modulated spectrum has its distribution left hand to the single frequency spectrum which indicates a “down-spread modulation”.

The peak reduction depends on the modulation scheme and modulation profile. System performance and timing requirements are the limiting factors for actual design implementations. The implementation was driven to keep the average clock frequency closed to its upper specification limit. The modulation amount was set to approximately  $-0.34\%$  (compared to  $-0.5\%$  on the CDC921).

In order to allow a downstream PLL to follow the frequency modulated signal, the bandwidth of the modulation signal is limited in order to minimize SSC induced tracking skew jitter. The ideal modulation profile used for CDC922 is shown in Figure 2.

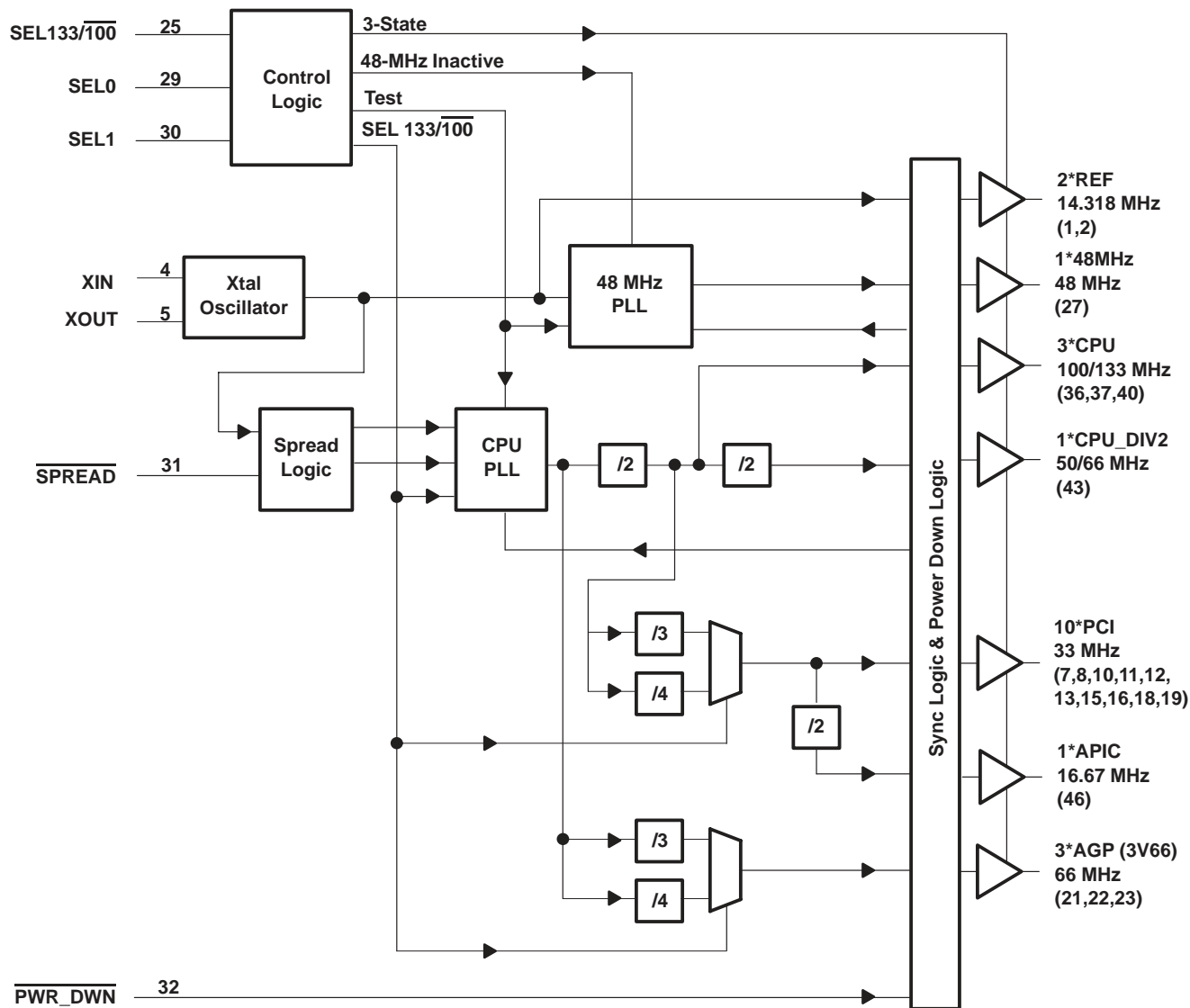


**Figure 2.** SSC Modulation Profile

# CDC922 133-MHz CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS WITH 3-STATE OUTPUTS

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## functional block diagram



# CDC922

## 133-MHz CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{DD}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance state or power-off state, $V_O$ (see Note 1)	–0.5 V to $V_{DD} + 0.5$ V
Current into any output in the low state, $I_O$	$2 \times I_{OL}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Operating free-air temperature range, $T_A$	–0°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATNG	DERATING FACTORT ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DL	1315.7 mW	10.53 mW/°C	842.1 mW	684.2 mW

† This is the inverse of the traditional junction-to-case thermal resistance ( $R_{\theta JA}$ ) and uses a board-mounted device at 95°C/W.

#### recommended operating conditions (see Note 2)

		MIN	NOM†	MAX	UNIT
Supply voltage, $V_{DD}$	3.3 V	3.135		3.465	V
	2.5 V	2.375		2.625	
High-level input voltage, $V_{IH}$		2		$V_{DD} + 0.3$ V	V
Low-level input voltage, $V_{IL}$		GND – 0.3 V		0.8	V
Input voltage, $V_I$		0		$V_{DD}$	V
High-level output current, $I_{OH}$	CPUx, CPU_DIV2			–12	mA
	APIC			–12	
	48MHz, REFx			–14	
	PCIx, PCI_F, 3V66x			–18	
Low-level output current, $I_{OL}$	CPUx, CPU_DIV2			12	mA
	APIC			12	
	48MHz, REFx			9	
	PCIx, PCI_F, 3V66x			12	
Reference frequency, $f_{(XTAL)}^\ddagger$	Test mode		130		MHz
Crystal frequency, $f_{(XTAL)}^\S$	Normal mode	13.8	14.318	14.8	MHz
Operating free-air temperature, $T_A$		0		85	°C

NOTE 2: Unused inputs must be held high or low to prevent them from floating.

† All nominal values are measured at their respective nominal  $V_{DD}$  values.

‡ Reference frequency is a test clock driven on the XIN input during the device test mode and normal mode. In test mode, XIN can be driven externally up to  $f_{(XTAL)} = 130$  MHz. If XIN is driven externally, XOUT is floating.

§ This is a series fundamental crystal with  $f_O = 14.31818$  MHz.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$	Input clamp voltage	$V_{DD} = 3.135\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V
$R_I$	Input resistance	XIN, XOUT $V_{DD} = 3.465\text{ V}$ , $V_I = V_{DD} - 0.5\text{ V}$	80		350	k $\Omega$
$I_{IH}$	High-level input current	XOUT $V_{DD} = 3.135\text{ V}$ , $V_I = V_{DD} - 0.5\text{ V}$		20	50	mA
		$\overline{\text{SEL0, SEL1, SPREAD}}$ $V_{DD} = 3.465\text{ V}$ , $V_I = V_{DD}$		<10	10	$\mu\text{A}$
		$\overline{\text{PWR\_DWN}}$ $V_{DD} = 3.465\text{ V}$ , $V_I = V_{DD}$		<10	10	$\mu\text{A}$
		$\overline{\text{SEL133/100}}$ $V_{DD} = 3.465\text{ V}$ , $V_I = V_{DD}$		<10	10	$\mu\text{A}$
$I_{IL}$	Low-level input current	XOUT $V_{DD} = 3.135\text{ V}$ , $V_I = 0\text{ V}$		-2	-5	mA
		$\overline{\text{SEL0, SEL1, SPREAD}}$ $V_{DD} = 3.465\text{ V}$ , $V_I = \text{GND}$		<10	-10	$\mu\text{A}$
		$\overline{\text{PWR\_DWN}}$ $V_{DD} = 3.465\text{ V}$ , $V_I = \text{GND}$		<10	-10	$\mu\text{A}$
		$\overline{\text{SEL133/100}}$ $V_{DD} = 3.465\text{ V}$ , $V_I = \text{GND}$		<10	-10	$\mu\text{A}$
$I_{OZ}$	High-impedance-state output current	$ V_{DD}  = \text{max}$ , $V_O = V_{DD}$ or GND			$\pm 10$	$\mu\text{A}$
$I_{DD}$	Supply current	$V_{DD} = 2.625\text{ V}$ , $\overline{\text{PWR\_DWN}} = \text{low}$ All outputs = low		<20	100	$\mu\text{A}$
		$V_{DD} = 2.625\text{ V}$ , All outputs = high		<20	100	$\mu\text{A}$
		$V_{DD} = 3.465\text{ V}$ , $\overline{\text{PWR\_DWN}} = \text{low}$ All outputs = low		<50	200	$\mu\text{A}$
		$V_{DD} = 3.465\text{ V}$ , All outputs = high		12	37	mA
$I_{DD(Z)}$	High-impedance-state supply current	$V_{DD} = 2.625\text{ V}$			1.4	mA
		$V_{DD} = 3.465\text{ V}$			30	
Dynamic $I_{DD}$		$C_L = 20\text{ pF}$ , CPU = 133 MHz	$V_{DD} = 3.465\text{ V}$	114	156	mA
			$V_{DD} = 2.625\text{ V}$	44	60	
$C_I$	Input capacitance	$V_{DD} = 3.3\text{ V}$ , $V_I = V_{DD}$ or GND	3.3		5.8	pF
	Crystal terminal capacitance	$V_{DD} = 3.3\text{ V}$ , $V_I = 0.3\text{ V}$	18	18.5	22.5	pF

† All typical values are measured at their respective nominal  $V_{DD}$  values.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

**CPUx, CPU\_DIV2, APIC (Type 1)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
VOH	High-level output voltage	VDD = min to max, IOH = -1 mA	VDD - 0.1 V			V
		VDD = 2.375 V, IOH = -12 mA	2			
VOL	Low-level output voltage	VDD = min to max, IOL = 1 mA			0.1	V
		VDD = 2.375 V, IOL = 12 mA		0.18	0.4	
IOH	High-level output current	VDD = 2.375 V, VO = 1 V	-26	-42		mA
		VDD = 2.5 V, VO = 1.25 V		-46		
		VDD = 2.625 V, VO = 2.375 V		-16	-27	
IOL	Low-level output current	VDD = 2.375 V, VO = 1.2 V	27	57		mA
		VDD = 2.5 V, VO = 1.25 V		63		
		VDD = 2.625 V, VO = 0.3 V		23	43	
CO	Output capacitance	VDD = 3.3 V, VO = VDD or GND	5.8		8.5	pF
ZO	Output impedance	High state VO = 0.5 VDD, VO/IOH	13.5	27	45	Ω
		Low state VO = 0.5 VDD, VO/IOL	13.5	20	45	

† All typical values are measured at their respective nominal VDD values.

**48MHz, REFx (Type 3)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
VOH	High-level output voltage	VDD = min to max, IOH = -1 mA	VDD - 0.1 V			V
		VDD = 3.135 V, IOH = -14 mA	2.4			
VOL	Low-level output voltage	VDD = min to max, IOL = 1 mA			0.1	V
		VDD = 3.135 V, IOL = 9 mA		0.18	0.4	
IOH	High-level output current	VDD = 3.135 V, VO = 1 V	-27	-41		mA
		VDD = 3.3 V, VO = 1.65 V		-41		
		VDD = 3.465 V, VO = 3.135 V		-12	-23	
IOL	Low-level output current	VDD = 3.135 V, VO = 1.95 V	29	50		mA
		VDD = 3.3 V, VO = 1.65 V		53		
		VDD = 3.465 V, VO = 0.4 V		20	37	
CO	Output capacitance	VDD = 3.3 V, VO = VDD or GND	4.5		7	pF
ZO	Output impedance	High state VO = 0.5 VDD, VO/IOH	20	40	60	Ω
		Low state VO = 0.5 VDD, VO/IOL	20	31	60	

† All typical values are measured at their respective nominal VDD values.





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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

### PCIx, 3V66x (Type 5)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = min to max, I <sub>OH</sub> = –1 mA	V <sub>DD</sub> – 0.1 V			V
		V <sub>DD</sub> = 3.135 V, I <sub>OH</sub> = –18 mA	2.4			
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = min to max, I <sub>OL</sub> = 1 mA			0.1	V
		V <sub>DD</sub> = 3.135 V, I <sub>OL</sub> = 12 mA		0.15	0.4	
I <sub>OH</sub>	High-level output current	V <sub>DD</sub> = 3.135 V, V <sub>O</sub> = 1 V	–33	–53		mA
		V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V		–53		
		V <sub>DD</sub> = 3.465 V, V <sub>O</sub> = 3.135 V		–16	–33	
I <sub>OL</sub>	Low-level output current	V <sub>DD</sub> = 3.135 V, V <sub>O</sub> = 1.95 V	30	67		mA
		V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V		70		
		V <sub>DD</sub> = 3.465 V, V <sub>O</sub> = 0.4 V		27	49	
C <sub>O</sub>	Output capacitance	V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = V <sub>DD</sub> or GND	4.5		7.5	pF
Z <sub>O</sub>	Output impedance	High state V <sub>O</sub> = 0.5 V <sub>DD</sub> , V <sub>O</sub> /I <sub>OH</sub>	12	31	55	Ω
		Low state V <sub>O</sub> = 0.5 V <sub>DD</sub> , V <sub>O</sub> /I <sub>OL</sub>	12	24	55	

† All typical values are measured at their respective nominal V<sub>DD</sub> values.

### switching characteristics, V<sub>DD</sub> = 3.135 V to 3.465 V, T<sub>A</sub> = 0°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overshoot/undershoot			GND – 0.7 V		V <sub>DD</sub> + 0.7 V	V
Ring back			V <sub>IL</sub> – 0.1 V		V <sub>IH</sub> + 0.1 V	V
Stabilization time, $\overline{\text{PWR\_DWN}}$ to PCIx		f(CPU) = 133 MHz		0.05	3	ms
t <sub>dis3</sub>	Disable time, $\overline{\text{PWR\_DWN}}$ to PCIx	f(CPU) = 133 MHz		50		ns
Stabilization time, $\overline{\text{PWR\_DWN}}$ to CPUx		f(CPU) = 133 MHz		0.03	3	ms
t <sub>dis4</sub>	Disable time, $\overline{\text{PWR\_DWN}}$ to CPUx	f(CPU) = 133 MHz		50		ns
Stabilization time†		After SEL1, SEL0			3	ms
		After power up			3	

† Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at X1. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics tables are not applicable. Stabilization time is defined as the time from when V<sub>DD</sub> achieves its nominal operating level until the output frequency is stable and operating within specification.

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switching characteristics,  $V_{DD} = 2.375\text{ V to }2.625\text{ V}$ ,  $T_A = 0^\circ\text{C to }85^\circ\text{C}$  (continued)

### CPUx

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{en1}$	Output enable time	SEL133/100	CPUx	$f_{(CPU)} = 100\text{ or }133\text{MHz}$		6	10	ns
$t_{dis1}$	Output disable time	SEL133/100	CPUx	$f_{(CPU)} = 100\text{ or }133\text{MHz}$		8	10	ns
$t_c$	CPU clock period†			$f_{(CPU)} = 100\text{ MHz}$	10	10.04	10.2	ns
				$f_{(CPU)} = 133\text{ MHz}$	7.5	7.53	7.7	ns
Cycle to cycle jitter				$f_{(CPU)} = 100\text{ or }133\text{MHz}$			250	ps
Duty cycle				$f_{(CPU)} = 100\text{ or }133\text{MHz}$	45	55		%
$t_{sk(o)}$	CPU bus skew	CPUx	CPUx	$f_{(CPU)} = 100\text{ or }133\text{MHz}$	50		175	ps
$t_{sk(p)}$	CPU pulse skew	CPU <sub>n</sub>	CPU <sub>n</sub>	$f_{(CPU)} = 100\text{ or }133\text{MHz}$			2.2	ns
$t_{(off)}$	CPU clock to APIC clock offset, rising edge				1.5	2.8	4	ns
$t_{(off)}$	CPU clock to 3V66 clock offset, rising edge				0	0.75	1.5	ns
$t_{w1}$	Pulse duration width, high			$f_{(CPU)} = 100\text{ MHz}$	2.6	4.3		ns
				$f_{(CPU)} = 133\text{ MHz}$	1.4	3.7		
$t_{w2}$	Pulse duration width, low			$f_{(CPU)} = 100\text{ MHz}$	2.8	4.3		ns
				$f_{(CPU)} = 133\text{ MHz}$	1.7	4		
$t_r$	Rise time			$V_O = 0.4\text{ V to }2.0\text{ V}$	0.4	1.5	2.2	ns
$t_f$	Fall time			$V_O = 0.4\text{ V to }2.0\text{ V}$	0.4	1.4	2	ns

† The average over any 1- $\mu\text{s}$  period of time is greater than the minimum specified period.

### CPU\_DIV2

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{en1}$	Output enable time	SEL133/100	CPU_DIV2	$f_{(CPU)} = 100\text{ or }133\text{MHz}$		6	10	ns
$t_{dis1}$	Output disable time	SEL133/100	CPU_DIV2	$f_{(CPU)} = 100\text{ or }133\text{MHz}$		8	10	ns
$t_c$	CPU_DIV2 clock period†			$f_{(CPU)} = 100\text{ MHz}$	20	20.08	20.4	ns
				$f_{(CPU)} = 133\text{ MHz}$	15	15.06	15.3	ns
Cycle to cycle jitter				$f_{(CPU)} = 100\text{ or }133\text{MHz}$			250	ps
Duty cycle				$f_{(CPU)} = 100\text{ or }133\text{MHz}$	45	55		%
$t_{sk(p)}$	CPU_DIV2 pulse skew			$f_{(CPU)} = 100\text{ or }133\text{MHz}$			1.6	ns
$t_{w1}$	Pulse duration width, high			$f_{(CPU)} = 100\text{ MHz}$	7.1		ns	
				$f_{(CPU)} = 133\text{ MHz}$	4.7			
$t_{w2}$	Pulse duration width, low			$f_{(CPU)} = 100\text{ MHz}$	7.3	8.9		ns
				$f_{(CPU)} = 133\text{ MHz}$	5	6.6		
$t_r$	Rise time			$V_O = 0.4\text{ V to }2.0\text{ V}$	0.4	1.4	2	ns
$t_f$	Fall time			$V_O = 0.4\text{ V to }2.0\text{ V}$	0.4	1.3	1.8	ns

† The average over any 1- $\mu\text{s}$  period of time is greater than the minimum specified period.



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**WITH 3-STATE OUTPUTS**

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**switching characteristics,  $V_{DD} = 2.375\text{ V to }2.625\text{ V}$ ,  $T_A = 0^\circ\text{C to }85^\circ\text{C}$  (continued)**

**APIC**

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{en1}$	Output enable time	SEL133/100	APIC	$f_{(APIC)} = 16.67\text{ MHz}$		6	10	ns
$t_{dis1}$	Output disable time	SEL133/100	APIC	$f_{(APIC)} = 16.67\text{ MHz}$		8	10	ns
$t_c$	APIC clock period†			$f_{(APIC)} = 16.67\text{ MHz}$	60	60.24	60.6	ns
	Cycle to cycle jitter			$f_{(CPU)} = 100\text{ or }133\text{ MHz}$			400	ps
	Duty cycle			$f_{(APIC)} = 16.67\text{ MHz}$	45		55	%
$t_{sk(p)}$	APIC pulse skew			$f_{(APIC)} = 16.67\text{ MHz}$			3	ns
$t_{(off)}$	APIC clock to CPU clock offset, rising edge	APIC	CPUx		-1.5		-4	ns
$t_{w1}$	Pulse duration width, high			$f_{(APIC)} = 16.67\text{ MHz}$	25.5	28		ns
$t_{w2}$	Pulse duration width, low			$f_{(APIC)} = 16.67\text{ MHz}$	25.3	29.2		ns
$t_r$	Rise time			$V_O = 0.4\text{ V to }2\text{ V}$	0.4	1.6	2.1	ns
$t_f$	Fall time			$V_O = 0.4\text{ V to }2\text{ V}$	0.4	1.2	1.7	ns

† The average over any 1- $\mu\text{s}$  period of time is greater than the minimum specified period.

**switching characteristics,  $V_{DD} = 3.135\text{ V to }3.465\text{ V}$ ,  $T_A = 0^\circ\text{C to }85^\circ\text{C}$**

**3V66**

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{en1}$	Output enable time	SEL133/100	3V66x	$f_{(3V66)} = 66\text{ MHz}$		6	10	ns
$t_{dis1}$	Output disable time	SEL133/100	3V66x	$f_{(3V66)} = 66\text{ MHz}$		8	10	ns
$t_c$	3V66 clock period†			$f_{(3V66)} = 66\text{ MHz}$	15	15.06	15.3	ns
	Cycle to cycle jitter			$f_{(CPU)} = 100\text{ or }133\text{ MHz}$			400	ps
	Duty cycle			$f_{(3V66)} = 66\text{ MHz}$	45		55	%
$t_{sk(o)}$	3V66 bus skew	3V66x	3V66x	$f_{(3V66)} = 66\text{ MHz}$		50	150	ps
$t_{sk(p)}$	3V66 pulse skew	3V66n	3V66n	$f_{(3V66)} = 66\text{ MHz}$			2.6	ns
$t_{(off)}$	3V66 clock to CPU clock offset	3V66x	CPUx		0	-0.75	-1.5	ns
$t_{(off)}$	3V66 clock to PCI clock offset, rising edge				1.2	2.1	3	ns
$t_{w1}$	Pulse duration width, high			$f_{(3V66)} = 66\text{ MHz}$	5.2			ns
$t_{w2}$	Pulse duration width, low			$f_{(3V66)} = 66\text{ MHz}$	5			ns
$t_r$	Rise time			$V_O = 0.4\text{ V to }2\text{ V}$	0.5	1.5	2	ns
$t_f$	Fall time			$V_O = 0.4\text{ V to }2\text{ V}$	0.5	1.5	2	ns

† The average over any 1- $\mu\text{s}$  period of time is greater than the minimum specified period.



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switching characteristics,  $V_{DD} = 3.135\text{ V to }3.465\text{ V}$ ,  $T_A = 0^\circ\text{C to }85^\circ\text{C}$  (continued)

**48MHz**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{en1}$	Output enable time	SEL133/100	48MHz	6		10	ns	
$t_{dis1}$	Output disable time	SEL133/100	48MHz	8		10	ns	
$t_c$	48MHz clock period <sup>†</sup>		$f_{(48MHz)} = 48\text{ MHz}$	20.5	20.83	21.1	ns	
	Cycle to cycle jitter		$f_{(CPU)} = 100\text{ or }133\text{ MHz}$			500	ps	
	Duty cycle		$f_{(48MHz)} = 48\text{ MHz}$	45			55	%
$t_{sk(p)}$	48MHz pulse skew	48MHz	48MHz			3	ns	
$t_{w1}$	Pulse duration width, high		$f_{(48MHz)} = 48\text{ MHz}$	7.8			ns	
$t_{w2}$	Pulse duration width, low		$f_{(48MHz)} = 48\text{ MHz}$	7.8			ns	
$t_r$	Rise time		$V_O = 0.4\text{ V to }2\text{ V}$	1	2.1	2.8	ns	
$t_f$	Fall time		$V_O = 0.4\text{ V to }2\text{ V}$	1	1.9	2.8	ns	

<sup>†</sup> The average over any 1- $\mu\text{s}$  period of time is greater than the minimum specified period.

**REF**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{en1}$	Output enable time	SEL133/100	REFx	6		10	ns	
$t_{dis1}$	Output disable time	SEL133/100	REFx	8		10	ns	
$t_c$	REF clock period <sup>†</sup>		$f_{(REF)} = 14.318\text{ MHz}$	69.84			ns	
	Cycle to cycle jitter		$f_{(CPU)} = 100\text{ or }133\text{ MHz}$			700	ps	
	Duty cycle		$f_{(REF)} = 14.318\text{ MHz}$	45			55	%
$t_{sk(o)}$	REF bus skew	REFx	REFx	150		250	ps	
$t_{sk(p)}$	REF pulse skew	REFn	REFn			2	ns	
$t_{w1}$	Pulse duration width, high		$f_{(REF)} = 14.318\text{ MHz}$	26.2	32.7		ns	
$t_{w2}$	Pulse duration width, low		$f_{(REF)} = 14.318\text{ MHz}$	26.2	31.2		ns	
$t_r$	Rise time		$V_O = 0.4\text{ V to }2\text{ V}$	1	2	2.8	ns	
$t_f$	Fall time		$V_O = 0.4\text{ V to }2\text{ V}$	1	1.9	2.8	ns	

<sup>†</sup> The average over any 1- $\mu\text{s}$  period of time is greater than the minimum specified period.



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switching characteristics,  $V_{DD} = 3.135\text{ V to }3.465\text{ V}$ ,  $T_A = 0^\circ\text{C to }85^\circ\text{C}$  (continued)

**PCI**

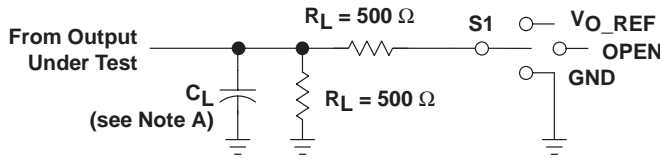
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{en1}$	Output enable time	SEL133/100	PCIx		6	10	ns
$t_{dis1}$	Output disable time	SEL133/100	PCIx	$f_{(PCI)} = 33\text{ MHz}$	8	10	ns
$t_c$	PCIx clock period <sup>†</sup>						
	Cycle to cycle jitter		$f_{(PCI)} = 33\text{ MHz}$	30	30.12	30.5	ns
	Duty cycle		$f_{(CPU)} = 100\text{ or }133\text{ MHz}$			300	ps
	Duty cycle		$f_{(PCI)} = 33\text{ MHz}$	45		55	%
$t_{sk(o)}$	PCIx bus skew	PCIx	PCIx	$f_{(PCI)} = 33\text{ MHz}$	70	300	ps
$t_{sk(p)}$	PCIx pulse skew	PCIn	PCIn	$f_{(PCI)} = 33\text{ MHz}$		4	ns
$t_{(off)}$	PCIx clock to 3V66 clock offset				-1.2	-3	ns
$t_{w1}$	Pulse duration width, high		$f_{(PCI)} = 33\text{ MHz}$	12			ns
$t_{w2}$	Pulse duration width, low		$f_{(PCI)} = 33\text{ MHz}$	12			ns
$t_r$	Rise time		$V_O = 0.4\text{ V to }2\text{ V}$	0.5	1.6	2	ns
$t_f$	Fall time		$V_O = 0.4\text{ V to }2\text{ V}$	0.5	1.5	2	ns

<sup>†</sup> The average over any 1- $\mu\text{s}$  period of time is greater than the minimum specified period.

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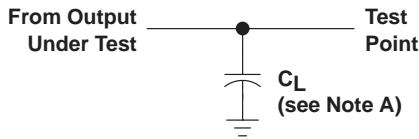
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**PARAMETER MEASUREMENT INFORMATION**

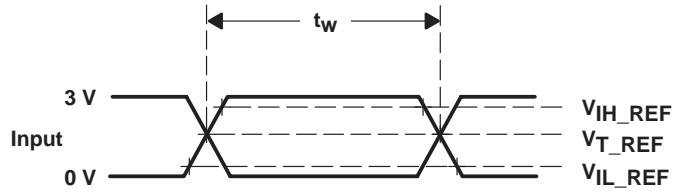


TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>O_REF</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

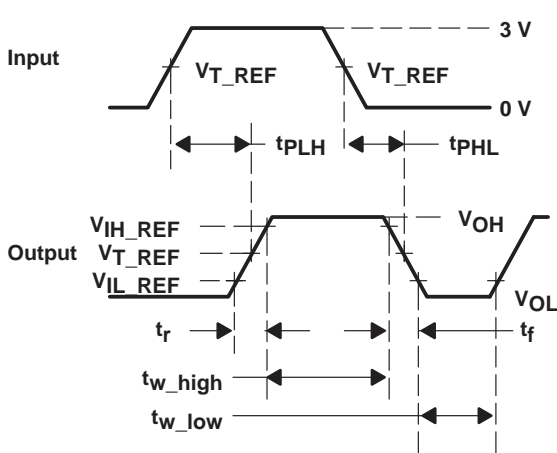
**LOAD CIRCUIT for t<sub>pd</sub> and t<sub>sk</sub>**



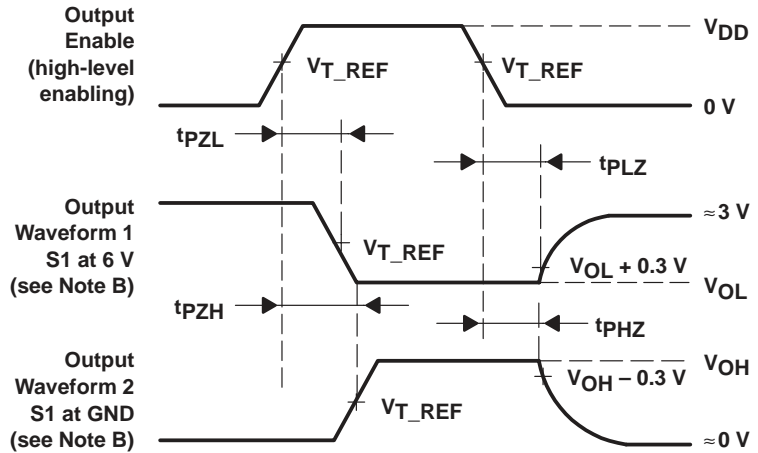
**LOAD CIRCUIT FOR t<sub>r</sub> and t<sub>f</sub>**



**VOLTAGE WAVEFORMS**



**VOLTAGE WAVEFORMS**



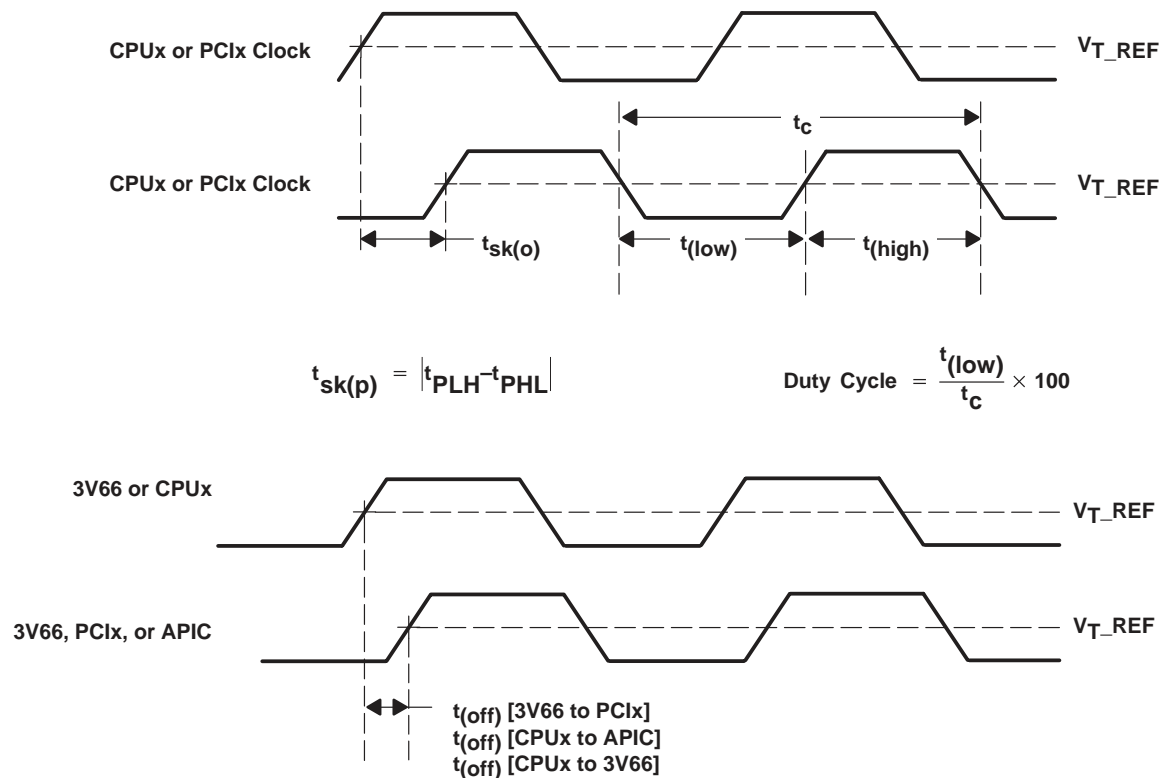
**VOLTAGE WAVEFORMS**

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance. C<sub>L</sub> = 20 pF (CPUx, APIC, 48MHz, REF), C<sub>L</sub> = 30 pF (PC1x)  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 14.318 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time with one transition per measurement.

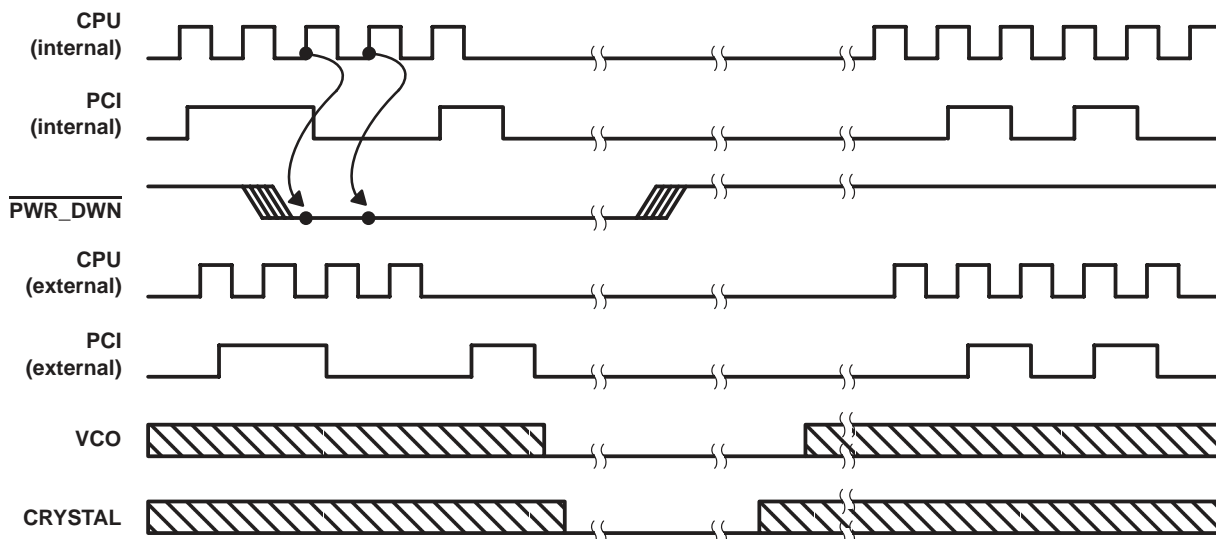
PARAMETER		3.3-V INTERFACE	2.5-V INTERFACE	UNIT
V <sub>IH_REF</sub>	High-level reference voltage	2.4	2	V
V <sub>IL_REF</sub>	Low-level reference voltage	0.4	0.4	V
V <sub>T_REF</sub>	Input Threshold reference voltage	1.5	1.25	V
V <sub>O_REF</sub>	Off-state reference voltage	6	4.6	V

**Figure 3. Load Circuit and Voltage Waveforms**

**PARAMETER MEASUREMENT INFORMATION**



**Figure 4. Waveforms for Calculation of Skew, Offset, and Jitter**



NOTE A: Shaded sections on the VCO and Crystal waveforms indicate that the VCO and crystal oscillators are active and there is a valid clock.

**Figure 5. Power-Down Timing**

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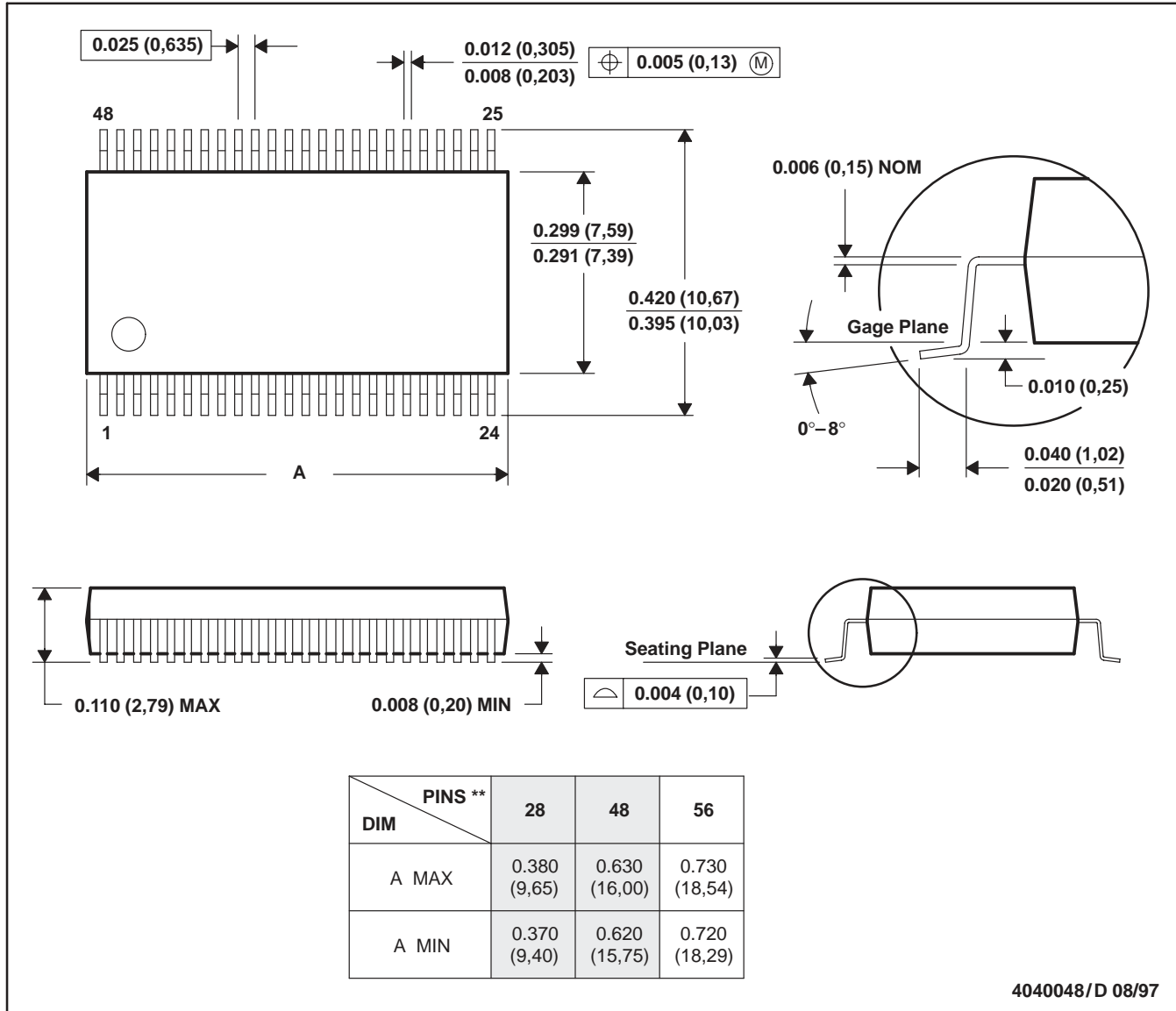
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**MECHANICAL DATA**

**DL (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

48-PIN SHOWN



4040048/D 08/97

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDC922DL	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
CDC922DLR	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
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Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

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