

QUADRATURE CLOCK CONVERTER

June 2015

FEATURES:

- x1, x2 and x4 resolution
- Programmable output pulse width (200ns to 140µs)
- Excellent regulation of output pulse width
- TTL and low voltage CMOS compatible I/Os
- +3V to +12V operation (VDD - VSS)
- **LS7183N, LS7184N** (DIP);
LS7183NS, LS7184NS (SOIC) - See Figure 1

Applications:

- Interface incremental encoders to Up / Down Counters (See Figure 6A and Figure 6B)
- Interface rotary encoders to Digital Potentiometers (See Figure 7)

DESCRIPTION:

The **LS7183N** and **LS7184N** are CMOS quadrature clock converters. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B inputs of the **LS7183N / LS7184N**, are converted to strings of Up Clocks and Down Clocks (**LS7183N**) or to a Clock and an Up/Down direction control (**LS7184N**). These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

INPUT/OUTPUT DESCRIPTION:

RBIAS (Pin 1)

Input for external component connection. A resistor connected between this input and Vss adjusts the output clock pulse width (Tow).

VDD (Pin 2)

Supply Voltage positive terminal.

VSS (Pin 3)

Supply Voltage negative terminal.

A, B (Pin 4, Pin 5)

Quadrature Clock inputs A and B. Directional output pulses are generated from the A and B clocks according to Fig. 2. A and B inputs have built-in immunity for noise signals less than 50ns duration (Validation delay, T_{VD}). The A and B inputs are inhibited during the occurrence of a directional output clock (UPCK or DNCK), so that spurious clocks resulting from encoder dither are rejected.

MODE (Pin 6)

MODE is a 3-state input to select resolution x1, x2 or x4. The input quadrature clock rate is multiplied by factors of 1, 2 and 4 in x1, x2 and x4 mode, respectively, in producing the output UP/DN clocks (See Fig. 2). x1, x2 and x4 modes selected by the MODE input logic levels are as follows:

- Mode = 0 : x1 selected
- Mode = 1 : x2 selected
- Mode = Float : x4 selected

PIN ASSIGNMENT - TOP VIEW

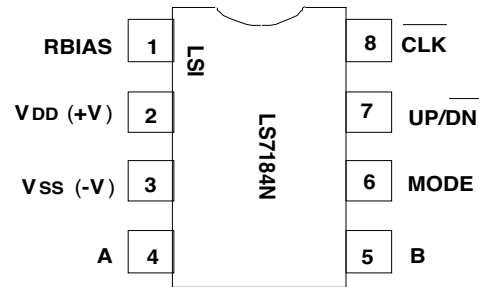
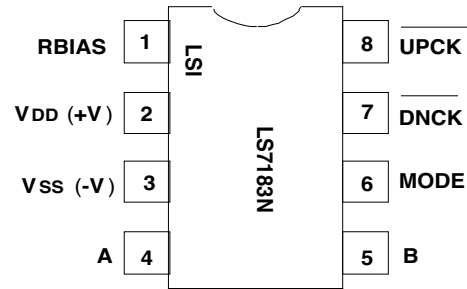


FIGURE 1

LS7183N - DNCK (Pin 7)

In **LS7183N**, this is the DOWN Clock Output. This output consists of low-going pulses generated when A input lags the B input.

LS7184N - UP/DN (Pin 7)

In **LS7184N**, this is the count direction indication output. When A input leads the B input, the UP/DN output goes high indicating that the count direction is UP. When A input lags the B input, UP/DN output goes low, indicating that the count direction is DOWN.

LS7183N - UPCK (Pin 8)

In **LS7183N**, this is the UP Clock output. This output consists of low-going pulses generated when A input leads the B input.

LS7184N - CLK (Pin 8)

In **LS7184N**, this is the combined UP Clock and DOWN Clock output. The count direction at any instant is indicated by the UP/DN output (Pin 7).

NOTE: For the **LS7184N**, the timing of CLK and UP/DN requires that the counter interfacing with **LS7184N** counts on the rising edge of the CLK pulses.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	$V_{DD} - V_{SS}$	16	V
Voltage at any input	V_{IN}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Operating temperature	T_A	-20 to +85	°C
Storage temperature	T_{STG}	-55 to 150	°C

DC ELECTRICAL CHARACTERISTICS: (Unless otherwise specified VDD=3V to 12V and TA=-20°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITION
Supply Voltage	V_{DD}	3	-	12	V	-
Supply Current	I_{DD}	-	1.5	1.65	mA	$V_{DD}=12V$, all input frequencies=0 Hz and $R_{BIAS}=2M\Omega$

MODE INPUT:

Logic 0	V_{ml}	-	-	0.5	V	-
Logic 1	V_{mh}	$V_{DD} - 0.5$	-	-	V	-
Logic Float	V_{mf}	$(V_{DD}/2) - 0.5$	$V_{DD}/2$	$(V_{DD}/2) + 0.5$	V	-
Logic 0 Input Current	I_{ml}	-	2.2	4.2	μA	$V_{DD} = 3V$
	I_{ml}	-	3.5	6.9	μA	$V_{DD} = 5V$
	I_{ml}	-	8.3	16.2	μA	$V_{DD} = 12V$
Logic 1 Input Current	I_{mh}	-	-2	-9.8	μA	$V_{DD} = 3V$
	I_{mh}	-	-3.4	-6.6	μA	$V_{DD} = 5V$
	I_{mh}	-	-8.2	-16	μA	$V_{DD} = 12V$

A,B INPUTS:

Logic 0	V_{ABl}	-	-	$0.25V_{DD}$	V	-
Logic 1	V_{ABh}	$0.7V_{DD}$	-	-	V	-
Input Current	I_{ABlk}	-	0	10	nA	-

RBIAS INPUT:

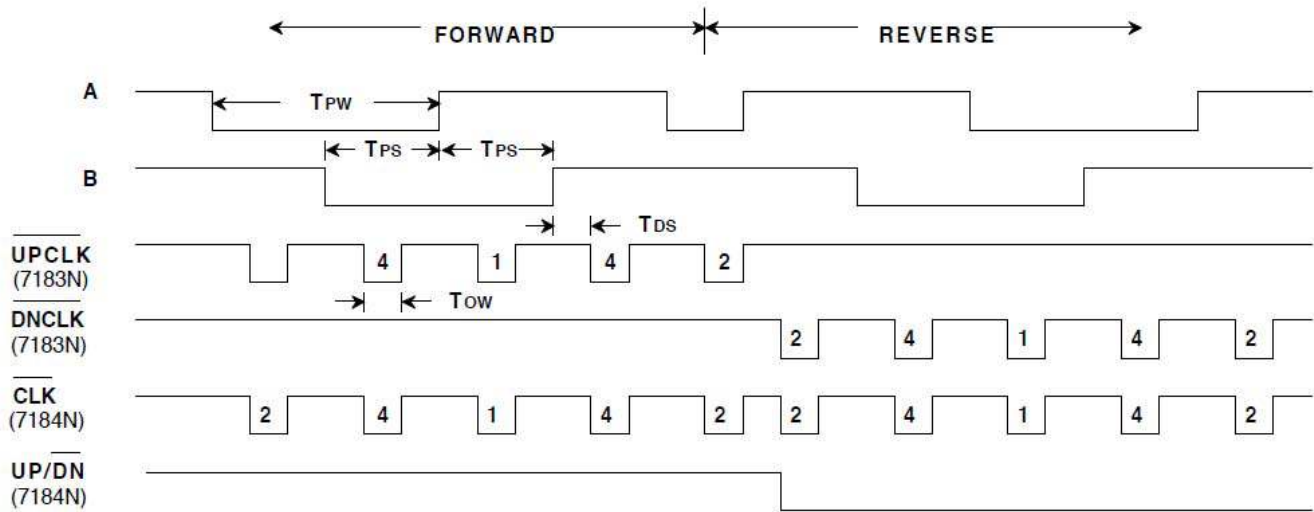
External Resistor	R_B	2K	-	10M	Ω	-
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ALL OUTPUTS:

Sink Current	I_{ol}	-	-3.4	-	mA	$V_O = 0.5V, V_{DD} = 3V$
	I_{ol}	-	-4.8	-	mA	$V_O = 0.5V, V_{DD} = 5V$
	I_{ol}	-	-7.2	-	mA	$V_O = 0.5V, V_{DD} = 12V$
Source Current	I_{oh}	-	1.7	-	mA	$V_O = 2.5V, V_{DD} = 3V$
	I_{oh}	-	2.2	-	mA	$V_O = 4.5V, V_{DD} = 5V$
	I_{oh}	-	3.1	-	mA	$V_O = 11.5V, V_{DD} = 12V$

TRANSIENT CHARACTERISTICS ($T_A = -20^\circ C$ to $+85^\circ C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITION	
Output Clock Pulse Width	T_{OW}	540	-	-	ns	$V_{DD} = 3V$	
	T_{OW}	225	-	-	ns	$V_{DD} = 5V$	
	T_{OW}	112	-	-	ns	$V_{DD} = 12V$	
A,B INPUTS:							
	Validation Delay	T_{VD}	-	450	-	ns	$V_{DD} = 3V$
	T_{VD}	-	200	-	ns	$V_{DD} = 5V$	
T_{VD}	-	90	-	ns	$V_{DD} = 12V$		
Phase Delay	T_{PS}	$T_{VD}+T_{OW}$	-	∞	s	-	
Pulse Width	T_{PW}	$2T_{PS}$	-	∞	s	-	
Frequency	$f_{A,B}$	-	-	$1/(2T_{PW})$	Hz	-	
Input to output Delay	T_{DS}	-	490	565	ns	$V_{DD} = 3V$	
	T_{DS}	-	220	345	ns	$V_{DD} = 5V$	
	T_{DS}	-	125	135	ns	$V_{DD} = 12V$	



NOTE: Output clocks labeled 1, 2 and 4 have the following interpretations.
 1: Generated in x1, x2 and x4 modes
 2: Generated in x2 and x4 modes only
 4: Generated in x4 mode only

FIGURE 2. LS7183N, LS7184N INPUT/OUTPUT TIMING

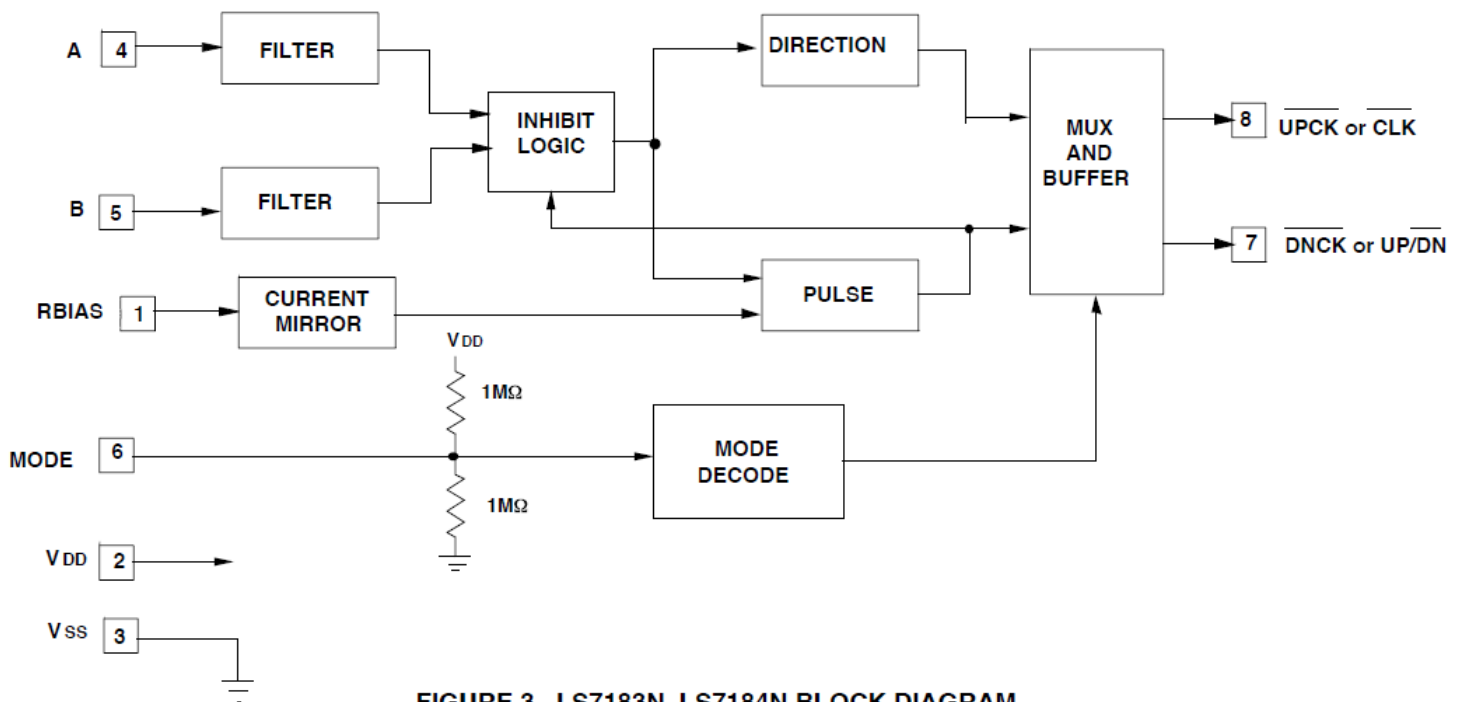


FIGURE 3. LS7183N, LS7184N BLOCK DIAGRAM

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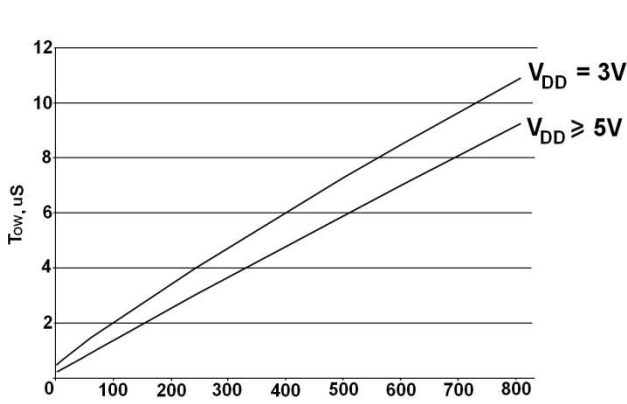


Figure 4. T_{OW} vs. R_{BIAS} (R in $K\Omega$)

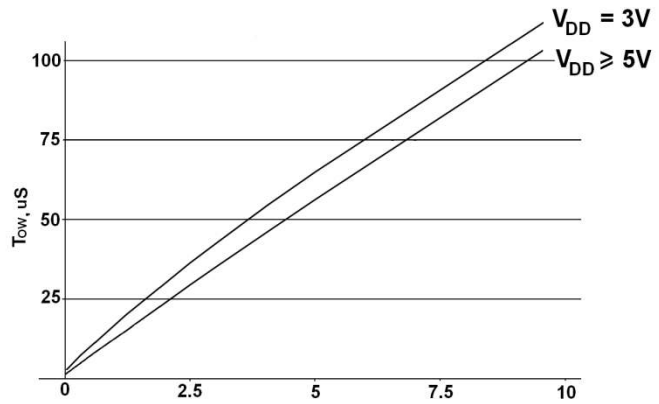


Figure 5. T_{OW} vs. R_{BIAS} (R in $M\Omega$)

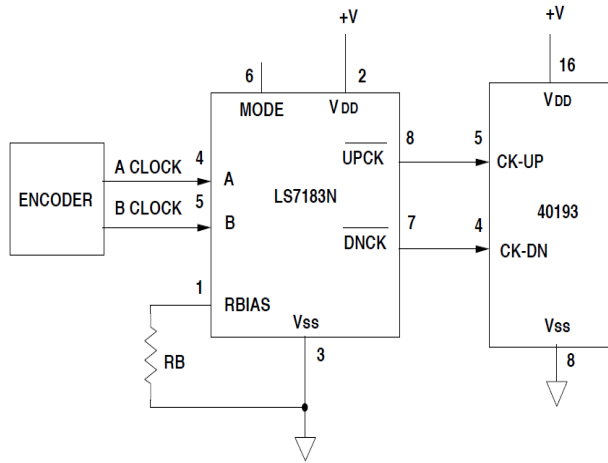


Figure 6A. TYPICAL APPLICATION FOR LS7183 in X4 MODE

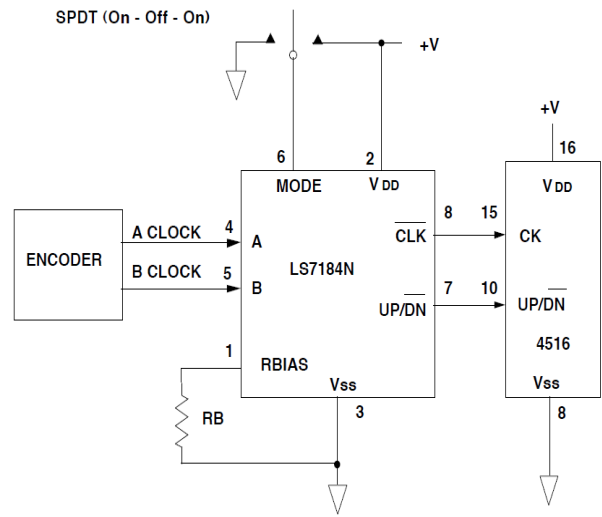
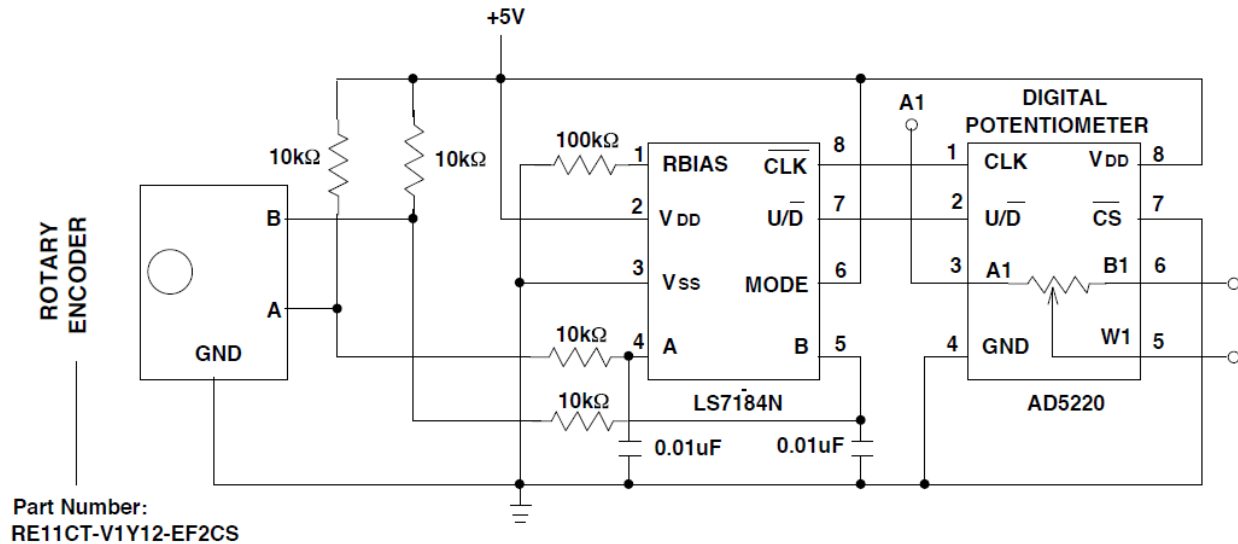


Figure 6B. TYPICAL APPLICATION FOR LS7184N WITH MODE SELECTION

*See NOTE at bottom right of Page 1



Part Number:
RE11CT-V1Y12-EF2CS

FIGURE 7. ROTARY ENCODER CONTROL OF DIGITAL POTENTIOMETER