SN75DP126 DisplayPort™ 1:2 Re-Driver Switch with TMDS Translator

1 Features

- One Dual-Mode DisplayPort™ (DP++) Input; Switchable to One DP++ Output or One TMDS Output Compatible with HDMI 1.4b and DVI
- Supports DP v1.1a and DP v1.2 Signaling Including HBR2 Data Rates to 5.4 Gbps
- Supports HDMI 1.4b with TMDS Clock Frequencies up to 340 MHz with 10 m Cable
- Glue-less interface to AMD, Intel, and NVIDIA Graphics Processors
- Auto-Configuration Through Link Training for DisplayPort Connection
- Integrated DDC-Accessible DP-HDMI Adaptor ID for HDMI/DVI Sink Recognition
- Output Signal Conditioning with Tunable Voltage Swing and Pre-Emphasis Gain for both DisplayPort and TMDS Outputs
- Highly-Configurable Input-Variable Equalizer
- Two Device Options Including a Dual Power-Supply Configuration for Lowest Power
- 2-kV ESD HBM Protection
- Temperature Range: 0°C to 85°C
- 56-Pin 5-mm x 11-mm QFN Package

2 Applications

- Notebook PC
- Desktop PC
- PC Docking Station
- PC Standalone Video Card

3 Description

The SN75DP126 switches one Dual-Mode DisplayPort (DP++) input to one Dual-Mode DisplayPort (DP++) sink output or one HDMI/DVI sink output. The HDMI/DVI output has a built-in level translator compliant with DVI 1.0 and HDMI 1.4b standard TMDS signaling, and is specified up to a maximum data rate of 3.4 Gbps, supporting resolutions greater than 1920 X 1440 and HDTV deep color at 1080p. An integrated DP-HDMI Adaptor ID buffer can be accessed when the HDMI/DVI sink is selected to indicate support for HDMI signaling.

The device compensates for PCB-related frequency loss and switching-related loss to provide the optimum electrical performance from source to sink. The DP++ Main Link signal inputs feature-configurable equalizers with selectable boost settings.

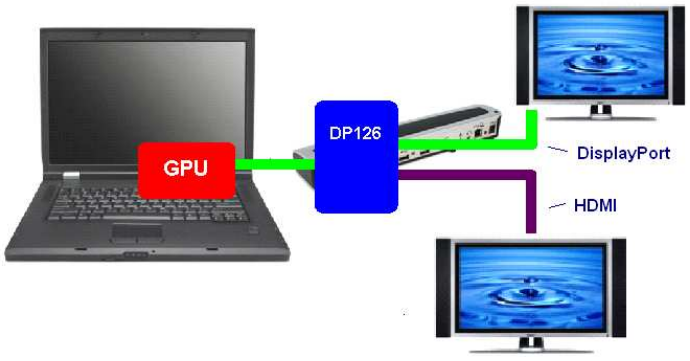
At the SN75DP126 DP++ Main Link output, four primary levels of differential output voltage (V_{OD}) swing and four primary levels of pre-emphasis are available as well as a secondary level of boost adjustment, programmed through I^2C, for fine-tuning the Main Link output. The device can monitor the AUX channel and automatically adjust output signaling levels and input equalizers based on DP Link Training commands.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75DP126	WQFN (56)	11.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2012) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed the location of the illustrations within the Elec Spec section to the very end of the tables. ... 11

Changes from Original (February 2012) to Revision A **Page**

- Changed the device From Product Preview To Production ... 1

5 Description (continued)

The SN75DP126 offers separate AUX and DDC source interfaces that connect to the DisplayPort AUX sink channel and the HDMI DDC sink channel, that seamlessly interface to graphics processor (GPU) comprising separate DDC and AUX interfaces as well as GPUs with combined DDC/AUX. Other sideband circuits such as Hot Plug Detect (HPD) are optimized to reduce external components providing a seamless connection to Intel, AMD, and NVIDIA graphics processors.

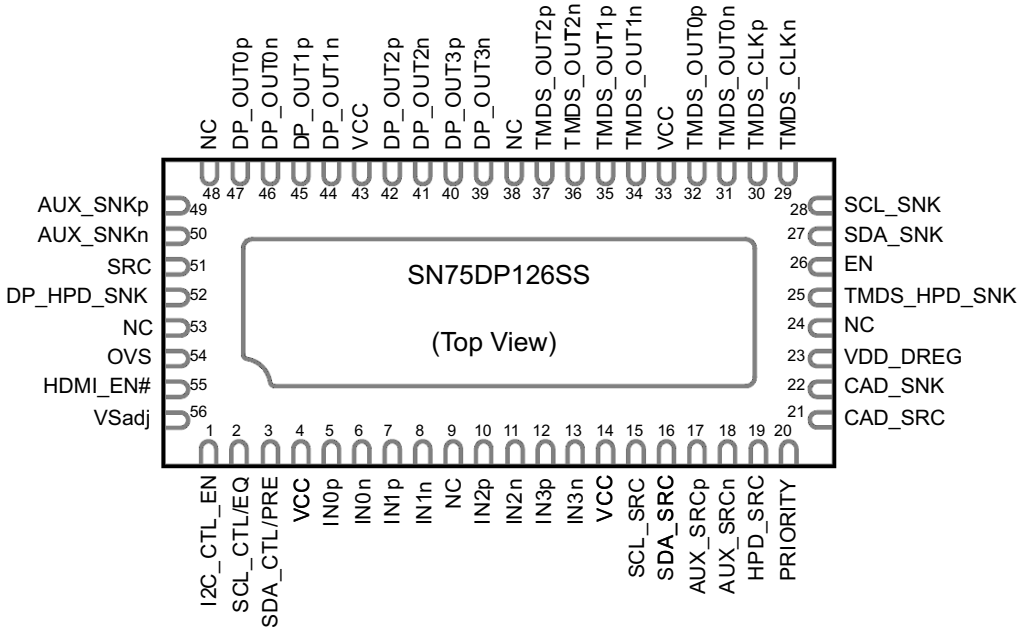
The SN75DP126 is optimized for mobile applications, and contains activity-detection circuitry on the DP++ Main Link input that transitions to a low-power Output Disable mode in the absence of a valid input signal. Other low power modes are supported, including a Standby mode with typical dissipation of ~2 mW when no video sink (for example, monitor) is connected.

The device is characterized for an extended operational temperature range from 0°C to 85°C.

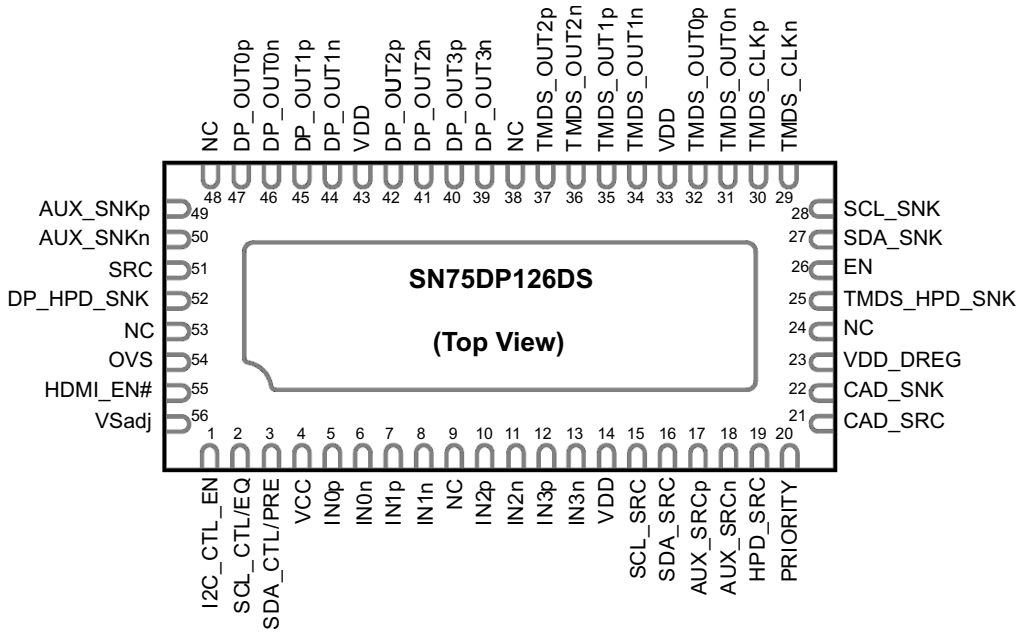
At the SN75DP126 HDMI/DVI output, the differential output voltage swing and pre-emphasis levels are configurable. The SN75DP126 output signal conditioning and EQ parameters are programmable through the I^2C interface, the VSadj terminal, and the I2C_CTL_EN terminal. The HDMI/DVI sink TMDS output slew rate is controlled by the SRC control input.

6 Pin Configuration and Functions

SN75DP126SS Single Supply RHU Package
56-Pin WQFN with Thermal Pad
Top View



SN75DP126DS Dual Supply RHU Package
56-Pin WQFN with Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
SIGNAL	NO.		
DISPLAYPORT AND HDMI MAIN LINK TERMINALS			
IN0p, IN0n	5, 6	100Ω Differential Input	DisplayPort Main Link Lane 0 Differential Input
IN1p, IN1n	7, 8		DisplayPort Main Link Lane 1 Differential Input
IN2p, IN2n	10, 11		DisplayPort Main Link Lane 2 Differential Input
IN3p, IN3n	12, 13		DisplayPort Main Link Lane 3 Differential Input
DP_OUT0p, DP_OUT0n	47, 46	100Ω Differential Output	DisplayPort Main Link Lane 0 Differential Output
DP_OUT1p, DP_OUT1n	45, 44		DisplayPort Main Link Lane 1 Differential Output
DP_OUT2p, DP_OUT2n	42, 41		DisplayPort Main Link Lane 2 Differential Output
DP_OUT3p, DP_OUT3n	40, 39		DisplayPort Main Link Lane 3 Differential Output
TMDS_CLKp, TMDS_CLKn	30, 29	100Ω Differential Output (Failsafe)	HDMI/DVI Clock TMDS Differential Output
TMDS_OUT0p, TMDS_OUT0n	32, 31		HDMI/DVI Data Lane 0 TMDS Differential Output
TMDS_OUT1p, TMDS_OUT1n	35, 34		HDMI/DVI Data Lane 1 TMDS Differential Output
TMDS_OUT2p, TMDS_OUT2n	37, 36		HDMI/DVI Data Lane 2 TMDS Differential Output

Pin Functions (continued)

PIN		I/O	DESCRIPTION
SIGNAL	NO.		
AUX CHANNEL AND DDC DATA TERMINALS			
AUX_SRCp, AUX_SRCn	17, 18	I/O (Failsafe)	Source Side Bidirectional DisplayPort Auxiliary Data Channel. These signals are connected to the AUX_SNK channel when the DisplayPort sink is selected; AC coupling should be implemented.
AUX_SNKp, AUX_SNKn	49, 50		Sink Side Bidirectional DisplayPort Auxiliary Data Channel.
SCL_SRC, SDA_SRC	15, 16		Source Side Bidirectional I^2C Display Data Channel (DDC) for TMDS modes. These terminals include integrated 60 kΩ pull-up resistors.
SCL_SNK, SDA_SNK	28, 27		HDMI/DVI Sink Side Bidirectional I^2C Display Data Channel (DDC).
HOT PLUG DETECT AND CAD TERMINALS			
HPD_SRC	19	Output	Hot Plug Detect Output to the Source. This output shall be driven high when the source shall be connected to either the HDMI/DVI sink or the DisplayPort sink, and driven low when no sink is selected. This output will be asserted for a fixed period of time during active (PRIORITY based) transition from one sink to the other.
CAD_SRC	21		Source Side Cable Adapter Detect Output. When the DisplayPort sink is selected, this output represents the condition of the CAD_SNK input, active high as default; polarity may be programmed through the local I^2C interface. When the HDMI/DVI sink is selected, this output is driven high.
DP_HPD_SNK	52	Input (Failsafe)	DisplayPort Hot Plug Detect Input from Sink. This device input is 5-V tolerant, and includes an integrated 130 kΩ pull-down resistor. *Note: pull this input high during compliance testing or use I^2C control interface to go into compliance test mode and control DP_HPD_SNK and HPD_SRC by software.*
TMDS_HPD_SNK	25		HDMI/DVI Hot Plug Detect Input from Sink. This device input is 5-V tolerant, and includes an integrated 130 kΩ pull-down resistor.
CAD_SNK	22	Input	DisplayPort Cable Adapter Detect Input. An external 1MΩ resistor to GND is recommended. This terminal is used to select DP mode (low input) or TMDS mode (high input) when the DisplayPort sink is selected .
CONTROL TERMINALS			
VSadj	56	Input	HDMI/DVI Sink Differential Voltage Swing Control. An external resistor connecting this pin to GND determines the output voltage swing. A value of 4.7 kΩ is recommended to provide a typical swing of 1000 mV. VSadj resistor values of 4.7 kΩ ± 1 kΩ control the output voltage swing in a near-linear function of approximately 2 mV/100 Ω. *Note: this input does not impact the output when a DisplayPort sink is selected and operating in TMDS mode (as supported by the DP++ source)*
HDMI_EN#	55		HDMI/DVI Sink Type Control. When this input is low, the output is HDMI 1.4b compliant when the HDMI/DVI sink is selected. When this input is high, the output is DVI 1.0 compliant when the HDMI/DVI sink is selected.
PRIORITY	20		Output Select Priority. Selects the priority for the output in the case both DP_HPD_SNK and TMDS_HPD_SNK are high indicating two sinks are connected. When low, the DisplayPort sink has priority selection. When high, the HDMI/DVI sink has priority. *Note: An external RC circuit should be connected to the PRIORITY pin to insure that the SN76DP126 functions properly with some non-compliant monitors. See the SN75DP126 Reference Schematics for more information.*
SRC	51	3-Level Input	TMDS Slew Rate Control. When the HDMI/DVI sink is selected, the slew rate is controlled by the HDMI_EN# input and by the SRC control input: V_{IL} = TMDS rise and fall times meet tT1 specifications V_{IM} (between V_{IL} and V_{IH}) = TMDS rise and fall times meet t_{T2} specifications (Recommended setting) V_{IH} = TMDS rise and fall times meet t_{T3} specifications *Note: this input does not impact the output when a DisplayPort sink is selected and operating in TMDS mode (as supported by the DP++ source)*
OVS	54	3-Level Input	Source Side DDC Input/Output Buffer Control Input. When the HDMI/DVI sink is selected, the DDC V_{OL} and V_{IL} is controlled by the OVS control input: V_{IL} = Source DDC interface meets $V_{OL(3)}$ and $V_{IL(3)}$ specifications V_{IM} (between V_{IL} and V_{IH}) = Source DDC interface meets $V_{OL(2)}$ and $V_{IL(2)}$ specifications V_{IH} = Source DDC interface meets $V_{OL(1)}$ and $V_{IL(1)}$ specifications
I2C_CTL_EN	1	3-Level Input	Local I^2C Interface Enable Control and Target Address Select. When low, the local I^2C interface is disabled; when input is between V_{IL} and V_{IH} levels, the local I^2C interface is enabled and is addressed at 0x58h (Write) and 0x59h (Read); when input is high, the local I^2C interface is enabled and is addressed at 0x5Ah (Write) and 0x5Bh (Read).
SCL_CTL/EQ	2	3-Level Input (Failsafe)	Local I^2C Interface Clock, or Equalizer Setting Control Input. When I2C_CTL_EN is input high or floating, this terminal is the local I^2C interface clock used to configure SN75DP126. When I2C_CTL_EN is low, this terminal can be used to configure the input EQ.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
SIGNAL	NO.		
SDA_CTL/PRE	3	I/O 3-Level Input (Failsafe)	Local I^2C Interface Data, or TMDS Pre-emphasis Control Input. When I2C_CTL_EN is input high or floating, this terminal is the local I^2C interface data signal. When I2C_CTL_EN is low, this terminal configures the HDMI/DVI sink TMDS output pre-emphasis as: V_{IL} = 0 dB pre-emphasis applied to TMDS output V_{IM} = Not Recommended V_{IH} = 2 dB pre-emphasis applied to TMDS output When 2 dB pre-emphasis is enabled, the steady state TMDS output swing is reduced from that selected by VSadj, and the transition time is reduced from that selected by SRC. *Note: this input does not impact the output when a DisplayPort sink is selected and operating in TMDS mode (as supported by the DP++ source), whereas no pre-emphasis is applied to the output signal in this condition.*
EN	26	Low-Voltage Input (Failsafe)	Device Enable / Reset (Power Down). This input incorporates internal pullup of 150 kΩ, and only 1.2-V tolerant (the high level shall be limited to 1.2 V). When high, the device is enabled for normal operation. When low, the device is in power down mode; all outputs excluding HPD_SRC and CAD_SRC are high-impedance, and inputs excluding DP_HPD_SNK, TMDS_HPD_SNK, and CAD_SNK are ignored; all local I^2C and DPCD registers are reset to their default values when this input is low. At power up, the EN input must not be de-asserted until the V_{CC} supply has reached at least the minimum recommended supply voltage level.
SUPPLY AND GROUND TERMINALS			
V_{CC}	SN75DP126SS 4, 14, 33, 43 SN75DP126DS 4		3.3-V Supply
V_{DD}	SN75DP126DS 14, 33, 43		1.05-V Supply
V_{DD_DREG}	23		SN75DP126SS: Digital voltage regulator decoupling; install 1uF to GND. SN75DP126DS: Treat same as V_{DD}; this pin will be most noisy of all V_{DD} terminals and needs a de-coupling capacitor nearby.
GND	Exposed Thermal Pad		Ground. Reference GND connection shall be made to the exposed thermal pad.
NC	9, 53, 38, 48, 24		No connect. These terminals may be left unconnected, or connect to GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	V_{CC}	–0.3	4	V
	V_{DD}, V_{DD_DREG}	–0.3	1.3	V
Voltage range	Main Link I/O Differential Voltage	–0.3	1.4	V
	DP_HPD_SNK, TMDS_HPD_SNK, SCL_SNK, SDA_SNK	–0.3	5.5	V
	EN	–0.3	1.3	V
	All other terminals	–0.3	4	V
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{DD}	Digital core and Main Link supply voltage		1.0	1.05	1.2	V
T_A	Operating free-air temperature		0		85	°C
T_S	Storage temperature		-65		150	°C
T_{CASE}	Case temperature			97.1		°C
DP++ MAIN LINK TERMINALS						
V_{ID}	Peak-to-peak input differential voltage; RBR, HBR, HBR2		0.3		1.40	Vpp
$d_{R(DP)}$	Data rate; DisplayPort sink			5.4		Gbps
$d_{R(HDMI)}$	Data rate; HDMI sink			3.4		Gbps
C_{AC}	AC coupling capacitance (each DP input and each DP output line)		75		200	nF
R_{tdiff}	Differential output termination resistance; DisplayPort sink and HDMI sink		80	100	120	Ω
V_{Oterm}	Output termination voltage (AC coupled)		0		2	V
$t_{SK(HBR2)}$	Intra-pair skew at the input at 5.4 Gbps			20		ps
$t_{SK(HBR)}$	Intra-pair skew at the input at 2.7 Gbps			100		ps
$t_{SK(RBR)}$	Intra-pair skew at the input at 1.62 Gbps			300		ps
AUX CHANNEL DATA TERMINALS						
V_{I-DC}	DC Input Voltage, AUX_SRCp/n and AUX_SNKp/n (DP and TMDS modes)		-0.5		3.6	V
V_{ID}	Differential input voltage amplitude (DP mode only)		300		1400	mV_{PP}
$d_{R(AUX)}$	Data rate (before Manchester encoding)		0.8	1	1.2	Mbps
$d_{R(FAUX)}$	Data rate Fast AUX (300ppm frequency tolerance)			720		Mbps
t_{jccin_adj}	Cycle-to-cycle AUX input jitter adjacent cycle (DP mode only)				0.05	UI
t_{jccin}	Cycle-to-cycle AUX input jitter within one cycle (DP mode only)				0.1	UI
C_{AC}	AUX AC coupling capacitance		75		200	nF
DDC, LOCAL I^2C, AND CONTROL TERMINALS						
V_{I-DC}	DC Input Voltage	DP_HPD_SNK, TMDS_HPD_SNK, SCL/SDA_SNK	–0.3		5.5	V
		All other DDC, local I^2C, and control terminals	–0.3		3.6	
V_{IH}	High-level input voltage	SCL/SDA_SRC	2.1			V
		All other DDC, Local I^2C, and control terminals	V_{CC}–0.5			
V_{IL}	Low-level input voltage(1)			0.5		V
V_{IM}	Mid-level input voltage(2)		V_{CC}/2–0.3		V_{CC}/2+0.3	
d_R	Data rate			100		kbps
$V_{TH(EN)}$	EN input threshold voltage		280		800	mV
f_{SCL}	SCL clock frequency standard I^2C mode			100		kHz
$t_{w(L)}$	SCL clock low period standard I^2C mode		4.7			µs
$t_{w(H)}$	SCL clock high period standard I^2C mode		4.0			µs
C_{bus}	Total capacitive load for each bus line (DDC and local I^2C terminals)			400		pF

(1) V_{IL} for SCL_SRC and SDA_SRC are listed in the AUX/DDC/I^2C Electrical Characteristics Table.
(2) V_{IM} is only applicable for 3-Level control pins.

7.4 Thermal Information

THERMAL METRIC[1]		SN75DP126 RHU (WQFN) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Power Supply Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device current under normal operation	4 DP Lanes; DP Sink Maximum Conditions: DP at 5.4-Gbps PRBS, V_{OD} = 510 mV_{pp}, PRE = 6 dB; AUX at 1-Mbps PRBS, V_{ID} = 1000 mVpp; EQ = 6 dB Typical Conditions: DP at 5.4-Gbps PRBS, V_{OD} = 510 mVpp, PRE = 0 dB AUX and I^2C Idle; EQ = 3 dB		138	242	mA
		2 DP Lanes; DP Sink Maximum Conditions: DP at 5.4-Gbps PRBS, V_{OD} = 510 mVpp, PRE = 6 dB; AUX at 1-Mbps PRBS, V_{ID} = 1000 mVpp; EQ = 6 dB Typical Conditions: DP at 5.4-Gbps PRBS, V_{OD} = 510 mVpp, PRE = 0 dB AUX and I^2C Idle; EQ = 3 dB		73	125	mA
		1 DP Lanes; DP Sink Maximum Conditions: DP at 5.4-Gbps PRBS, V_{OD} = 510 mVpp, PRE = 6 dB; AUX at 1-Mbps PRBS, V_{ID} = 1000 mVpp; EQ = 6 dB Typical Conditions: DP at 5.4-Gbps PRBS, V_{OD} = 510 mVpp, PRE = 0 dB AUX and I^2C Idle; EQ = 3 dB		42	70	mA
		4 DP Lanes; HDMI Sink Maximum Conditions: TMDS at 3.4 Gbps, V_{OD} = 1200 mVpp, V_{ID} = 1000 mVpp Typical Conditions: TMDS at 3.4 Gbps, V_{OD} = 1000 mVpp, DDC and I^2C Idle		130	160	mA
I_{SD}	Shutdown mode current	4 DP Lanes		0.55	4.00	mA
I_{SBY}	Standby mode current	4 DP Lanes.		0.85	4.00	mA
I_{D3}	D3 power down mode current	4 DP Lanes.		10	15	mA
I_{OD}	Output disable (squelch) mode current	4 DP Lanes.		53	75	mA

(1) Values are V_{CC} supply measurements for SN75DP126SS and V_{DD} supply measurements for the SN75DP126DS; the maximum V_{CC} supply measurement for the SN75DP126DS is 8 mA during normal operation and 0.5 mA during shutdown, standby, and D3 power down modes.

7.6 Main Link Input Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{EQ(HBR)}$	Equalizer gain for RBR/HBR	See Table 4 for EQ setting details; Max value represents the typical value for the maximum configurable EQ setting			9	dB
AEQ(HBR2)	Equalizer gain for HBR2				18	dB
AEQ(TMDS_D)	Equalizer gain for DP sink in TMDS mode; data lanes				9	dB
AEQ(TMDS_C)	Equalizer gain for DP sink in TMDS mode; clock lane				3	dB
AEQ(HDMI_D)	EQ gain, HDMI sink; data lanes				9	dB
AEQ(HDMI_C)	EQ gain, HDMI sink; clock lane				3	dB
RIN	Input termination impedance		40	50	60	Ω
VIterm	Input termination voltage	AC coupled; self-biased	0		2	V
$V_{SQUELCH}$	Squelch threshold voltage	SQUELCH_SENSITIVITY = 00		60		mV_{PP}
		SQUELCH_SENSITIVITY = 01 (default)		115		
		SQUELCH_SENSITIVITY = 10		160		
		SQUELCH_SENSITIVITY = 11		200		

7.7 DisplayPort Main Link Output Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OD(L0)}$	Output Differential Voltage Swing	$V_{PRE(L0)}$; 675 Mbps D10.2 Test Pattern; BOOST = 01; 100-Ω R_{tdiff} Termination		238	340	442	mV_{PP}
$V_{OD(L1)}$				357	510	663	
$V_{OD(L2)}$				484	690	897	
$V_{OD(L3)}$				700	1000	1300	
$V_{OD(TMDS)}$		675 Mbps D10.2 Test Pattern; BOOST = 01		420	600	780	
$\Delta V_{OD(L0L1)}$	Output Peak-to-Peak Differential Voltage Delta	$\Delta V_{ODn} = 20 \times \log(V_{ODL(n+1)} / V_{ODL(n)})$ Per PHY_CTS section 3.2 at TP2		1.7	3.5	5.3	dB
$\Delta V_{OD(L1L2)}$				1.6	2.5	3.5	
$\Delta V_{OD(L2L3)}$				0.8	3.5	6.0	
$V_{PRE(L0)}$	Driver output pre-emphasis	All V_{OD} options; Any BOOST setting			0	0.25	dB
$V_{PRE(L1)}$		$V_{OD} = V_{OD(L0)}$, $V_{OD(L1)}$, or $V_{OD(L2)}$; BOOST = 01			3.5		
$V_{PRE(L2)}$		$V_{OD} = V_{OD(L0)}$ or $V_{OD(L1)}$; BOOST = 01			6.0		
$V_{PRE(L3)}$		$V_{OD} = V_{OD(L0)}$; BOOST = 01			9.5		
$V_{PRE(BOOST)}$	Output V_{PRE} Boost	BOOST = 10			+15		%dB
		BOOST = 00			–15		
$\Delta V_{PRE(L1L0)}$	Pre-emphasis Delta	Per PHY_CTS section 3.3 at TP2		2.0			dB
$\Delta V_{PRE(L2L1)}$				1.6			
$\Delta V_{PRE(L3L2)}$				1.6			
$\Delta V_{ConsBit}$	Non-transition bit voltage variation	Per PHY_CTS section 3.3.5				30	%V
R_{OUT}	Driver output impedance			40	50	60	Ω
$V_{OCM(SS)}$	Steady state output common mode voltage			0		2	V
$V_{OCM(PP)}$	Output common mode noise	Per PHY_CTS section 3.10	RBR, HBR		20		mV_{RMS}
			HBR2		30		
I_{OS}	Short circuit current limit	Main Link outputs shorted to GND				50	mA

7.8 HDMI/DVI Main Link Output Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Single-end high level output voltage	VSadj = 4.7 kΩ	V_{CC} –10		V_{CC} +10	mV
V_{OL}	Single-end low level output voltage	VSadj = 4.7 kΩ	V_{CC} –600		V_{CC} –400	mV
V_{SWING}	Single-end output voltage swing	VSadj = 4.7 kΩ; SDA_CTL/PRE ≤ V_{IL}	400		600	mV
ΔV_{SWING}	Change in single-end output voltage swing per 100Ω ΔVSadj			20		mV
$V_{OCM(SS)}$	Steady state output common mode voltage		V_{CC} –300		V_{CC} -200	mV
$\Delta V_{OCM(SS)}$	Change in steady state output common mode voltage between logic levels		–5		5	mV
$V_{OD(PP)}$	Peak-to-peak output differential voltage	VSadj = 4.7 kΩ; SDA_CTL/PRE ≤ V_{IL}	800		1200	mV_{PP}
		VSadj = 4.7 kΩ; SDA_CTL/PRE ≥ V_{IH}		640		
$V_{OD(SS)}$	Steady state output differential voltage	VSadj = 4.7 kΩ; SDA_CTL/PRE ≤ V_{IL}		1000		mV_{PP}
		VSadj = 4.7 kΩ; SDA_CTL/PRE ≥ V_{IH}		630		
I_{OS}	Short circuit current limit	V_{ID} = 500 mV			15	mA

7.9 HPD/CAD/EN Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	HPD_SNK, CAD_SNK	2.1			V
		EN	0.8			
V_{IL}	Low-level input voltage	HPD_SNK, CAD_SNK			1.08	V
		EN			0.285	
V_{OH}	High-level output voltage	I_{OH} = 500 µA; HPD_SRC, CAD_SRC	2.7		3.6	V
V_{OL}	Low-level output voltage	I_{OH} = 500 µA; HPD_SRC, CAD_SRC	0		0.1	V
R_{outCAD}	CAD series output resistance (1)	DP_HPD_SNK = CAD_SNK = V_{CC}		150		Ω
R_{outHPD}	HPD series output resistance	DP_HPD_SNK = TMDS_HPD_SNK = V_{CC}		150		Ω
I_{LEAK}	Failsafe condition leakage current	V_{CC} = 0 V; V(pin) = 1.2 V; EN			20	µA
		V_{CC} = 0 V; V(pin) = 3.3 V; DP_HPD_SNK, TMDS_HPD_SNK			40	
I_{H_HPD}	High level input current	Device powered; V_{IH} = 1.9 V; I_{H_HPD} includes R_{pdHPD} resistor current			30	µA
I_{H_CAD}					1	
I_{L_HPD}	Low level input current	Device powered; V_{IL} = 0.8 V; IL_HPD includes RpdHPD resistor current			30	µA
I_{L_CAD}					1	
R_{pdHPD}	HPD input termination to GND; DP_HPD_SNK and TMDS_HPD_SNK	V_{CC} = 0 V	100	130	160	kΩ
R_{EN}	EN terminal pull-up resistor		120	150	180	kΩ

7.10 AUX/DDC/I²C Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IO}	I/O capacitance	V_{IO} = 0 V; f(test) = 1 MHz		10		pF
r_{ON}	On resistance AUX_SRCn to AUX_SNKn in DP mode	V_{CC} = 3.0 V w/ V_I = 2.6 V or V_{CC} = 3.6 V w/ V_I = 3.4 V; I_O = 5 mA			10	Ω
	On resistance AUX_SRCp to AUX_SNKp in DP mode	V_{CC} = 3.0 V w/ V_I = 0.3 V or V_{CC} = 3.6 V w/ V_I = 0.4 V; I_O = 500 mA			10	Ω
	On resistance SCL/SDA_SRC to AUX_SNK in TMDS mode	V_I = 0.4 V; I_O = 3 mA			30	Ω
Δr_{ON}	On resistance variation with input signal voltage change in DP mode	V_{CC} = 3.6 V, I_O = 5 mA, V_I = 2.6 V to 3.4 V V_{CC} = 3.0 V, I_O = 5 mA, V_I = 0 V to 0.4 V			5	Ω
$V_{ID(HYS)}$	Differential input hysteresis	By design (simulation only)		50		mV
I_{LEAK}	Failsafe condition leakage current	V_{CC} = 0 V; V(pin) = 3.3 V; SCL/SDA_SNK			40	µA
		V_{CC} = 0 V; V(pin) = 3.3 V; AUX_SNK p/n			20	
		V_{CC} = 0 V; V(pin) = 3.3 V; SCL_CTL/EQ, SDA_CTL/PRE, AUX_SRCp			5	
		V_{CC} = 0 V; V(pin) = 3.3 V; AUX_SRCn, SCL/SDA_SRC			60	
$I_{H\_AUX\_DDC}$	AUX/DDC High level input current	Device powered; V_I = V_{CC}			5	µA
I_{H_I2C}	I²C High level input current				20	
I_{L_AUX}	AUX Low level input current	Device powered; V_I = GND ; I_{L_DDCSRC} includes R_{DDC} resistor current			5	µA
I_{L_I2C}	I²C Low level input current				40	
I_{L_DDCSRC}	DDC Low level input current				80	
V_{AUX+}	AUX_SNKp voltage	Per PHY_CTS section 3.19	0		0.4	V
V_{AUX-}	AUX_SNKn voltage	Per PHY_CTS section 3.18	2.4		3.6	V
S_{1122}	AC coupled AUX line insertion loss	V_{ID} = 400 mV, 360 MHz sine wave			3	dB
R_{DDC}	Switchable pullup resistor on DDC at source side (SCL_DDC, SDA_DDC)	CAD_SNK = V_{IH}	48	60	72	kΩ
V_{IL1}	SCL/SDA_SRC low-level input voltage	OVS ≥ V_{IH}			0.4	V
V_{IL2}		OVS at V_{IM}			0.4	
V_{IL3}		OVS ≤ V_{IL}			0.3	
V_{OL1}	SCL/SDA_SRC low-level output voltage	OVS ≥ V_{IH}	0.6		0.7	V
V_{OL2}		OVS at V_{IM}	0.5		0.6	
V_{OL3}		OVS ≤ V_{IL}	0.4		0.5	
V_{OL4}	SCL/SDA_SNK and SCL/SDA_CTL low-level output voltage	I_O = 3 mA			0.4	V

7.11 DisplayPort Main Link Output Switching Characteristics

over recommended operating conditions (unless otherwise noted) Figure 1 and Figure 2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay time			350		ps
t_{SK1}	Intra-pair output skew	Signal input skew = 0 ps; dR = 2.7 Gbps, V_{PRE} = 0 dB, 800 mVpp , D10.2 clock pattern at device input; see Figure 2			20	ps
t_{SK2}	Inter-pair output skew				70	ps
Δt_{jit}	Total peak to peak residual jitter	V_{OD}(L0); VPRE(L0); EQ = 8 dB; clean source; minimum input and output cabling; 1.62 Gbps, 2.7 Gbps, and 5.4-Gbps PRBS7 data pattern.			15	ps
t_{sq_enter}	Squelch Entry Time	Time from active DP signal turned off to ML output off with noise floor minimized	10		120	µs
t_{sq_exit}	Squelch Exit Time	Time from DP signal on to ML output on	0		1	µs

7.12 HDMI/DVI Main Link Switching Characteristics

over recommended operating conditions (unless otherwise noted) Figure 3, Figure 4, and Figure 5

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time (low to high)		250		600	ps
t_{PHL}	Propagation delay time (high to low)		250		800	ps
t_{T1}	Transition time (rise and fall time); measured at 20% and 80% levels	SRC ≤ V_{IL}; SDA_CTL/PRE ≤ V_{IL}; 340 MHz	75		140	ps
t_{T2}		SRC at V_{IM}; SDA_CTL/PRE ≤ V_{IL}; 340 MHz	85		160	
t_{T3}		SRC ≥ V_{IH}; SDA_CTL/PRE ≤ V_{IL}; 340 MHz	100		200	
$t_{SK1(T)}$	Intra-pair output skew				0.15t_{bit}	ps
$t_{SK2(T)}$	Inter-pair output skew				30	ps
Δt_{JIT}	Total peak to peak residual jitter; clock and data lanes	SRC at V_{IM}; d_R = 3.4 Gbps; 0 dB V_{PRE}; EQ = 13 dB			30	ps
t_{sq_enter}	Squelch Entry Time	d_R = 3.4 Gbps	10		120	µs
t_{sq_exit}	Squelch Exit Time		0		1	

7.13 HPD/CAD Switching Characteristics

over recommended operating conditions (unless otherwise noted) Figure 6

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(HPD)}$	Propagation delay DP/TMDS_HPD_SNK to HPD_SRC; rising edge and falling edge	See Figure 7; not valid during switching time $t_{S(HPD)}$			120	ns
$t_{PD(CAD)}$	Propagation delay CAD_SNK to CAD_SRC; rising edge and falling edge	See Figure 10			50	ns
$t_{SK(HPD\_CAD)}$	Output skew HPD_SRC to CAD_SRC when HDMI/DVI sink is selected; rising edge and falling edge	See Figure 10			50	ns
$t_{T(HPD1)}$	HPD logic switch time	See Figure 8		350		ms
$t_{T(HPD2)}$	HPD logic switch pause time	See Figure 8		4.1		ms
$t_{T(HPD3)}$	HPD logical disconnect timeout	See Figure 9		350		ms

7.14 AUX/DDC/I²C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{sk(AUX)}$	AUX intra-pair skew	V_{ID} = 400 mV, see Figure 11			400	ps
$t_{PLH(AUX)}$	AUX propagation delay, low to high	CAD_SNK ≤ V_{IL}; 1-Mbps pattern; see Figure 12			3	ns
$t_{PHL(AUX)}$	AUX propagation delay, high to low				3	ns
$t_{PLH1(DDC)}$	DDC propagation delay, low to high(1)	Source to Sink; CAD_SNK ≥ V_{IH}; 100-kbps pattern; C_L (Sink) = 400 pF; see Figure 13		360		ns
$t_{PHL1(DDC)}$	DDC propagation delay, high to low(1)			230		ns
$t_{PLH2(DDC)}$	DDC propagation delay, low to high(1)	Sink to Source; CAD_SNK ≥ V_{IH}; 100-kbps pattern; C_L (Source) = 100 pF; see Figure 14		250		ns
$t_{PHL2(DDC)}$	DDC propagation delay, high to low(1)			200		ns
$t_{PU(AUX)}$	Main link D3 wakeup time	V_{ID} = 0.1 V, V_{ICM} = 2 V source side (before AC coupling caps)			50	µs
Local I²C						
Refer to the I²C-Bus Specification, Version 2.1 (January 2000); SN75DP126 meets the switching characteristics for standard mode transfers up to 100 kbps.						

(1) Applies to DDC pass through to DisplayPort sink and the HDMI/DVI sink.

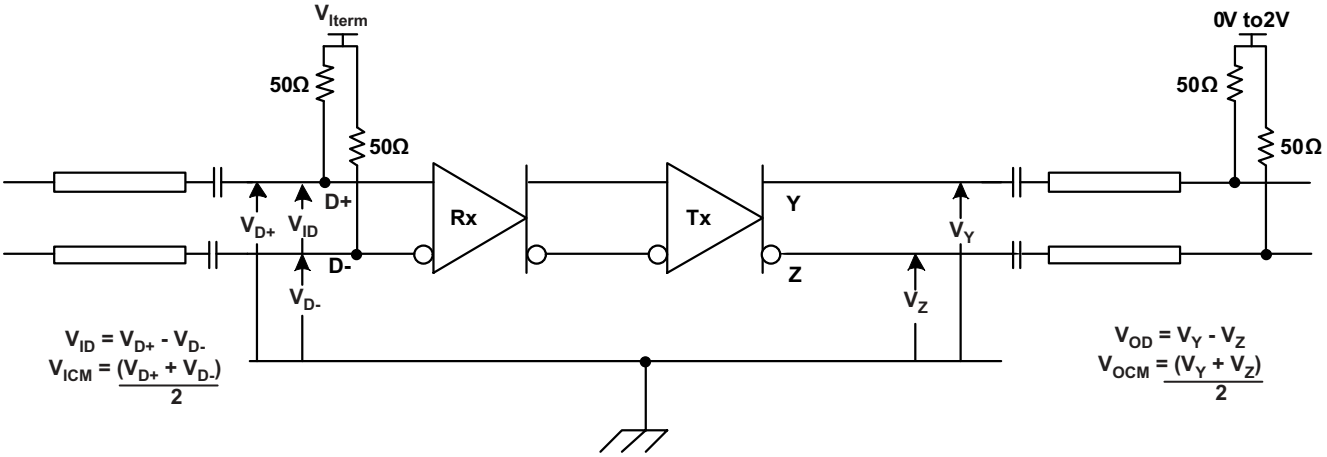


Figure 1. DisplayPort Sink Main Link Test Circuit

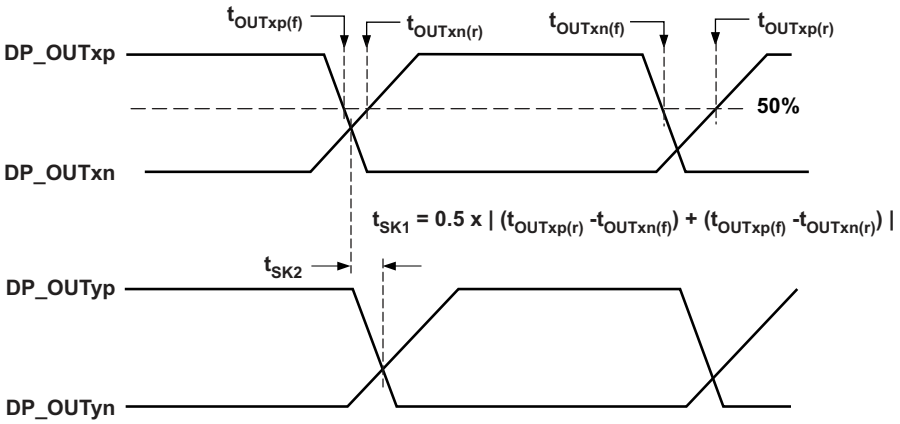


Figure 2. DisplayPort Sink Main Link Skew Measurements

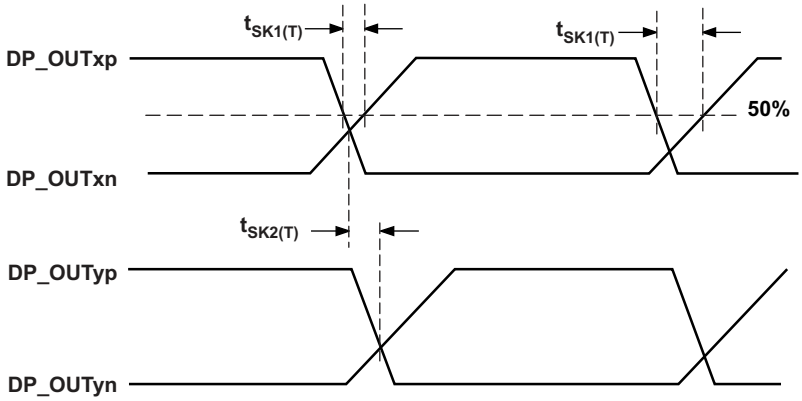


Figure 3. HDMI/DVI Sink TMDS Output Skew Measurements

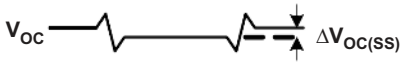
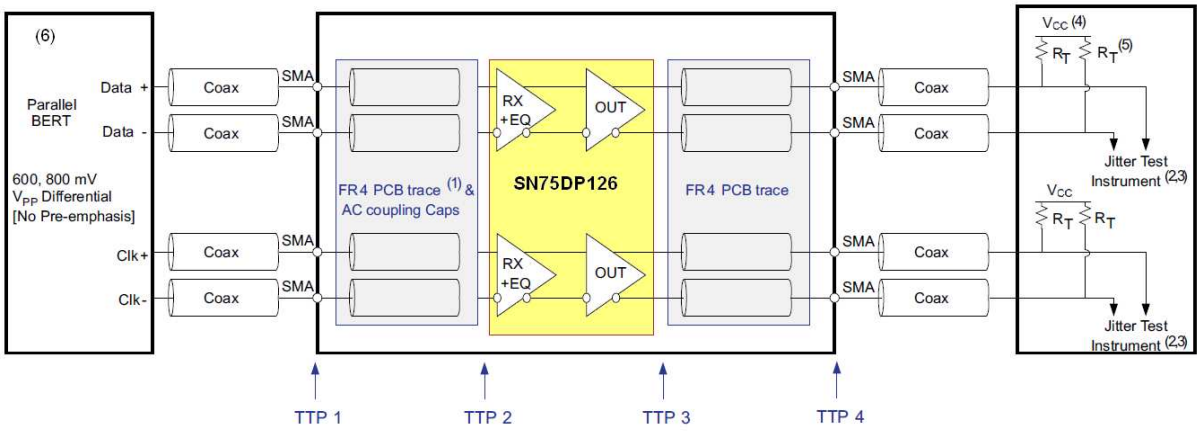


Figure 4. HDMI/DVI TMDS Output Common Mode Measurement



(1) The FR4 trace between TTP1 and TTP2 is designed to emulate 1-8" of FR4, AC coupling cap and connector. Trace width –4 mils.

(2) All Jitter is measured at a BER of 10^{-9}

(3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1

(4) V_{CC} = 3.3 V

(5) RT = 50Ω

(6) The input signal from parallel Bert does not have any pre-emphasis. Refer to recommended operating conditions.

Figure 5. HDMI/DVI TMDS Output Jitter Measurement

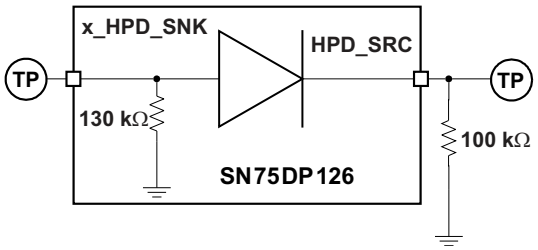


Figure 6. HPD Test Circuit

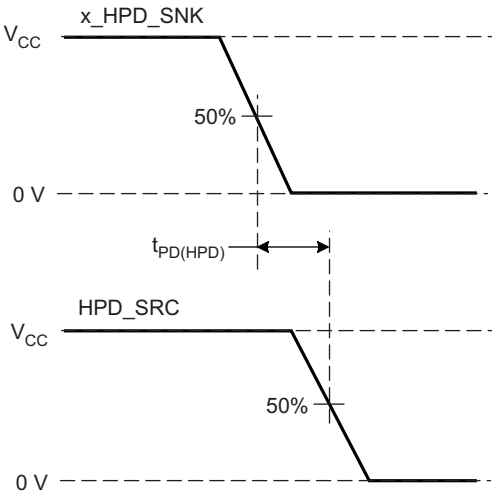


Figure 7. HPD Timing Diagram #1

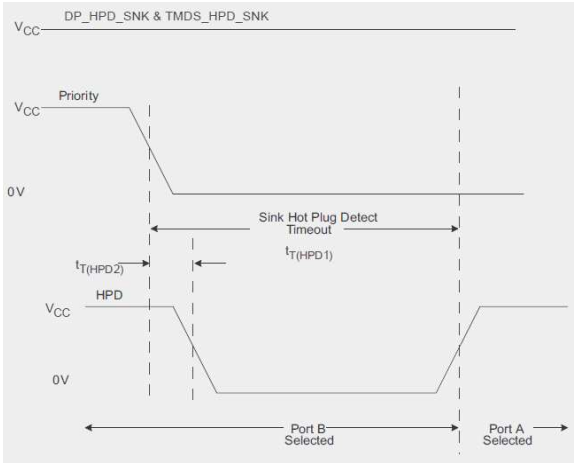


Figure 8. HPD Timing Diagram #2

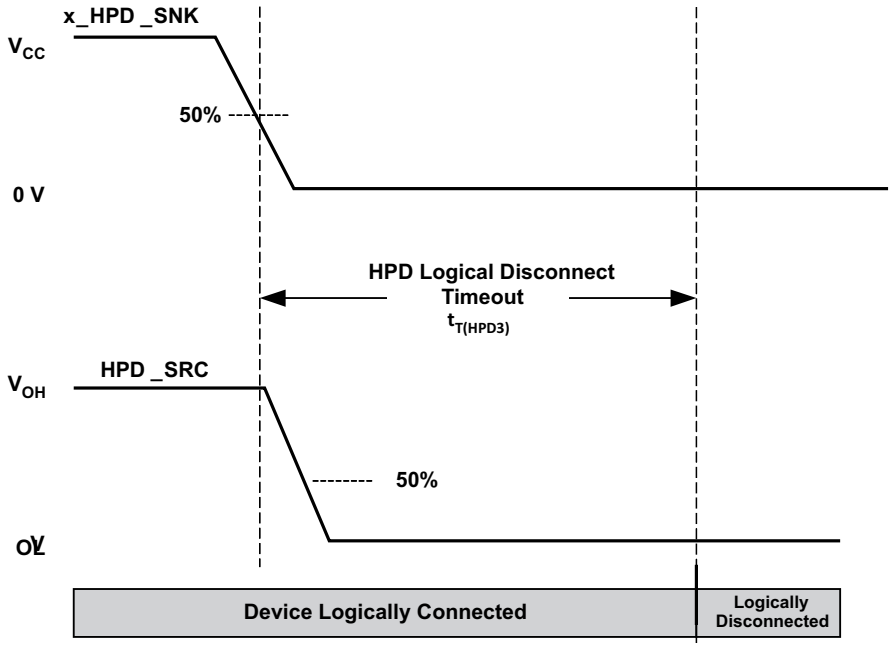


Figure 9. HPD Logic Disconnect Timeout

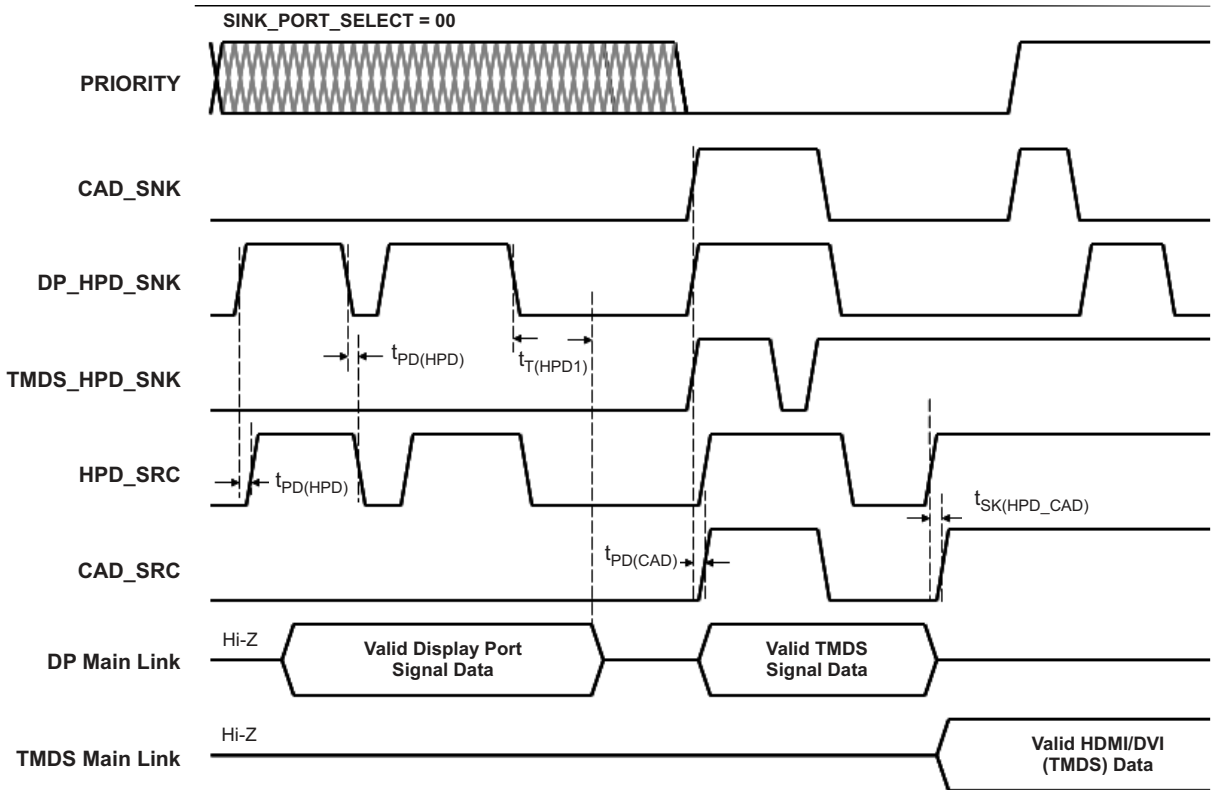


Figure 10. HPD and CAD Logic Description and Timing Diagram

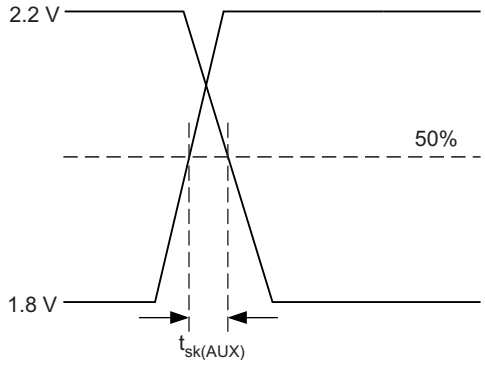


Figure 11. AUX Skew Measurement

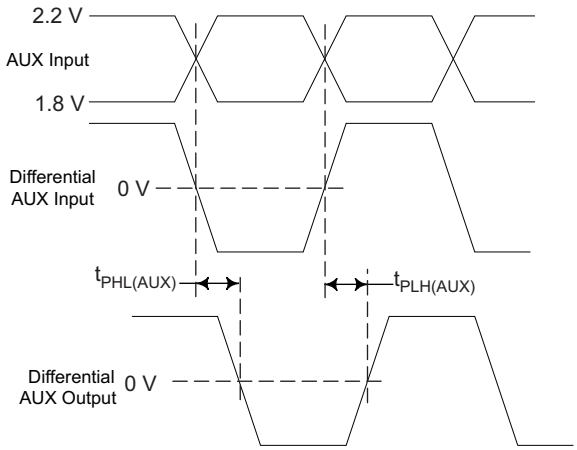


Figure 12. AUX Delay Measurement

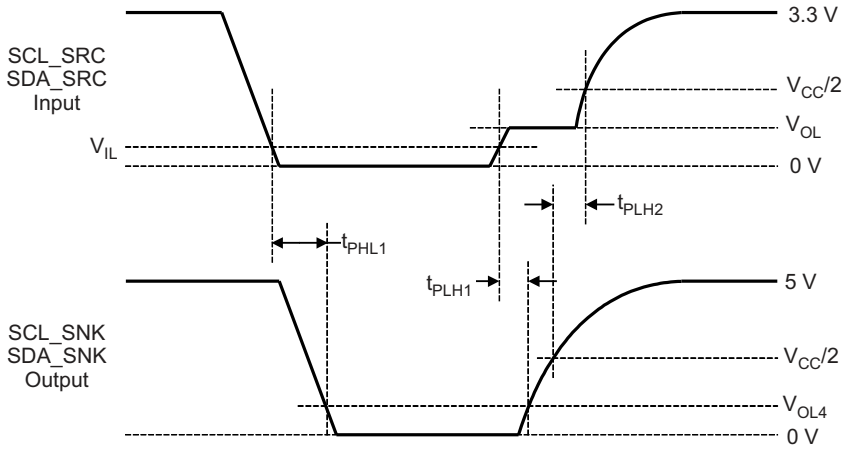


Figure 13. DDC Propagation Delay – Source to Sink

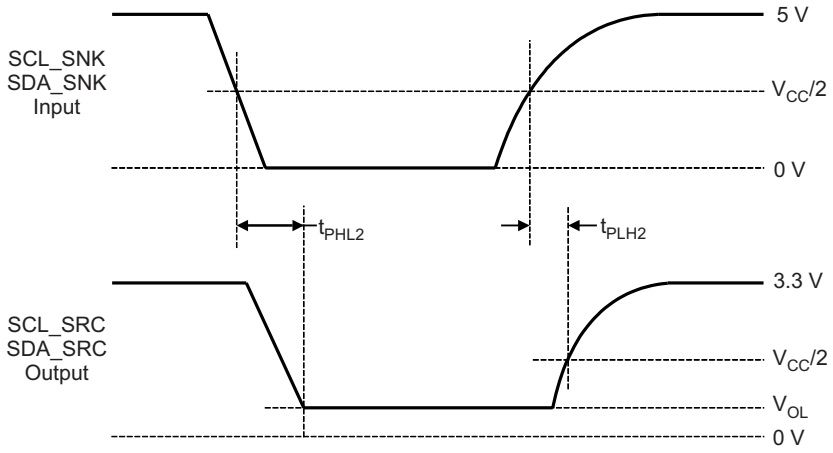


Figure 14. DDC Propagation Delay – Sink to Source

7.15 Typical Characteristics

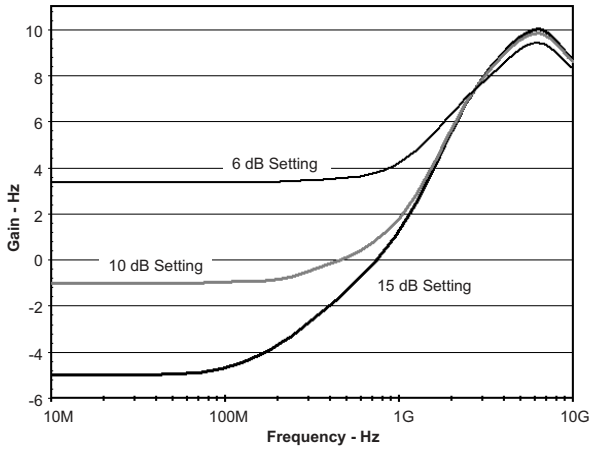
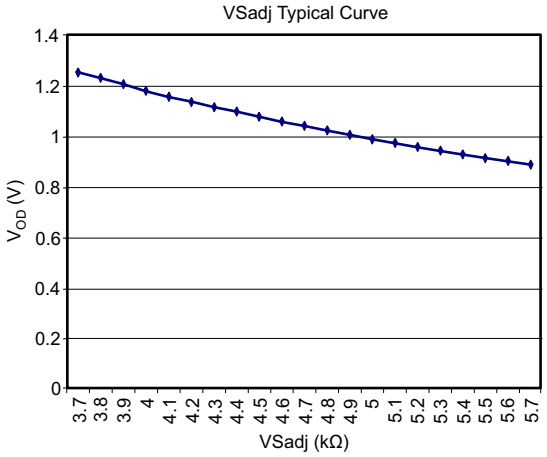


Figure 15. Typical EQ Gain Curves

Input Mode	Trace Length (inches)	Recommended Fixed EQ Setting
DisplayPort HBR2	2	10dB
	6	10dB
	10	10dB
	14	13dB
	18	15dB
	22	15dB
TMDS 3.4 Gbps	2	13dB
	6	13dB
	10	13dB
	14	13dB
	18	15dB
	22	15dB

Figure 16. Characterization Test Board Trace Lengths vs EQ Setting



Gain represents SN75DP126 design simulation.

Figure 17. V_{OD} vs. VSadj

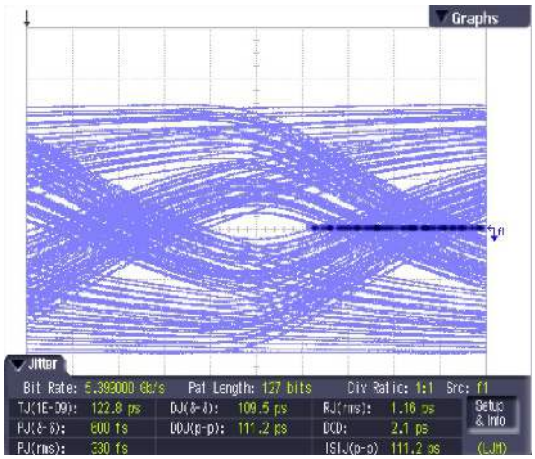


Figure 18. Main Link Input with 22-inch Trace; DisplayPort Sink

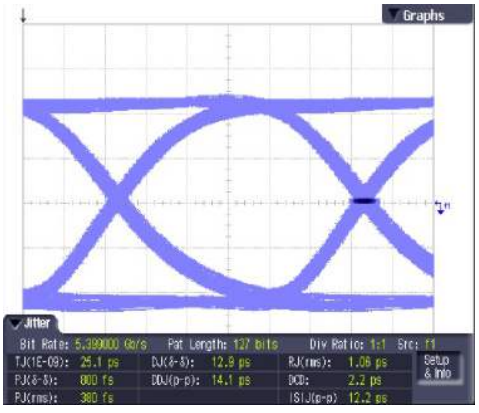


Figure 19. SN75DP126 Output; 22-inch Input Trace; 15 dB EQ Setting; DP Sink

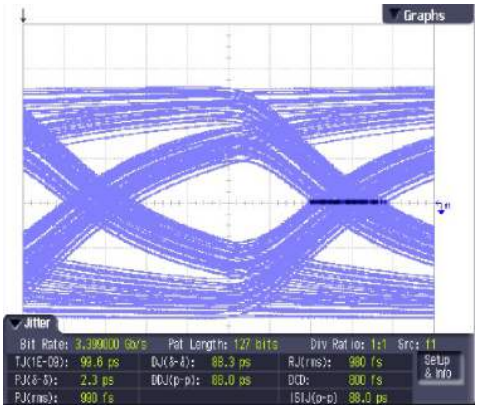


Figure 20. Main Link Input with 22-inch Trace; TMDS Sink

Typical Characteristics (continued)

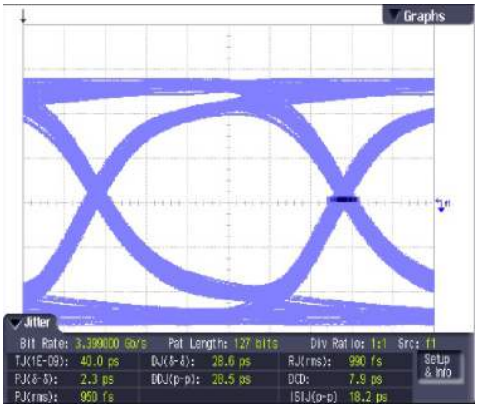


Figure 21. SN75DP126 Output; 22-inch Input Trace; 15 dB EQ Setting; TMDS Sink

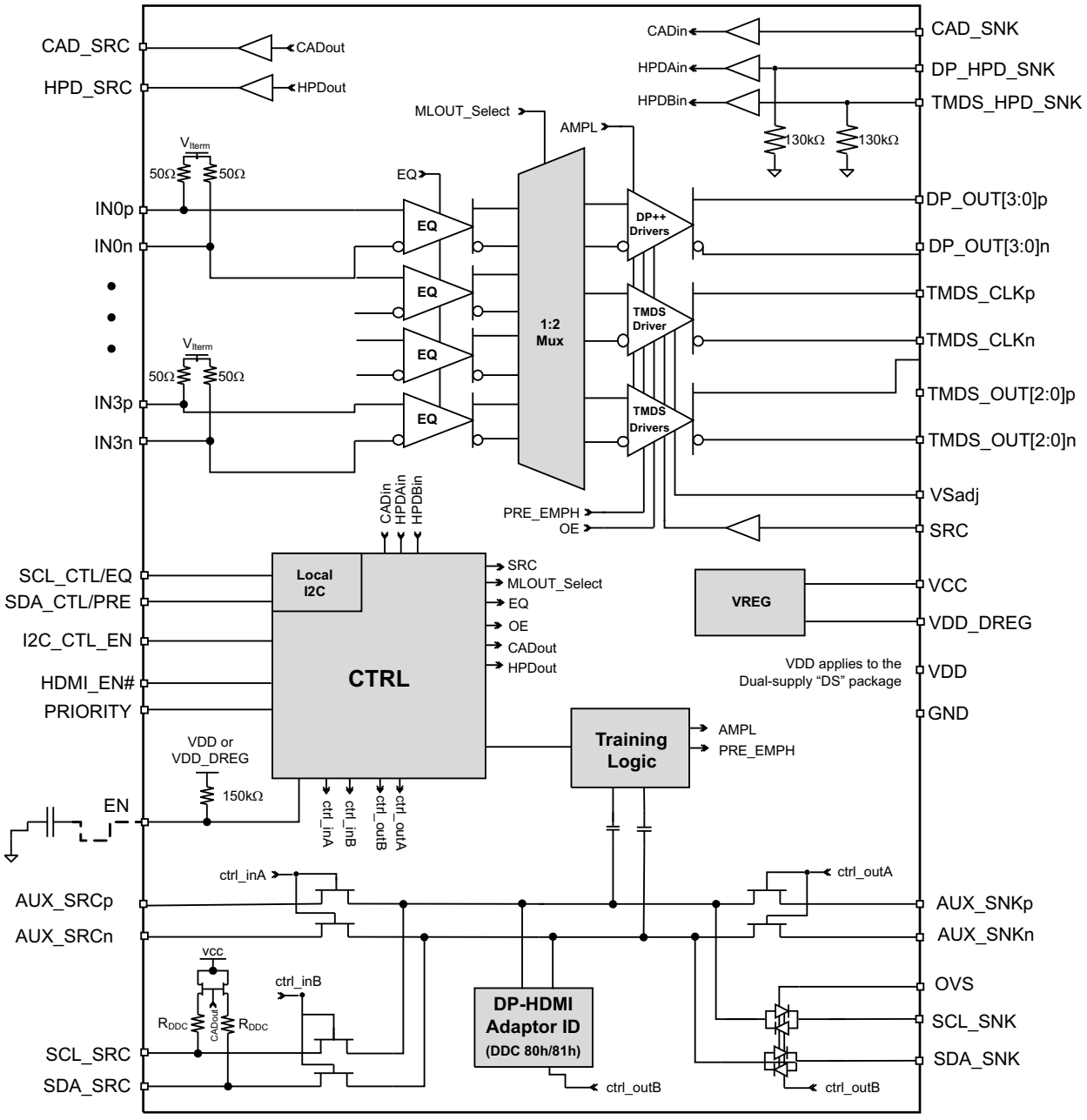
8 Detailed Description

8.1 Overview

The SN75DP126 compensates for PCB related frequency loss and switching related loss to provide the optimum electrical performance from source to SINK. THE DP++ main link signal inputs feature configurable equalizers with selectable boost settings.

The SN75DP126 switches one dual-mode Displayport (DP++) input to one Dual-mode Displayport (DP++) sink output or one HDMI/DVI sink outpuT. The HDMI/DVI output has a built in level translator compliant with DVI 1.0 and HDMI 1.4A standard TMDS signaling, and is specified up to a maximum data rate of 3.5GBPS, supporting resolutions greater than 1920 × 1440 and HDTV deep color at 1080P. An integrated DP-HDMI adaptor ID buffer can be accessed when the HDMI/DVI sink is selected to indicate support for HDMI signaling.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Implementing the EN Signal

The SN75DP126 EN input gives control over the device reset and to place the device into Shutdown mode. When EN is low, all DPCD and local I^2C registers are reset to their default values, and all Main Link lanes are disabled.

It is critical to reset the digital logic of the SN75DP126 after the V_{CC} supply (and V_{DD} supply for SN75DP126DS) is stable (that is, the power supply has reached the minimum recommended operating voltage). To reset the digital logic, transition the EN input from a low level to a high level. This method is shown in Figure 22. A system may provide a control signal to the EN signal that transitions low to high after the power supply is (or supplies are) stable. An alternate implementation is to use an external capacitor connected between EN and GND to allow delaying the EN signal during power up, as shown in Figure 23.

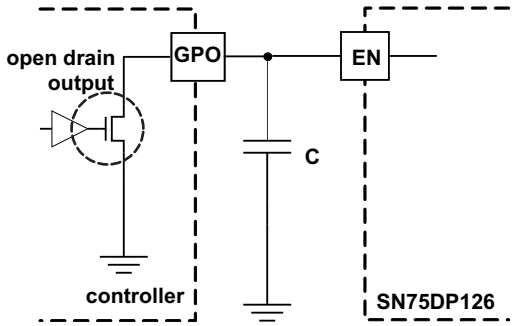


Figure 22. EN Input from Active Controller

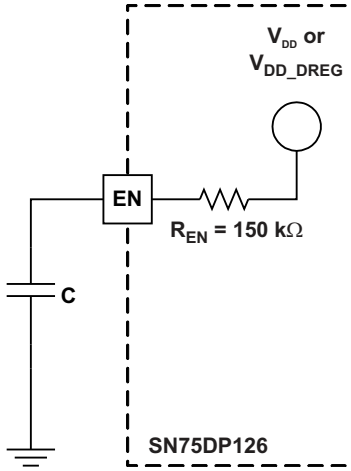


Figure 23. External Capacitor Controlled EN

When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V_{CC} (and V_{DD} when applicable) supply, where a slower ramp-up results in a larger value external capacitor.

Refer to the latest reference schematic for the SN75DP126 device and/or consider approximately 200nF capacitor as a reasonable first estimate for the size of the external capacitor.

When implementing an EN input from an active controller, it is recommended to use an open drain driver if the EN input is driven. This protects the EN input from damage of an input voltage greater than V_{DD_DREG} (or V_{DD}).

8.3.2 Hot Plug Detect (HPD) and Cable Adapter Detect (CAD) Description

The SN75DP126 drives the source-side Hot Plug Detect (HPD_SRC) signal output high to indicate to the GPU or graphics source that at least one sink has been detected and selected for connectivity; when no sink is selected the HPD_SRC is driven low. A high-level DP_HPD_SNK input indicates a DisplayPort sink device is connected, and a high-level TMDS_HPD_SNK input indicates a HDMI/DVI sink device is connected.

When DP_HPD_SNK is high, the DisplayPort sink is selected if the TMDS_HPD_SNK input is low. When TMDS_HPD_SNK is high, the HDMI/DVI sink is selected if the DP_HPD_SNK input is low. If both DP_HPD_SNK and TMDS_HPD_SNK inputs are high, then the PRIORITY input determines which sink is selected.

When the DisplayPort sink is selected, the CAD_SNK input indicates whether a DP sink (CAD_SNK = low) or a TMDS sink (CAD_SNK = high) is connected. The level of CAD_SNK is passed to the CAD_SRC output when the DisplayPort sink is selected. When the HDMI/DVI sink is selected, the CAD_SRC output is driven high regardless of the value input on CAD_SRC.

A sink is determined to be disconnected when the corresponding HPD_SNK input goes low for a duration of $t_{T(HPD)}$. When switching from one sink to the other based on the PRIORITY selection, that is, both sinks are connected and either PRIORITY has changed or the sink with higher PRIORITY was connected after the sink with lower PRIORITY, the SN75DP126 asserts HPD_SRC for a duration at least $t_{T(HPD)}$ before the switchover connection is established.

Through the local I^2C interface it is possible to force the device to ignore DP_HPD_SNK, TMDS_HPD_SNK, and CAD_SNK, and control HPD_SRC and CAD_SRC directly.

When the EN pin is de-asserted (device is in power down mode), the HPD path from DP_HPD_SNK and/or TMDS_HPD_SNK to HPD_SRC is not reset. As a result, the source may need to retrain the link once EN is asserted (device is in active mode).

See Figure 10 and Table 1 for more information about the HPD and CAD functions.

8.3.3 OVS Function Description

The SN75DP126 provides an output-voltage select (OVS) control for the source side buffers on the DDC I^2C lines. When the sink side is driven low, the corresponding source side driver turns on and drives the source side down to a low-level output voltage, V_{OL}. The value of V_{OL} and V_{IL} on the source side of the SN75DP126 depends on setting of the OVS pin. V_{OL} is always higher than V_{IL} on the source side to prevent lockup of the buffers on the DDC I^2C lines. When the sink side is pulled up, the source side driver turns off and the sink side pin is high-impedance.

When the source side is driven below V_{IL} by an external I^2C driver, both the sink and source side drivers are turned on. The sink side driver drives the sink side to near 0V, and the source side driver is on, but is overridden by the external I^2C driver. When the source side is released by the external I^2C driver, the source side driver is still on, so the source side is only able to rise to V_{OL}. However, the sink side driver turns off because the source side is above the V_{IL} threshold. If no external I^2C driver is keeping the sink side low, the sink side rises causing the source side driver to turn off. See Figure 13 and Figure 14 for more information.

It is important that any external I^2C driver on the source side is able to drive the bus below V_{IL} to achieve full operation. If the source side cannot be driven below V_{IL}, the sink side driver may not recognize and transmit the low value to the sink side.

8.3.4 AUX and DDC Configuration Details

The SN75DP126 connectivity between source-side AUX and DDC channels and the sink-side AUX and DDC channels is described in Table 3. Refer to the BLOCK DIAGRAM for more information about the AUX and DDC switches, buffers, and logic elements represented in Table 1.

Note that the DDC interface incorporates 60kΩ pull-up resistors on SDA_SRC and SCL_SRC which are enabled when CAD_SRC is driven high, and disabled (turned off) when CAD_SRC is driven low.

Table 1. AUX and DDC Switch, Buffers, and Logic Element Control

INPUTS				OUTPUTS AND CONTROLS							
TMDS_HPD_SNK	DP_HPD_SNK	PRIORITY	CAD_SNK	CAD_SRC (Source-Side Output)	AUX_SRC SWITCH	DDC_SRC SWITCH	DP AUX_SNK SWITCH	HDMI/DVI DDC LEVEL-SHIFTI I/O BUFFERS	AUX MONITOR (Link Training)	14DP-HDMI ADAPTOR ID12 (1580h/81h DDC Buffer)	COMMENTS
0	0	X	0	0 (1)	OFF	OFF	OFF	OFF	OFF	OFF	no sink selected; low power mode
			1	1 (1)							
0	1	X	0	0	ON	OFF	ON	OFF	ON	OFF	DisplayPort sink selected; operating in DP mode; AUX_SNK connects to AUX_SRC and Link Training enabled
1	1	0									
0	1	X	1	1	OFF	ON	ON	OFF	OFF	OFF	DisplayPort sink selected; operating in TMDS mode; AUX_SNK connects to source-side DDC (SCL/SDA_SRC)
1	1	0									
1	0	X	X	1	OFF	ON	OFF	ON	OFF	ON	HDMI/DVI sink selected; connect the source-side DDC to sink-side DDC; enable the DP-HDMI Adaptor ID accessed via DDC addresses 80h/81h
1	1	1									

(1) After transitioning from HDMI/DVI mode to low power mode, CAD_SRC will remain high regardless of the status of CAD_SNK

8.3.5 Source-Side Main Link EQ Configuration Details

A variety of EQ settings are available through external pin configuration to accommodate for different PCB loss and GPU settings. The I^2C interface is utilized to fully customize EQ configuration, lane-by-lane, beyond the input pin configuration options, as described in Table 2.

Table 2. Source-Side Main Link EQ Configurations

INPUTS								EQ SETTINGS		
EQ_I2C_ENABLE	(Register 05.7)	I2C_CTL_EN	(3-Level Input)	SCL_CTL/EQ	(3-Level Input)	LINK_TRAINING_ENABLE	(Register 04.2)	DISPLAYPORT SIGNAL MODE(1)(2) SOURCE LANES IN[3:0]	TMDS SIGNAL MODE(3) (TMDS DATA) SOURCE LANES IN[2:0]	TMDS SIGNAL MODE(3) (TMDS CLOCK) SOURCE LANE IN[3]
0		≤ V_{IL}		≤ V_{IL}		1		AEQ(L0) = 8 dB at 2.7 GHz AEQ(L1) = 6 dB at 2.7 GHz AEQ(L2) = 3.5 dB at 2.7 GHz AEQ(L3) = 0 dB at 2.7 GHz	6 dB at 2.7 GHz	3 dB at 1.35 GHz
						0		6 dB at 2.7 GHz		
				V_{IM}		X		6 dB at 2.7 GHz	6 dB at 2.7 GHz	3 dB at 1.35 GHz
				≥ V_{IH}				13 dB at 2.7GHz	13 dB at 2.7 GHz	3 dB at 1.35 GHz
		V_{IM}		X		1		AEQ(L0) = 15 dB at 2.7 GHz AEQ(L1) = 13 dB at 2.7 GHz AEQ(L2) = 10 dB at 2.7 GHz AEQ(L3) = 6 dB at 2.7 GHz	13 dB at 2.7 GHz	3 dB at 1.35 GHz
						0		13 dB at 2.7 GHz		
		≥ V_{IH}				X		18 dB at 2.7 GHz	18 dB at 2.7 GHz	3 dB at 1.35 GHz
1		V_{IM} or ≥ V_{IH}		X		1		AEQ(Lx) = 0 dB at 2.7 GHz (default) EQ settings for each link training level can be selected via local I^2C	0 dB at 2.7 GHz (default) EQ settings selected via local I^2C, training level L1 (AEQ_L1_LANEx_SET registers)	3 dB at 1.35 GHz
						0		0 dB at 2.7 GHz (default) EQ settings selected via local I^2C; training level L1 (AEQ_L1_LANEx_SET registers)	0 dB at 2.7 GHz (default) EQ settings selected via local I^2C; training level L1 (AEQ_L1_LANEx_SET registers)	3 dB at 1.35 GHz

(1) DisplayPort mode is active when the DisplayPort sink is selected and the CAD_SNK input is low
(2) In DisplayPort signaling mode, the EQ gain may be applied after the Link Training is complete
(3) TMDS mode is active when the DisplayPort sink is selected and the CAD_SNK input is high, or when the HDMI/DVI sink is selected

8.3.6 DP-HDMI Adaptor ID Buffer

The SN75DP126 includes the DP-HDMI adapter ID buffer for HDMI/DVI adaptor recognition, defined by the VESA DisplayPort Interoperability Guidelines Version 1.1a, accessible by standard I^2C protocols through the DDC interface when the HDMI/DVI sink is selected. The DP-HDMI adapter buffer is accessed at target addresses 80h (Write) and 81h (Read).

The DP-HDMI adapter buffer contains a read-only phrase DP-HDMI ADAPTOR<EOT> converted to ASCII characters as illustrated in Table 3, and supports the Write command procedures (accessed at target address 80h) to select the sub-address, as recommended in the VESA DisplayPort Interoperability Guideline Adaptor Checklist Version 1.0 section 2.3.

Table 3. SN75DP126 DP-HDMI Adaptor ID Buffer

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	0x10
Data	44	50	2D	48	44	4D	49	20	41	44	41	50	54	4F	52	04	FF

8.3.7 GPU with a Unified AUX/DDC Configuration

The SN75DP126 supports graphics processors with unified AUX/DDC configurations, where the source AUX channel is multiplexed with the source DDC channel, as illustrated in Figure 24.

Graphics processors with separate AUX and DDC channels (ie. non-unified) are also supported, where the separate channels are directly routed to the separate channels on the SN75DP126, maintaining the AC coupling on the AUX channel. In the non-unified configuration, it is recommended to implement 2-kΩ pull-up resistors on the source-side DDC channel. See Figure 25.

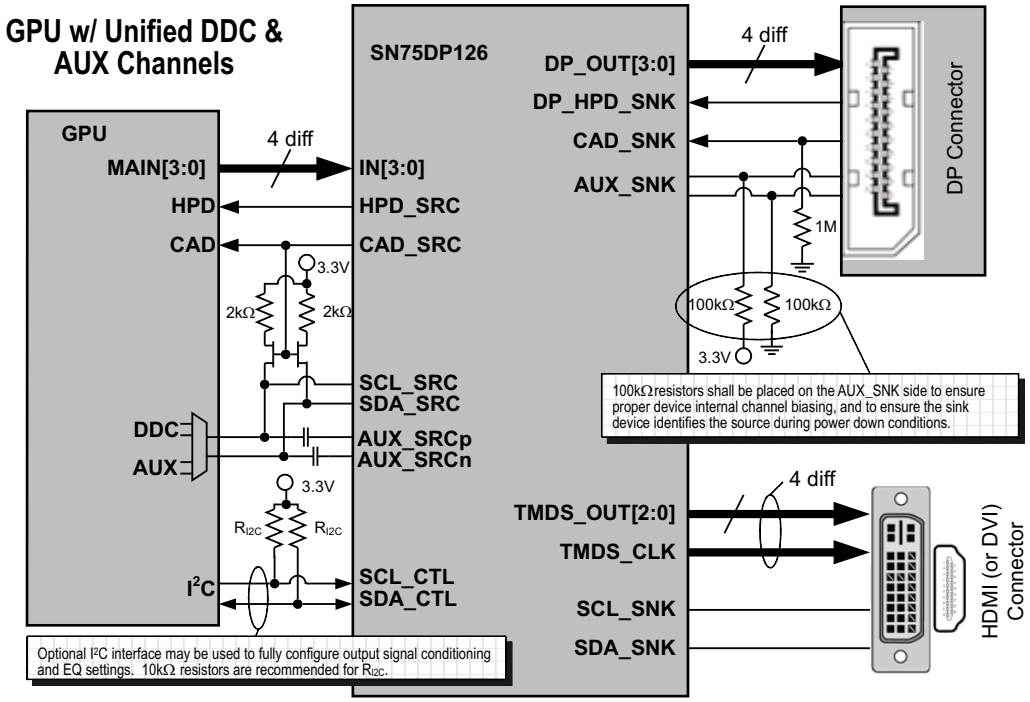


Figure 24. GPU with a Unified AUX/DDC Configuration

8.3.8 GPU with Separate DDC and AUX Channels

Graphics processors with separate AUX and DDC channels (ie. non-unified) are also supported, where the separate channels are directly routed to the separate channels on the SN75DP126, maintaining the AC coupling on the AUX channel. In the non-unified configuration, it is recommended to implement 2-kΩ pull-up resistors on the source-side DDC channel. See Figure 25.

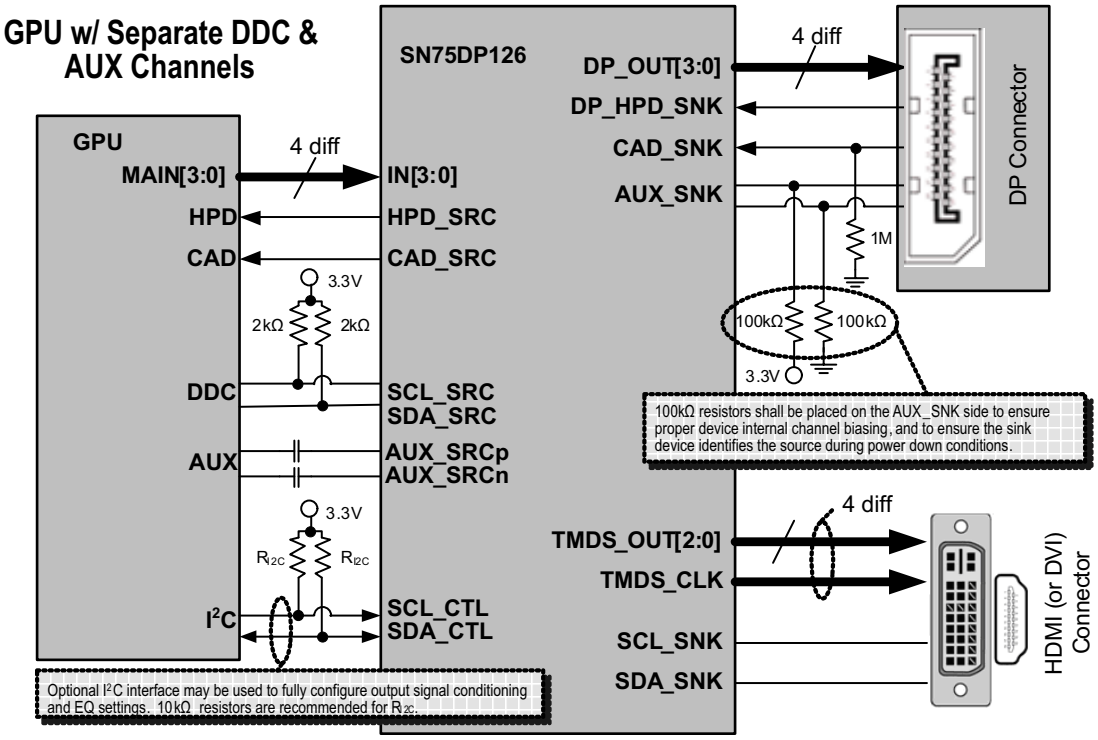


Figure 25. GPU with Separate DDC and AUX Channels

8.4 Device Functional Modes

8.4.1 Operating Modes Overview

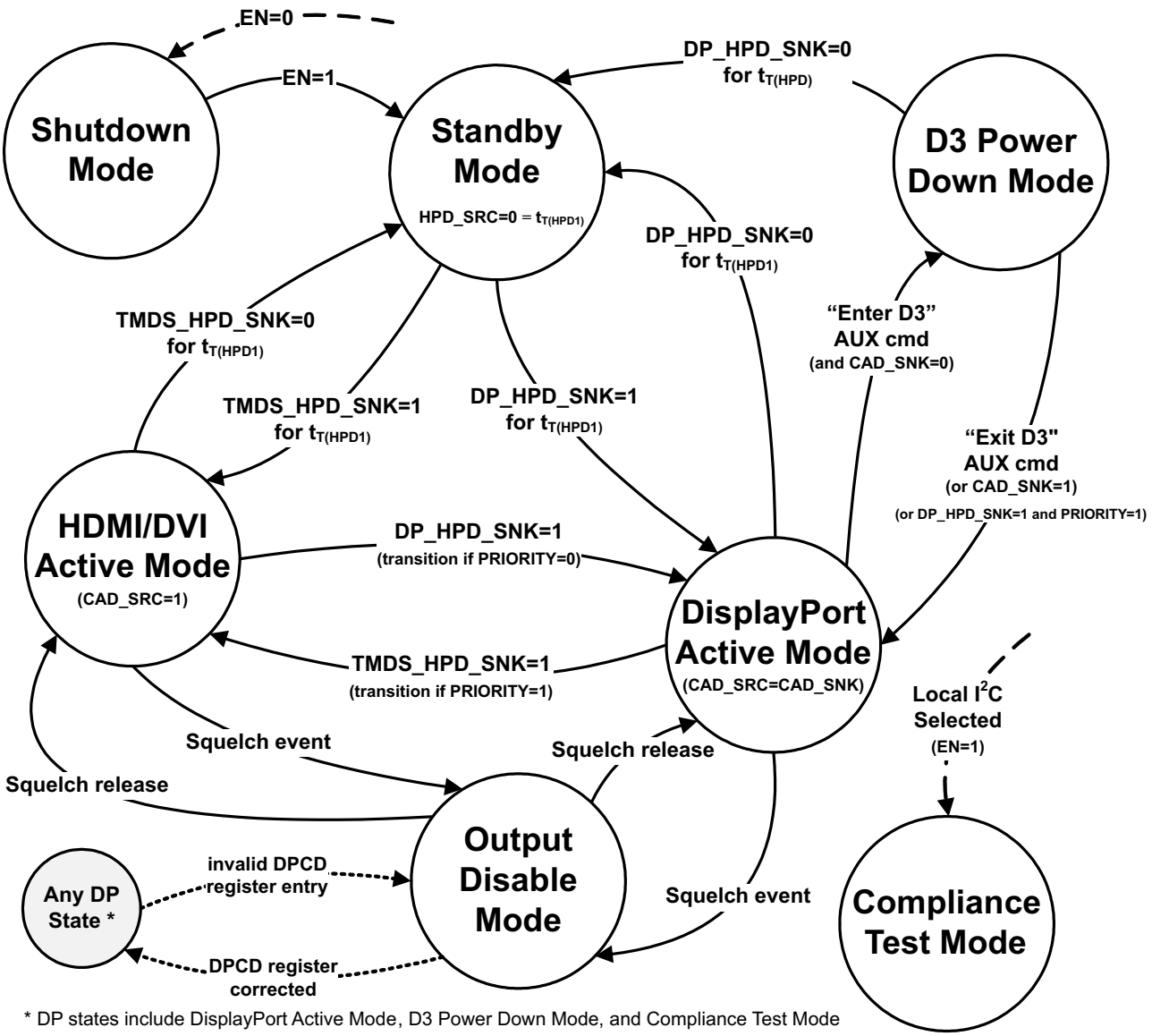


Figure 26. SN75DP126 Operating Modes Flow Diagram

Device Functional Modes (continued)

Table 4. Description of SN75DP126 Operating Modes

MODE	CHARACTERISTICS	CONDITIONS
Shutdown Mode	Least amount of power consumption (most circuitry turned off); HPD_SRC output is asserted if either DP_HPD_SNK or TMDS_HPD_SNK are input active (high); all other outputs are high-impedance; all other inputs are ignored; the local I^2C interface is inactive; in this state all local I^2C registers and DPCD registers are set to default values.	EN is low
Standby Mode	Main Link outputs are disabled; the local I^2C interface is active; in this state, the HPD_SRC (and CAD_SRC) outputs are driven low for at least $t_{T(HPD)}$ to indicate no sink connectivity to the source; the SN75DP126 passes through this state when transitioning from one active sink to the other for reasons of PRIORITY selection, where the HPD_SRC de-assertion for at least $t_{T(HPD)}$ communicates the sink plug event to the source.	EN is high; Either no sink is connected, or both sinks are connected and PRIORITY causes a transition from one sink to the other sink
DisplayPort Active Mode	The DisplayPort sink is selected and data transfer is enabled (normal operation); the Main Link output is either TMDS mode (CAD_SNK = 1) or DisplayPort mode (CAD_SNK = 0).	EN is high; DP_HPD_SNK is high, but after entering this state, DP_HPD_SNK can be low for less than tT(HPD) (for example, sink interrupt request to source); If both TMDS_HPD_SNK and DP_HPD_SNK are high, then a low input on PRIORITY causes the DisplayPort sink selection
	In TMDS mode, the DDC source-side channel (SCL/SDA_SRC) is connected to the sink DDC channel (AUX_SNK p/n) through a low-resistance circuit; and the CAD_SRC output is driven high. In TMDS mode the output signal swing is 600 mVpp unless this setting is adjusted through local I^2C interface programming; the Main Link input equalizer settings depend on device control inputs and local I^2C settings.	
	In DisplayPort mode the AUX source-side channel is connected to the sink AUX channel through a low-resistance circuit; and the CAD_SRC output is driven low. The AUX monitor is active for Link Training, which automatically updates the DPCD registers to enable the Main Link outputs (this Link Training operation may be de-activated and overridden by direct local I^2C programming); transactions other than Link Training and D3 power management commands are ignored on the AUX interface; the Main Link output signal conditioning (pre-emphasis and V_{OD}) and Main Link input equalizer settings depend on the Link Training, device control inputs, and local I^2C settings.	
D3 Power Down Mode	DisplayPort D3 low-power mode; DisplayPort sink Main Link outputs are disabled; local I^2C interface is active; AUX monitor is active.	EN is high; DisplayPort sink is selected, and operating in DisplayPort mode (CAD_SNK = 0); “Enter D3” AUX command has been performed
HDMI/DVI Active Mode	The HDMI/DVI sink is selected and data transfer is enabled (normal operation); the HDMI/DVI Main Link output (TMDS signaling) is enabled.	EN is high; TMDS_HPD_SNK is high; If both TMDS_HPD_SNK and DP_HPD_SNK are high, then a high input on PRIORITY causes the HDMI/DVI sink selection
	The DDC source-side channel (SCL/SDA_SRC) is connected to the HDMI/DVI sink DDC channel (SCL/SDA_SNK) through an I^2C buffer that separates the capacitive load between the source and sink; the DP-HDMI Adapter ID buffer containing a read-only phrase DP-HDMI ADAPTOR<EOT> converted to ASCII characters at DDC (I^2C target) addresses 80h(Write)/81h(Read) per the VESA DisplayPort Interoperability Guidelines Version 1.1a	
	The HDMI/DVI Main Link output signal conditioning (pre-emphasis and V_{OD}) and Main Link input equalizer settings depend on the device control inputs and local I^2C settings.	
Output Disable Mode	When low-signal levels on the source Main Link input are sensed (a squelch event) when in either sink-side is selected for active mode, a transition to this state occurs and the sink-side Main Link outputs are disabled; when the source Main Link input signal levels are above a pre-determined threshold, a transition back to the appropriate active mode occurs.	EN is high; DPCD register 101h or 103h entry is invalid
	Other than a disabled Main Link output, this state characteristics are identical to the active state from where the transition occurred.	
	A transition to this state may occur from DisplayPort Active Mode, D3 Power Down Mode, or Compliance Test Mode when DPCD writes (from the local I^2C or the AUX channel) update the DPCD 101h or 103h registers with invalid values; this action causes the DP sink to issue an interrupt and re-train the link.	
Compliance Test Mode	Through local I^2C registers the device can be forced into ignoring TMDS_HPD_SNK, DP_HPD_SNK, and CAD_SNK; HPD_SRC and CAD_SRC outputs are programmed through local I^2C registers (default output low); all other configurations (such as output signal conditioning and EQ settings) are programmable through the local I^2C registers in this state.	EN is high; Local I^2C programming selects the this mode

8.5 Register Maps

8.5.1 Link Training and DPCD Description

The SN75DP126 can monitor the auxiliary interface access to DisplayPort Configuration Data (DPCD) registers during Link Training in DisplayPort mode, to select the output voltage swing V_{OD}, output pre-emphasis, and the EQ setting of the Main Link. The AUX monitor for SN75DP126 supports Link Training in 1-Mbps Manchester mode, and is disabled during TMDS modes of operation.

The DPCD registers monitored by SN75DP126 are listed below. Bit fields not listed are reserved and values written to reserved fields are ignored.

Table 5. DPCD Registers Utilized by the SN75DP126 AUX Monitor

ADDRESS	NAME	DESCRIPTION
00100h	LINK_BW_SET	Bits 7:0 = Link Bandwidth Setting Write Values: 06h – 1.62 Gbps per lane 0Ah – 2.7 Gbps per lane (default) 14h – 5.4 Gbps per lane *Note: any other value is reserved; the SN75DP126 will revert to 5.4 Gbps operation when any other value is written* Read Values: 00h – 1.62 Gbps per lane 01h – 2.7 Gbps per lane (default) 02h – 5.4 Gbps per lane
00101h	LANE_COUNT_SET	Bits 4:0 = Lane Count Write Values: 0h – All lanes disabled (default) 1h – One lane enabled 2h – Two lanes enabled 4h – Four lanes enabled *Note: any other value is invalid and disables all Main Link output lanes* Read Values: 0h – All lanes disabled (default) 1h – One lane enabled 3h – Two lanes enabled Fh – Four lanes enabled
00103h	TRAINING_LANE0_SET	Write Values: Bits 1:0 = Output Voltage V_{OD} Level 00 – Voltage swing level 0 (default) 01 – Voltage swing level 1 10 – Voltage swing level 2 11 – Voltage swing level 3 Bits 4:3 = Pre-emphasis Level 00 – Pre-emphasis level 0 (default) 01 – Pre-emphasis level 1 10 – Pre-emphasis level 2 11 – Pre-emphasis level 3 *Note: the following combinations are not allowed for bits [1:0]/[4:3]: 01/11, 10/10, 10/11, 11/01, 11/10, 11/11; setting to any of these invalid combinations disables all Main Link lanes until the register value is changed back to a valid entry* Read Values: Bits 1:0 = Output Voltage V_{OD} Level 00 – Voltage swing level 0 (default) 01 – Voltage swing level 1 10 – Voltage swing level 2 11 – Voltage swing level 3 Bits 3:2 = Pre-emphasis Level 00 – Pre-emphasis level 0 (default) 01 – Pre-emphasis level 110 – Pre-emphasis level 2 11 – Pre-emphasis level 3
00104h	TRAINING_LANE1_SET	Sets the V_{OD} and pre-emphasis levels for lane 1
00105h	TRAINING_LANE2_SET	Sets the V_{OD} and pre-emphasis levels for lane 2
00106h	TRAINING_LANE3_SET	Sets the V_{OD} and pre-emphasis levels for lane 3

Register Maps (continued)

Table 5. DPCD Registers Utilized by the SN75DP126 AUX Monitor (continued)

ADDRESS	NAME	DESCRIPTION
0010F	TRAINING_LANE0_1_SET2	Write Values: Bits 1:0 = Lane 0 Post Cursor 2 00 – IN0 expects post cursor2 level 0; OUT0 transmits at post cursor 2 level 0 01 – IN0 expects post cursor2 level 1; OUT0 transmits at post cursor 2 level 0 10 – IN0 expects post cursor2 level 2; OUT0 transmits at post cursor 2 level 0 11 – IN0 expects post cursor2 level 3; OUT0 transmits at post cursor 2 level 0 Bits 5:4 = Lane 1 Post Cursor 2 00 – IN1 expects post cursor2 level 0; OUT1 transmits at post cursor 2 level 0 01 – IN1 expects post cursor2 level 1; OUT1 transmits at post cursor 2 level 0 10 – IN1 expects post cursor2 level 2; OUT1 transmits at post cursor 2 level 0 11 – IN1 expects post cursor2 level 3; OUT1 transmits at post cursor 2 level 0 Read Values: Bits 1:0 = Lane 0 Post Cursor 2 00 – IN0 expects post cursor2 level 0; OUT0 transmits at post cursor 2 level 0 01 – IN0 expects post cursor2 level 1; OUT0 transmits at post cursor 2 level 0 10 – IN0 expects post cursor2 level 2; OUT0 transmits at post cursor 2 level 0 11 – IN0 expects post cursor2 level 3; OUT0 transmits at post cursor 2 level 0 Bits 3:2 = Lane 1 Post Cursor 2 00 – IN1 expects post cursor2 level 0; OUT1 transmits at post cursor 2 level 0 01 – IN1 expects post cursor2 level 1; OUT1 transmits at post cursor 2 level 0 10 – IN1 expects post cursor2 level 2; OUT1 transmits at post cursor 2 level 0 11 – IN1 expects post cursor2 level 3; OUT1 transmits at post cursor 2 level 0
0110F	TRAINING_LANE2_3_SET2	Bit definition identical to that of TRAINING_LANE_0_1_SET2 but for lanes 2 (IN2/OUT2) and lane 3 (IN3/OUT3)
00600h	SET_POWER	Bits 1:0 = Power Mode Write Values: 01 – Normal mode (default) 10 – Power down mode; D3 Standby Mode The Main Link and all analog circuits are shut down and the AUX channel is monitored during the D3 Standby Mode. The device exits D3 Standby Mode by access to this register, when CAD_SNK goes high, or if DP_HPD_SNK goes low for longer than $t_{T(HPD)}$, which indicates that the DP sink was disconnected, or that the PRIORITY control has selected the HDMI/DVI sink. *Note: setting the register to the invalid combination 0600h[1:0] = 00 or 11 is ignored by the device and the device remains in normal mode* Read Values: 00 – Normal mode (default) 01 – Power-down mode; D3 Standby Mode

8.5.2 Local I²C Interface Overview

The SN75DP126 local I²C interface is enabled when EN is input high, and the I2C_CTL_EN control input is not input low. The SCL_CTL and SDA_CTL terminals are used for I²C clock and I²C data respectively. The SN75DP126 I²C interface conforms to the two-wire serial interface defined by the I²C Bus Specification, Version 2.1 (January 2000), and supports the standard mode transfer up to 100 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for SN75DP126 is factory preset to 010110x with the least significant bit being determined by the I2C_CTL_EN 3-level control input. Table 6 clarifies the SN75DP126 target address.

Table 6. SN75DP126 I²C Target Address Description

SN75DP126 I²C TARGET ADDRESS							
BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (W/R)
0	1	0	1	1	0	X	0/1

I2C_CTL_EN = Low : Local I²C interface is disabled.
I2C_CTL_EN = Between V_{IL} and V_{IH}: X = 0, Address Cycle is 0x58 (Write) and 0x59 (Read).
I2C_CTL_EN = High: X = 1, Address Cycle is 0x5A (Write) and 0x5B (Read).

The following procedure is followed to write to the SN75DP126 I²C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SN75DP126 7-bit address and a zero-value “W/R” bit to indicate a write cycle
2. The SN75DP126 acknowledges the address cycle

3. The master presents the sub-address (I^2C register within SN75DP126) to be written, consisting of one byte of data, MSB-first
4. The SN75DP126 acknowledges the sub-address cycle
5. The master presents the first byte of data to be written to the I^2C register
6. The SN75DP126 acknowledges the byte transfer
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SN75DP126
8. The master terminates the write operation by generating a stop condition (P)

The following procedure is followed to read the SN75DP126 I^2C registers.

1. The master initiates a read operation by generating a start condition (S), followed by the SN75DP126 7-bit address and a one-value "W/R" bit to indicate a read cycle
2. The SN75DP126 acknowledges the address cycle
3. The SN75DP126 transmit the contents of the memory registers MSB-first starting at register 00h
4. The SN75DP126 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I^2C master acknowledges reception of each data byte transfer
5. If an ACK is received, the SN75DP126 transmits the next byte of data
6. The master terminates the read operation by generating a stop condition (P)

Note that no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I^2C master terminates the read operation.

Refer to Table 7 for SN75DP126 local I^2C register descriptions. Reads from reserved fields not described return zeros, and writes are ignored.

Table 7. SN75DP126 Local I^2C Control and Status Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
01h	3:2	SINK_PORT_SELECT 00 – DP_HPD_SNK and TMDS_HPD_SNK select the sink; when both are asserted, the PRIORITY control input is used where PRIORITY = LOW selects the DisplayPort sink (default) 01 – DP_HPD_SNK and TMDS_HPD_SNK select the sink; when both are asserted, the PRIORITY control input is used where PRIORITY = LOW selects the HDMI/DVI sink 10 – Force DisplayPort sink selection regardless of device HPD and control inputs 11 – Force HDMI/DVI sink selection regardless of device HPD and control inputs	RW
	1	FORCE_HPD_SRC 0 – Enter Standby mode when DP_HPD_SNK and TMDS_HPD_SNK are input low, and drive HPD_SRC high when DP_HPD_SNK or TMDS_HPD_SNK are input high (default) 1 – Drive HPD_SRC output high regardless of DP_HPD_SNK and TMDS_HPD_SNK inputs	RW
	0	FORCE_SHUTDOWN_MODE 0 – SN75DP126 is forced to Shutdown mode 1 – Shutdown mode is determined by EN input, normal operation (default)	RW
02h	7:0	TI_TEST. This field defaults to zero value, and should not be modified.	RW
03h	5:4	SQUELCH_SENSITIVITY. Input Main Link squelch sensitivity is selected by this field, and determines the transitions to and from the Output Disable mode. 00 – Main Link IN0p/n squelch detection threshold set to 60 mVpp 01 – Main Link IN0p/n squelch detection threshold set to 115 mVpp (default) 10 – Main Link IN0p/n squelch detection threshold set to 160 mVpp 11 – Main Link IN0p/n squelch detection threshold set to 200 mVpp	RW
	3	SQUELCH_ENABLE 0 – Main Link IN0p/n squelch detection enabled (default) 1 – Main Link IN0p/n squelch detection disabled	RW

Table 7. SN75DP126 Local I²C Control and Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
04h	3	TI_TEST. This field defaults to zero value, and should not be modified.	RW
	2	LINK_TRAINING_ENABLE 0 – DisplayPort sink Link Training is disabled. V_{OD} and Pre-emphasis are configured through the I²C register interface; the EQ is fixed when this bit is zero. 1 – DisplayPort sink Link Training is enabled (default)	RW
	1	Reserved - Do not change this value	R/W
05h	7	EQ_I2C_ENABLE 0 – EQ settings controlled by device inputs only (default) 1 – EQ settings controlled by I²C register settings	RW
	6:4	AEQ_L0_LANE0_SET. This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L1_LANE0_SET. This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled • I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
06h	6:4	AEQ_L2_LANE0_SET. This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L3_LANE0_SET. This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW

Table 7. SN75DP126 Local I²C Control and Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
07h	6:4	AEQ_L0_LANE1_SET. This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L1_LANE1_SET. This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled • I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
08h	6:4	AEQ_L2_LANE1_SET. This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L3_LANE1_SET. This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
09h	6:4	AEQ_L0_LANE2_SET. This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L1_LANE2_SET. This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled • I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW

Table 7. SN75DP126 Local I²C Control and Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
0Ah	6:4	AEQ_L2_LANE2_SET. This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L3_LANE2_SET. This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
0Bh	6:4	AEQ_L0_LANE3_SET. This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L1_LANE3_SET. This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ mode: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
0Ch	6:4	AEQ_L2_LANE3_SET. This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L3_LANE3_SET. This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW

Table 7. SN75DP126 Local I²C Control and Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
15h	4:3	DP_BOOST. Controls the output pre-emphasis amplitude when the DisplayPort sink is selected; allows to reduce or increase all pre-emphasis settings by ~10%. Setting this field will impact V_{OD} when pre-emphasis is disabled. This setting also impacts the output in TMDS mode for the DisplayPort sink connection when the DisplayPort sink CAD_SNK input is high. 00 – Pre-emphasis reduced by ~10%; V_{OD} reduced by 10% if pre-emphasis is disabled. 01 – Pre-emphasis nominal (default) 10 – Pre-emphasis increased by ~10%; V_{OD} increased by 10% if pre-emphasis is disabled. 11 – Reserved	RW
	2	DP_TMDS_VOD. Sets the target output swing in TMDS mode when the DisplayPort sink is selected, where CAD_SNK input is high. 0 – Low TMDS output swing for DisplayPort sink channel (default) 1 – High TMDS output swing for DisplayPort sink channel	RW
	1:0	DP_TMDS_VPRE. Controls the output pre-emphasis in TMDS mode when the DisplayPort sink is selected, where CAD_SNK input is high. 00 – No TMDS pre-emphasis for DisplayPort sink channel (default) 01 – Low TMDS pre-emphasis for DisplayPort sink channel 10 – High TMDS pre-emphasis for DisplayPort sink channel 11 – Reserved	RW
17h	3	DP_HPD_TEST_MODE 0 – Normal HPD operating mode. (default) 1 – DisplayPort sink compliance test mode. DP_HPD_SNK is pulled high internally, the TMDS_HPD_SNK is pulled low internally, and the HPD_SRC output is driven high and the Main Link is activated depending on the squelch setting.	RW
	1	CAD_OUTPUT_INVERT 0 – CAD_SRC output high means TMDS cable adapter detected when the DisplayPort sink is selected (default) 1 – CAD_SRC output low means TMDS cable adapter detected when the DisplayPort sink is selected	RW
	0	CAD_TEST_MODE 0 – Normal CAD mode. CAD_SRC reflects the status of CAD_SNK, based on the value of CAD_OUTPUT_INVERT, when the DisplayPort sink is selected (default) 1 – Test mode. CAD_SRC indicates TMDS mode when the DisplayPort sink is selected, depending on the value of CAD_OUTPUT_INVERT; CAD_SNK input is ignored. This mode allows execution of certain tests on SN75DP126 without a connected TMDS display sink.	
18h	3:2	HDMI/DVI_PRE 00 – 0 dB Pre-emphasis applied to the HDMI/DVI sink TMDS output 01 – Reserved 10 – Reserved 11 – 2 dB Pre-emphasis applied to the HDMI/DVI sink TMDS output	RW
19h – 1Ah	7:0	TI_TEST. These registers shall not be modified.	RW
1Bh	7	I2C_SOFT_RESET. Writing a one to this register resets all I²C registers to default values. Writing a zero to this register has no effect. Reads from this register return zero.	WO
	6	DPCD_RESET. Writing a one to this register resets the DPCD register bits (corresponding to DPCD addresses 103h – 10Fh). Writing a zero to this register has no effect. Reads from this register return zero.	WO
1Ch	3:0	DPCD_ADDR_HIGH. This value maps to bits 19:16 of the 20-bit DPCD register address accessed through the DPCD_DATA register.	RW
1Dh	7:0	DPCD_ADDR_MID. This value maps to bits 15:8 of the 20-bit DPCD register address accessed through the DPCD_DATA register.	RW
1Eh	7:0	DPCD_ADDR_LOW. This value maps to bits 7:0 of the 20-bit DPCD register address accessed through the DPCD_DATA register.	RW

Table 7. SN75DP126 Local I²C Control and Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS
1Fh	7:0	DPCD_DATA. This register contains the data to write into or read from the DPCD register addressed by DPCD_ADDR_HIGH, DPCD_ADDR_MID, and DPCD_ADDR_LOW.	RW
20h	7:1	DEV_ID_REV. This field identifies the device and revision. 0000000 – SN75DP126 Revision 0	RO
	0	BIT_INVERT. The value read from this field is the inverse of that written. Default read value is '1'.	RW
21h	7:0	TI_TEST. These registers shall not be modified.	RW
22h – 27h	7:0	TI_TEST_RESERVED. These read only registers are reserved for test; writes are ignored.	RO

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN75DP126 switches one Dual-Mode DisplayPort (DP++) input to one DP++ sink output or one HDMI/DVI sink output. The HDMI/DVI output has a built-in level translator compliant with DVI 1.0 and HDMI 1.4b and supports resolutions greater than 1920 x 1440 and HDTV deep color at 1080p.

9.2 Typical Application

The SN75DP126 can be used in a dongle implementation to switch from one DP++ Source to one DP++ Sink or one HDMI/DVI Sink.

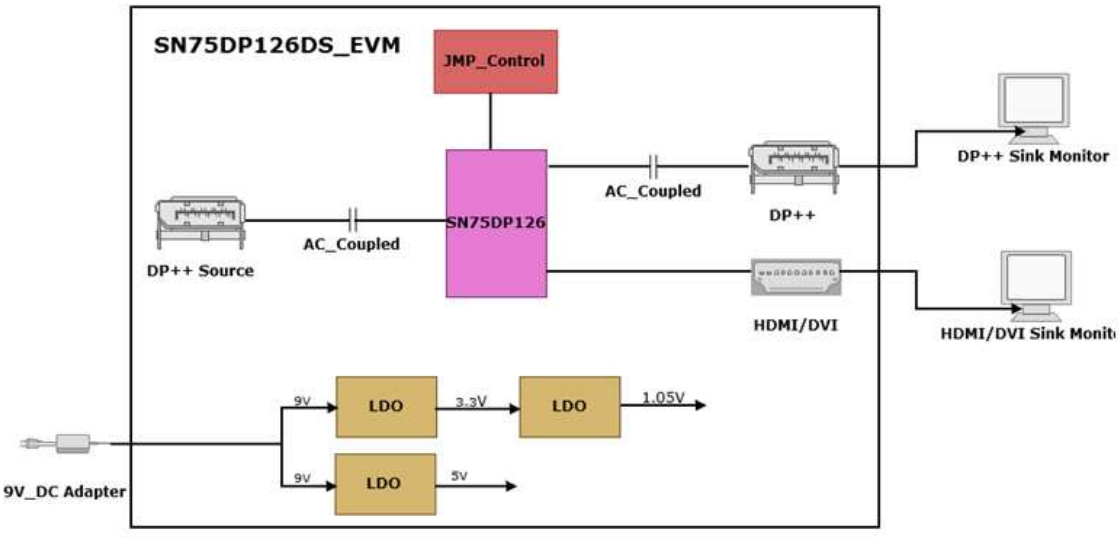


Figure 27. Typical Dongle Implementation

9.2.1 Design Requirements

The design requirements for this application are listed in Table 8.

Table 8. Design Requirements

Design Parameter	Example Value
Source	DP++
Sink	DP++
Sink Priority	High (DP)
OVS	Low
PRE	Low
EQ	Low
SLEW	Low
VCC	9 V

9.2.2 Detailed Design Procedure

9.2.2.1 AC Coupling Capacitors

The DP link is an AC-coupled interface. AC coupling capacitors must be placed between the Source and the DP126.

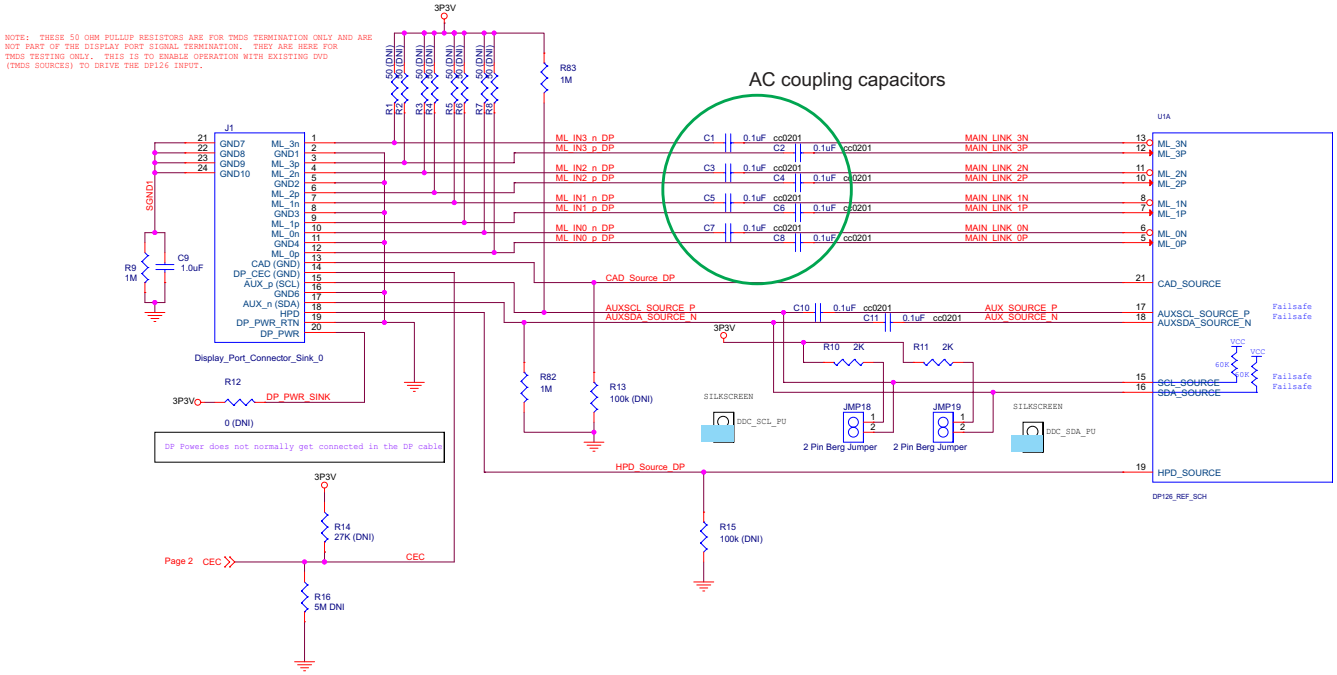


Figure 28. Source-to-DP126 AC Coupling Capacitors

AC coupling capacitors are required from the DP126 output to the DP Sink as well.

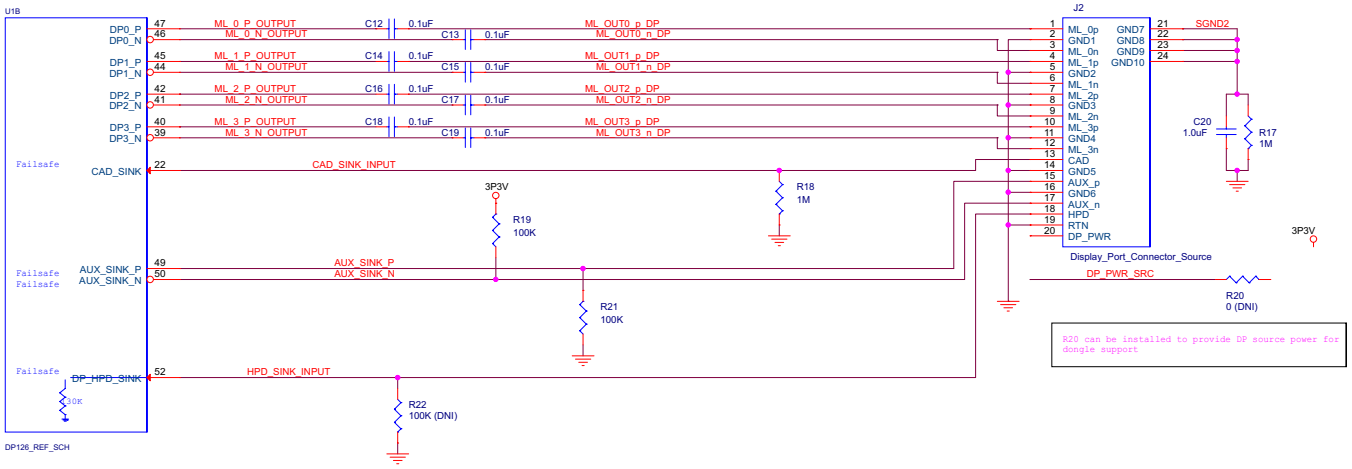


Figure 29. DP126 Output to the DP Sink AC Coupling Capacitors

9.2.2.2 Configuration Options

It is recommended to leave place holders on the Configuration I/O for further fine tuning.

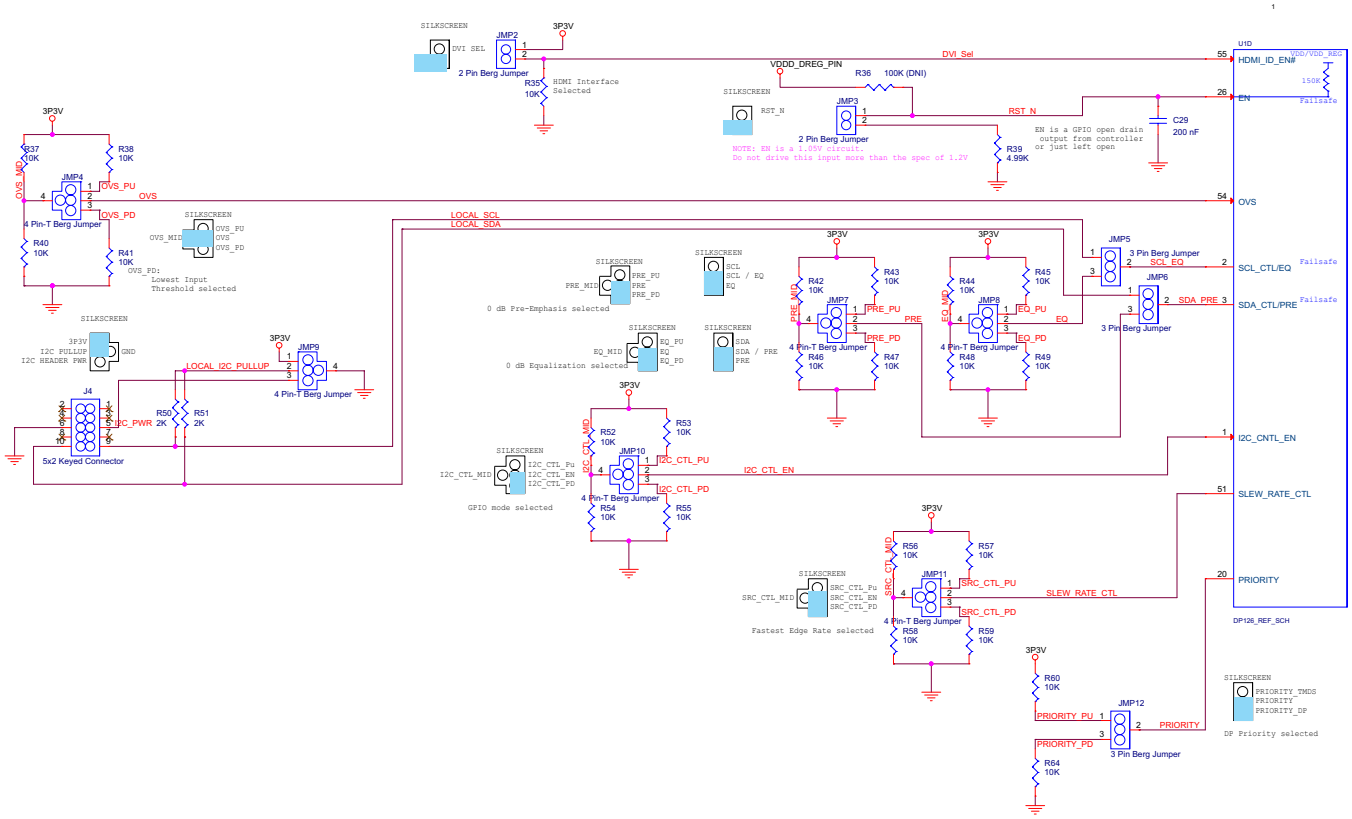


Figure 30. Configuration Options

9.2.2.3 Dual Layout for Single or Dual Power Supply

The SN75DP126DS requires dual power supply whereas the DP126SS requires only one power supply. The design can have options to use either one with minor hardware changes

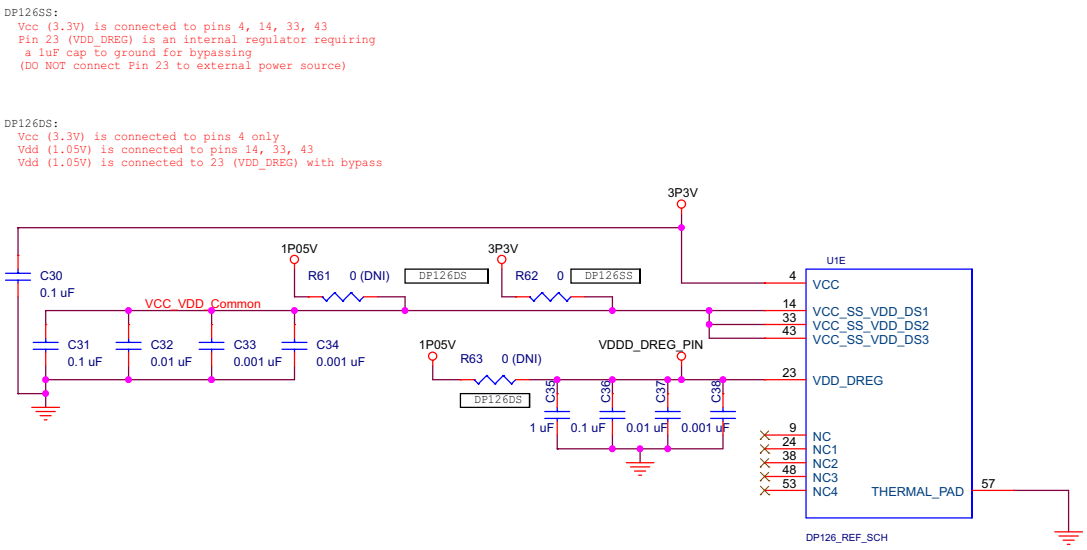


Figure 31. Power Supply Layout

9.2.3 Application Curves

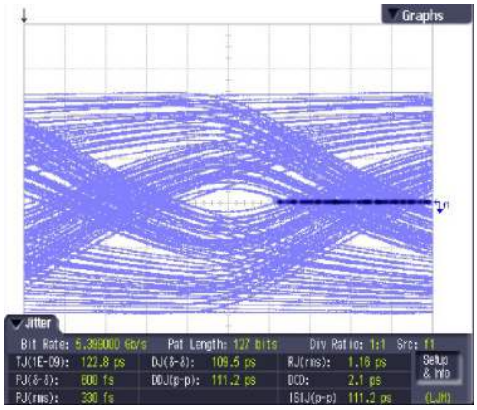


Figure 32. Main Link Input with 22-inch Trace; DisplayPort Sink

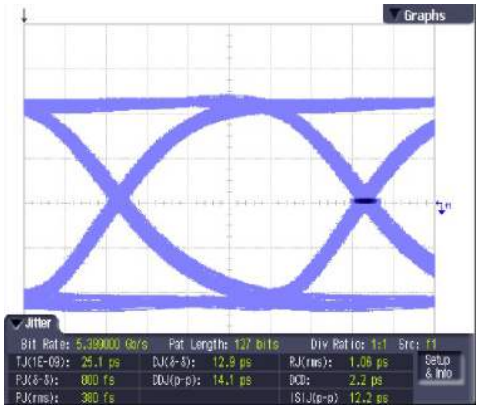


Figure 33. SN75DP126 Output; 22-inch Input Trace; 15 dB EQ Setting; DP Sink

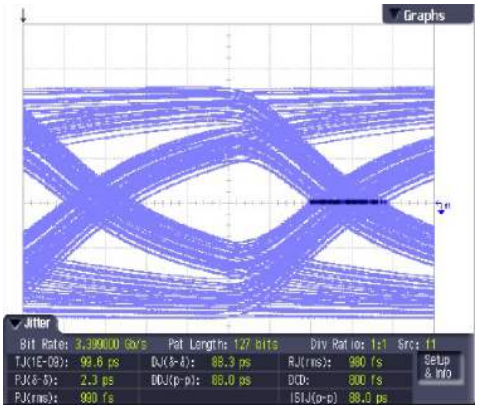


Figure 34. Main Link Input with 22-inch Trace; TMDS Sink

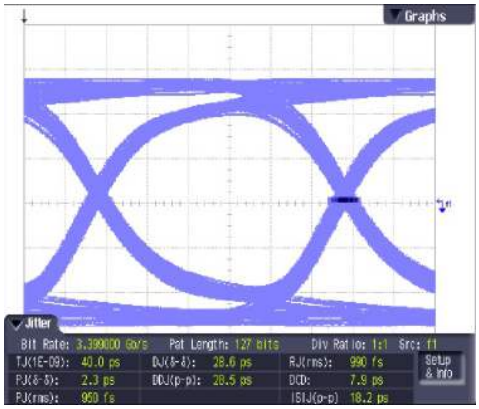


Figure 35. SN75DP126 Output; 22-inch Input Trace; 15 dB EQ Setting; TMDS Sink

10 Power Supply Recommendations

10.1 Analog vs Digital vs High Power

Digital ground and power carry the RF energy that needs to be contained, so it is best to isolate it from any other power and ground, either analog, high power, or other unrelated trace. If noise from the microcomputer or any other circuit gets on an isolated ground, it can be returned by careful placement of a small RF capacitor in the 470 – 1000 pF range. Choosing the location of the capacitor is by trial and error, and is best done in the screen room.

10.2 Analog Power-Supply Pins and Analog Reference Voltages

The reference voltage of an analog-to-digital (A/D) converter integrated into a microcomputer does supply a very small amount of clocked current; however, it is not enough to be concerned about from a noise-emissions standpoint. Most applications have the analog V_{SS} /V_{CC} tied to the digital V_{SS1} /V_{CC1} pins, which does not change significantly the noise characteristics of the A/D nor the radiated emissions

11 Layout

11.1 Layout Guidelines

- Decoupling with small current loops is recommended.
- It is recommended to place the de-coupling cap as close as possible to the device and on the same side of the PCB.
- Choose the capacitor such that the resonant frequency of the capacitor does not align closely with 5.4 GHz.
- Also provide several GND vias to the thermal pad to minimize the area of current loops.

11.1.1 Layer Stack

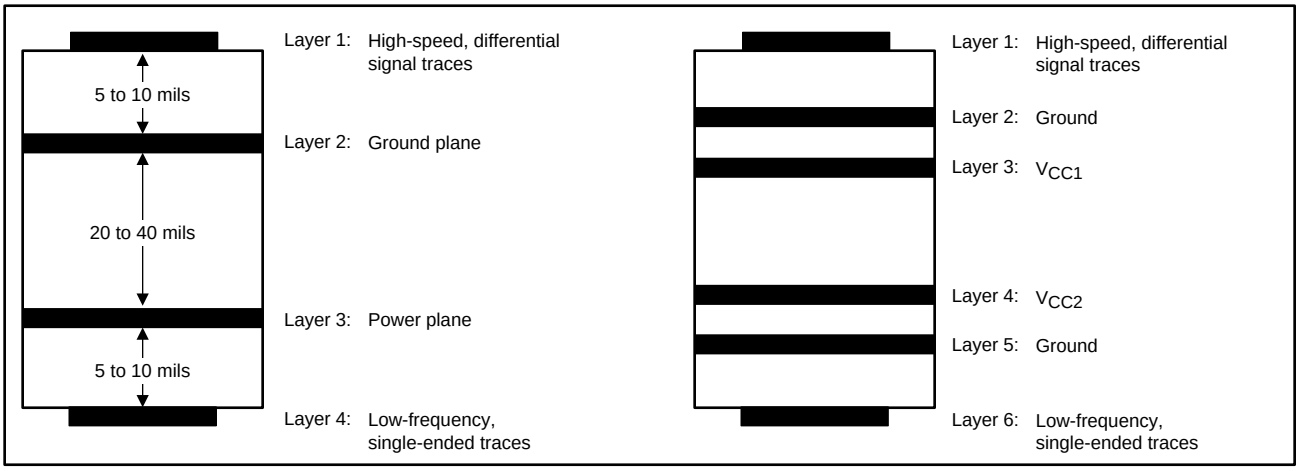


Figure 36. Recommended 4- or 6- Layer (0.062") Stack for a Receiver PCB Design

Routing the high-speed differential signal traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the DisplayPort connectors to the repeater inputs and from the repeater output to the subsequent receiver circuit.

Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.

Routing the fast-edged control signals on the bottom layer by prevents them from cross-talking into the high-speed signal traces and minimizes EMI.

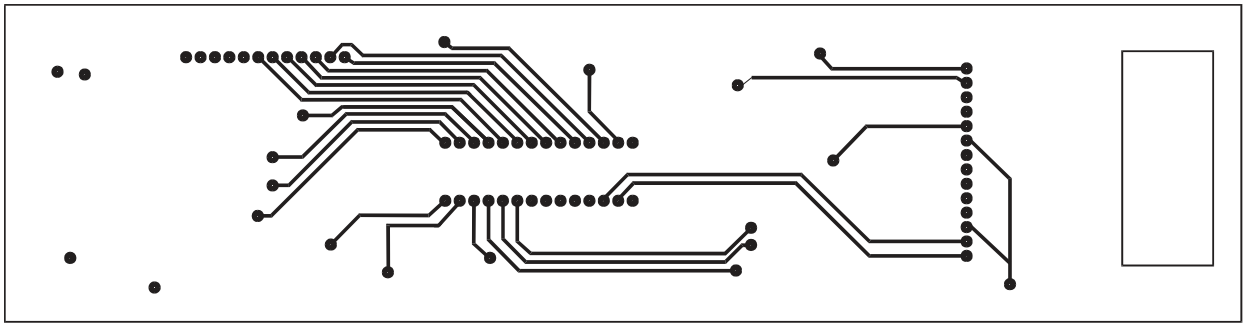
Layout Guidelines (continued)

If the receiver requires a supply voltage different from the one of the repeater, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also, the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. Finally, a second power/ground system provides added isolation between the signal layers.

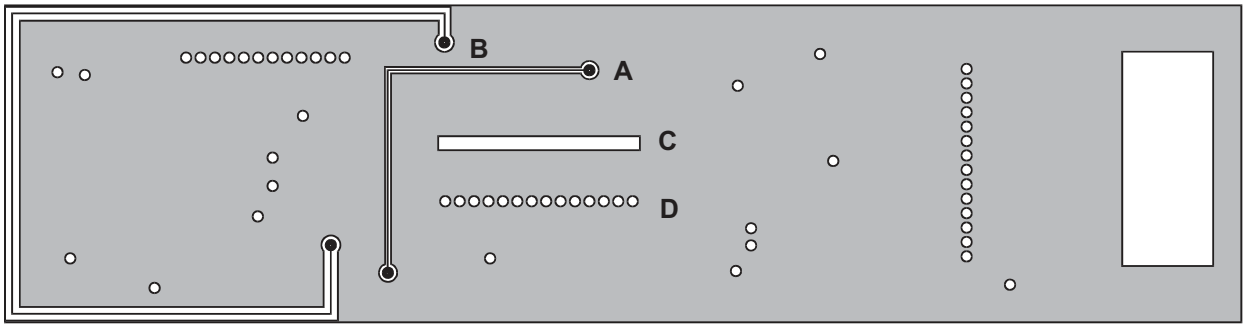
11.1.2 Power Plane Do's and Don'ts for Four-Layer Boards

Rreducing noise in four-layer board configurations is of paramount concern. The following guidelines should maintain the advantages gained in the four-layer board layout.

- Pay utmost attention to how the holes and cutouts in the planes are done. They break up the plane and, therefore, cause increased loop areas (see A and B in Figure 37).
- Avoid buried traces in the ground plane. If you have to use them, put them in the +V plane.
- When making through holes for 100-mil-center-spacing leads in the plane, place a small trace between each pin. Breaking up the plane with a row of holes is much better than having a long slot (see C and D in Figure 37).
- When splitting up the ground plane to make a digital and power ground for example, make sure that the signals connected to the microcomputer are still located entirely over the digital ground. Extending signal traces beyond the power ground is detrimental because the power ground does not work to reduce the loop area for digital noise signals.



Ground Plane



A POOR – Buried trace cuts ground plane into two parts

B BETTER – Buried trace around the perimeter
Best solution is no trace at all in the ground plane

C POOR – Slot formed by 100-mil spacing cuts up ground plane and focuses slot antenna radiation into that connection

D BETTER – Ground plane extends between 100-mil centers

Figure 37. Four-Layer Board Layout Considerations

Layout Guidelines (continued)

11.1.3 Differential Traces

Guidelines for routing PCB traces are necessary when trying to maintain signal integrity and lower EMI. Although there seems to be an endless number of precautions to be taken, this section provides only a few main recommendations as layout guidance.

1. Reduce intra-pair skew in a differential trace by introducing small meandering corrections at the point of mismatch.
2. Reduce inter-pair skew, caused by component placement and IC pinouts, by making larger meandering correction along the signal path. Use chamfered corners with a length-to-trace width ratio of between 3 and 5. The distance between bends should be 8 to 10 times the trace width.
3. Use 45 degree bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45o bends is seen as a smaller discontinuity.
4. When routing around an object, route both trace of a pair in parallel. Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur.
5. Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b), the resulting discontinuity, however, is limited to a far narrower area.
6. When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.
7. Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise they will cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.
8. Use the smallest size possible for signal trace vias and DisplayPort connector pads as they have less impact on the 100 Ω differential impedance. Large vias and pads can cause the impedance to drop below 85 Ω.
9. Use solid power and ground planes for 100 Ω impedance control and minimum power noise.
10. For 100 Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
11. Keep the trace length between the DisplayPort connector and the DisplayPort device as short as possible to minimize attenuation.
12. Use good DisplayPort connectors whose impedances meet the specifications.
13. Place bulk capacitors (for example, 10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.
14. Place smaller 0.1 µF or 0.01 µF capacitors at the device.

11.2 Layout Example

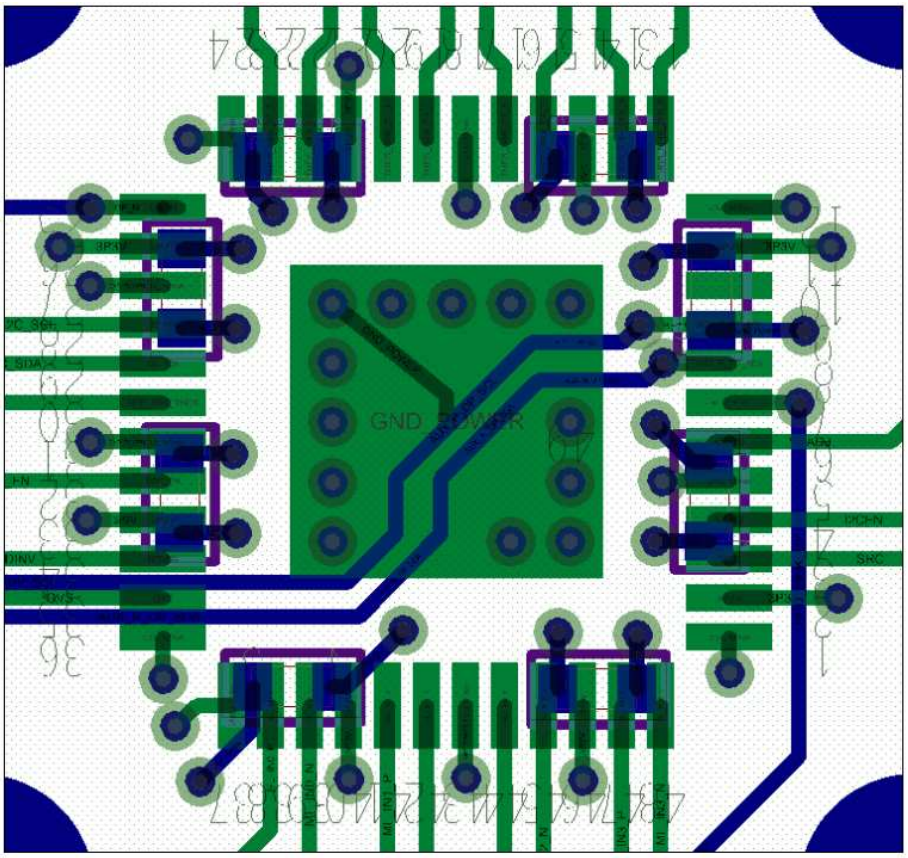


Figure 38. Thermal PAD Grounding

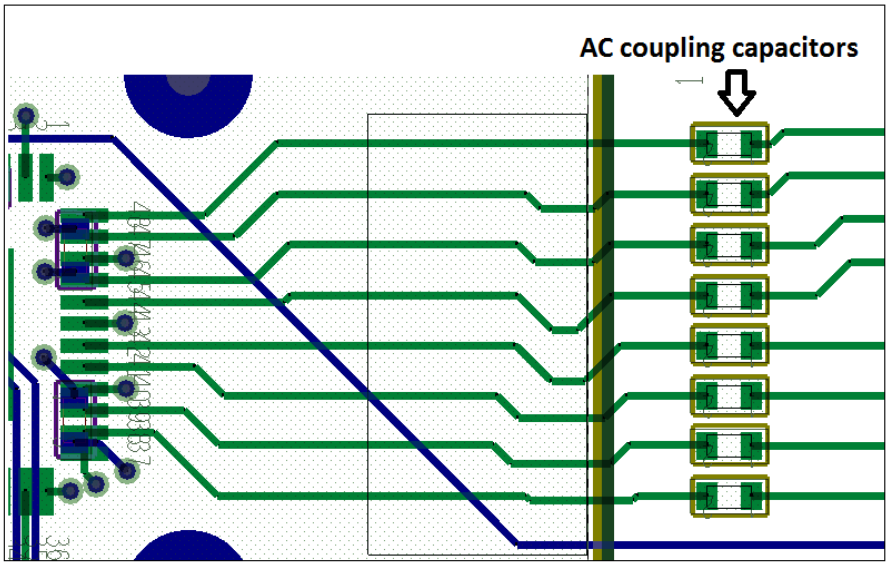


Figure 39. AC Capacitors Placement and Routing Example

Layout Example (continued)

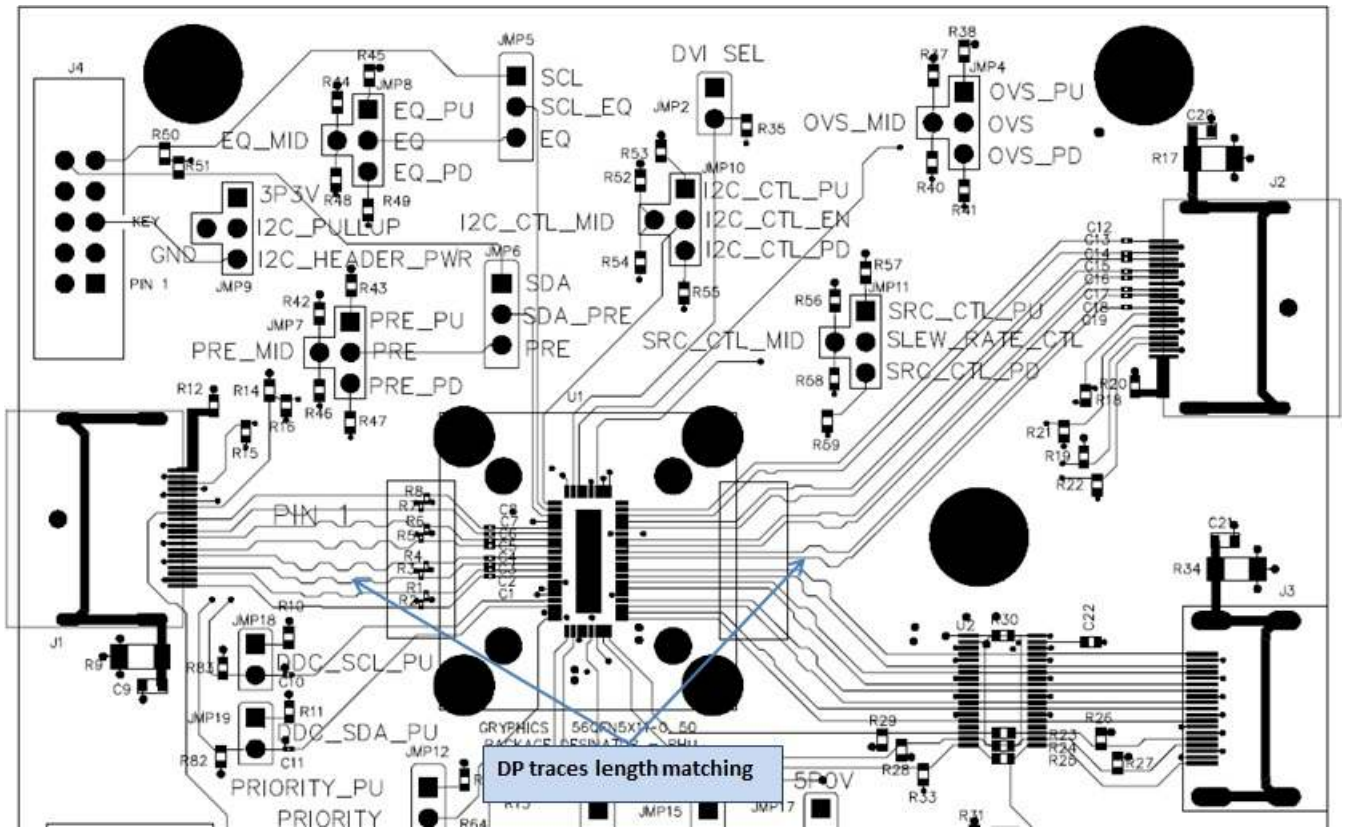


Figure 40. SN75DP126 Layout

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
DisplayPort is a trademark of VESA Standards Association.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75DP126SSRHUR	ACTIVE	WQFN	RHU	56	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 85	DP126SS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

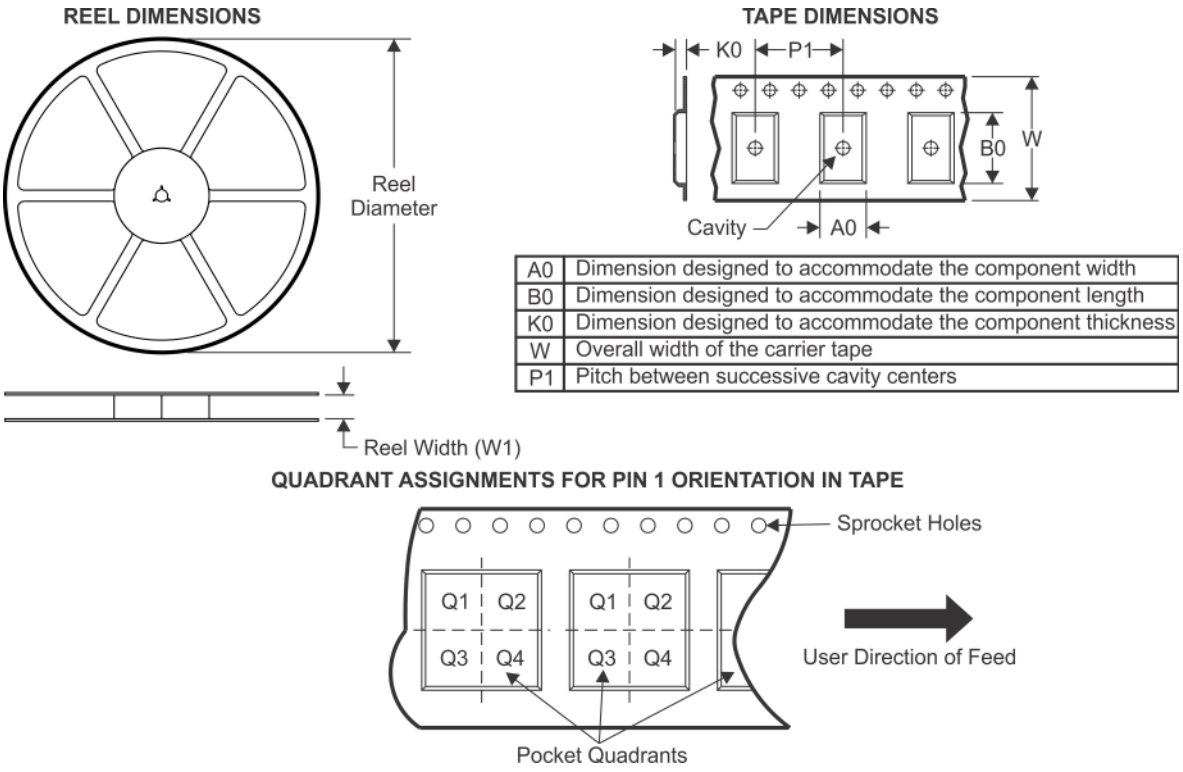
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

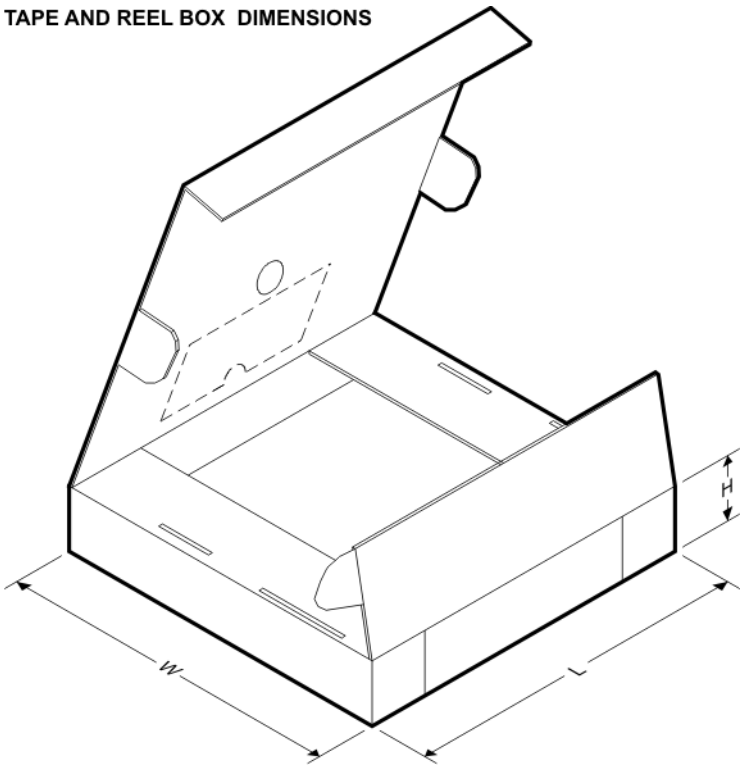


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP126SSRHUR	WQFN	RHU	56	2000	330.0	24.4	5.3	11.3	1.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

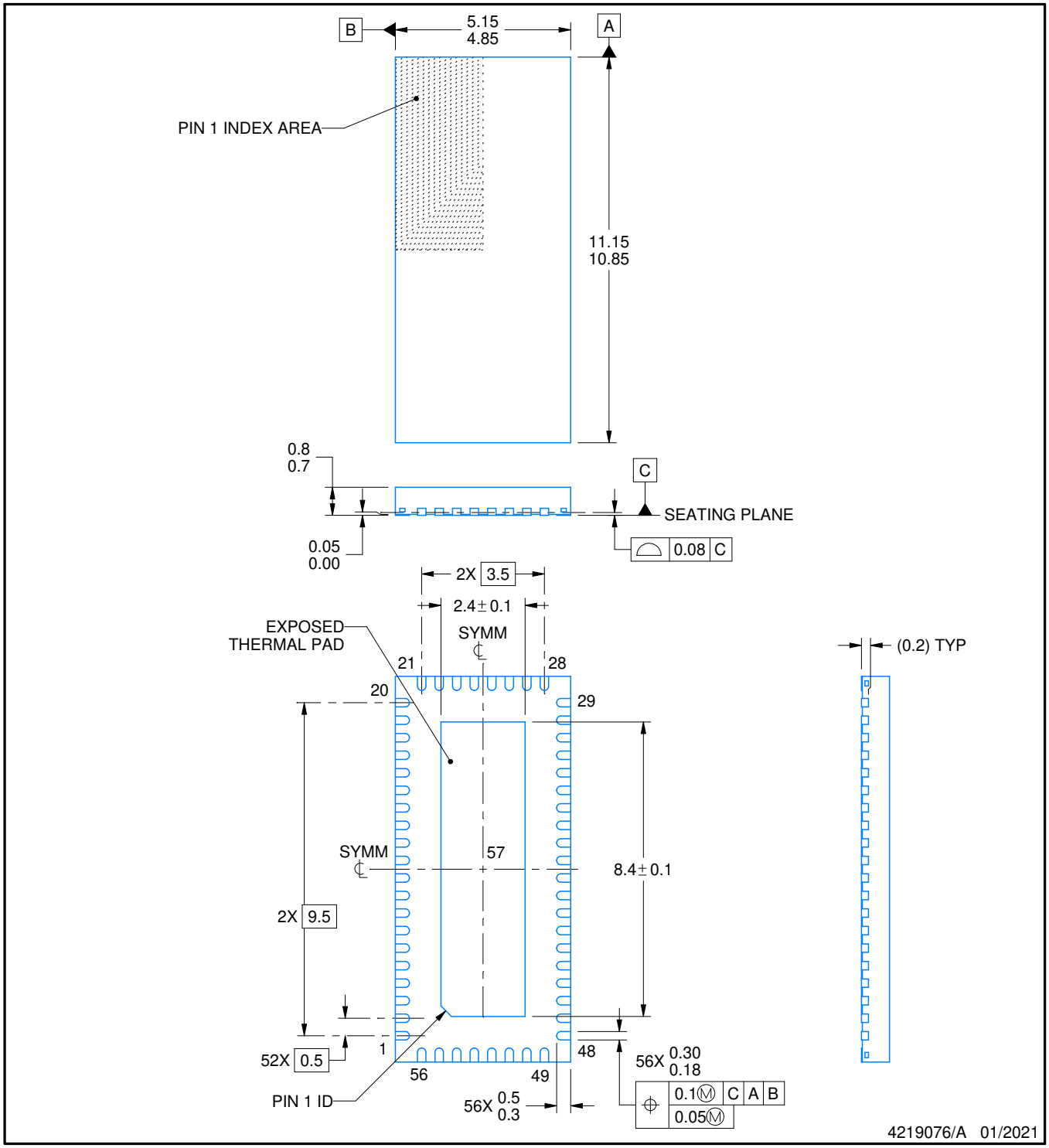
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP126SSRHUR	WQFN	RHU	56	2000	367.0	367.0	45.0

PACKAGE OUTLINE

RHU0056A

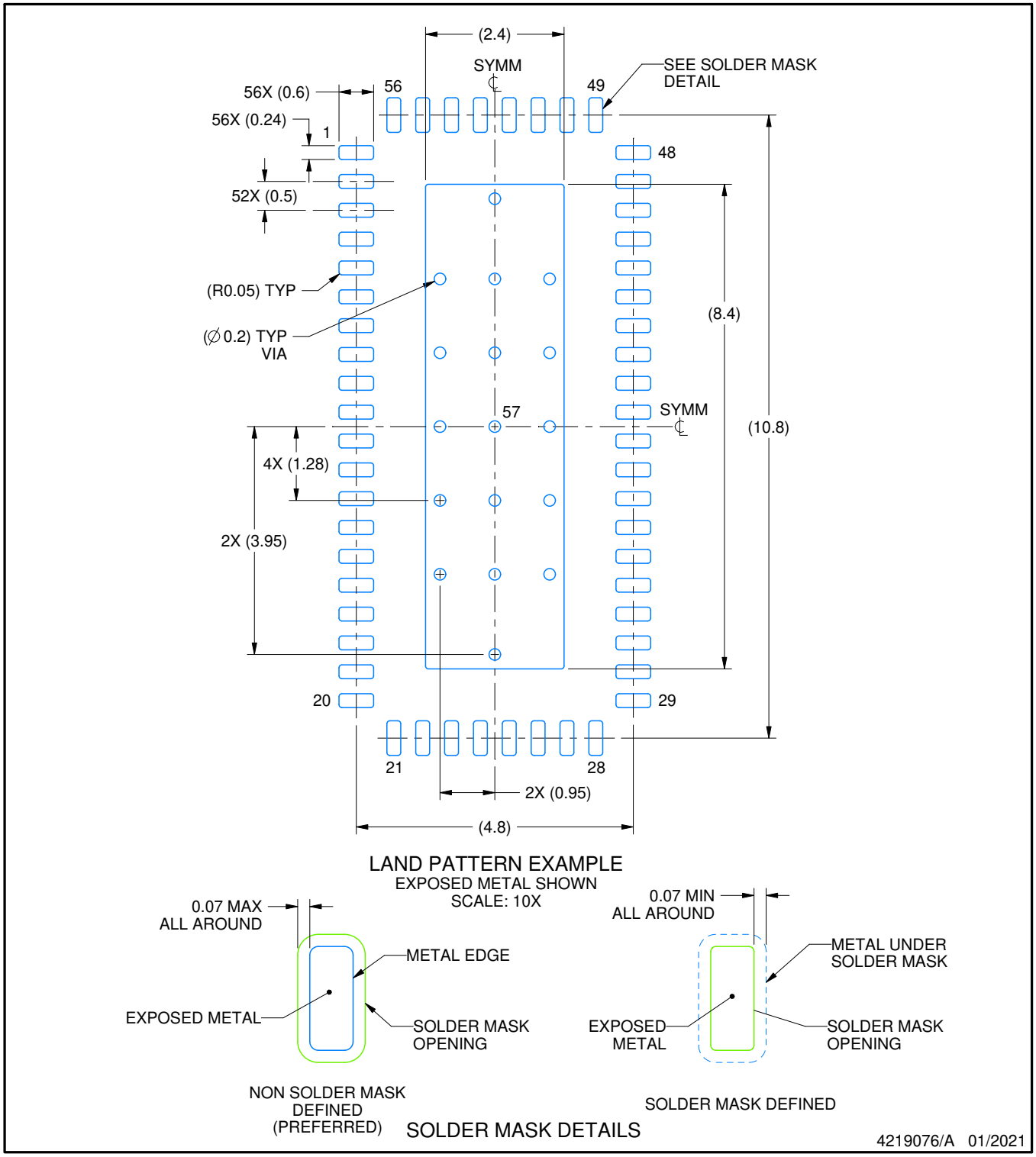
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



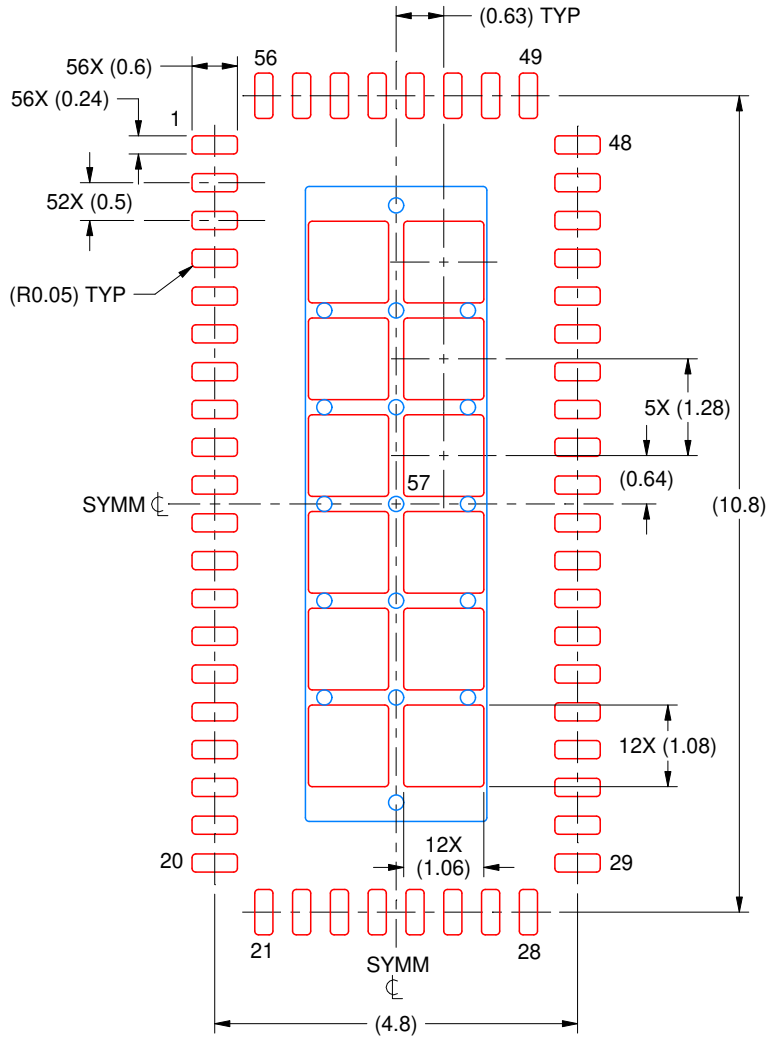
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219076/A 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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