Revision History

128Mb AS4C4M32D1A - 144 ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	May. 2016

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Features

- Fast clock rate: 200 MHz
- Differential Clock CK & $\overline{CK}$ input
- 4 Bi-directional DQS. Data transactions on both edges of DQS (1DQS / Byte)
- DLL aligns DQ and DQS transitions
- Edge aligned data & DQS output
- Center aligned data & DQS inpu
- 4 internal banks, 1M x 32-bit for each bank
- Programmable mode and extended mode registers
  - CAS Latency: 2, 2.5, 3
  - Burst length: 2, 4, 8
  - Burst Type: Sequential & Interleave
- All inputs except DQ's & DM are at the positive edge of the system clock
- 4 individual DM control for write masking only
- Auto Refresh and Self Refresh
- 4096 refresh cycles / 64ms
- Operating Temperature:
  - Industrial -40°C~85°C
  - Commercial 0°C to 70°C
- Power supplies: V_{DD} & V_{DDQ} = 2.5V ± 0.2V
- Interface: SSTL_2 I/O compatible
- 144-ball 12 x 12 x 1.4mm LFBGA package
  -Pb and Halogen Free

Overview

The 128Mb DDR SDRAM is a high-speed CMOS double data rate synchronous DRAM containing 128 Mbits. It is internally configured as a quad 1M x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CK). Data outputs occur at both rising edges of CK and $\overline{CK}$. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command, which is then followed by a Read or Write command. The device provides programmable Read or Write burst lengths of 2, 4, 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. In addition, 128Mb DDR SDRAM features programmable DLL option. By having a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth; result in a device particularly well suited to high performance main memory and graphics applications.

Table 1. Ordering Information

Part Number	Org	Temperature	MaxClock (MHz)	Package
AS4C4M32D1A-5BCN	4Mx32	Commercial 0°C to 70°C	200	144-ball FBGA
AS4C4M32D1A-5BIN	4Mx32	Industrial -40°C to 85°C	200	144-ball FBGA

Table 2. Speed Grade Information

Speed Grade	Clock Frequency	CAS Latency	tRCD (ns)	tRP (ns)
DDR1-400	200MHz	3	15	15

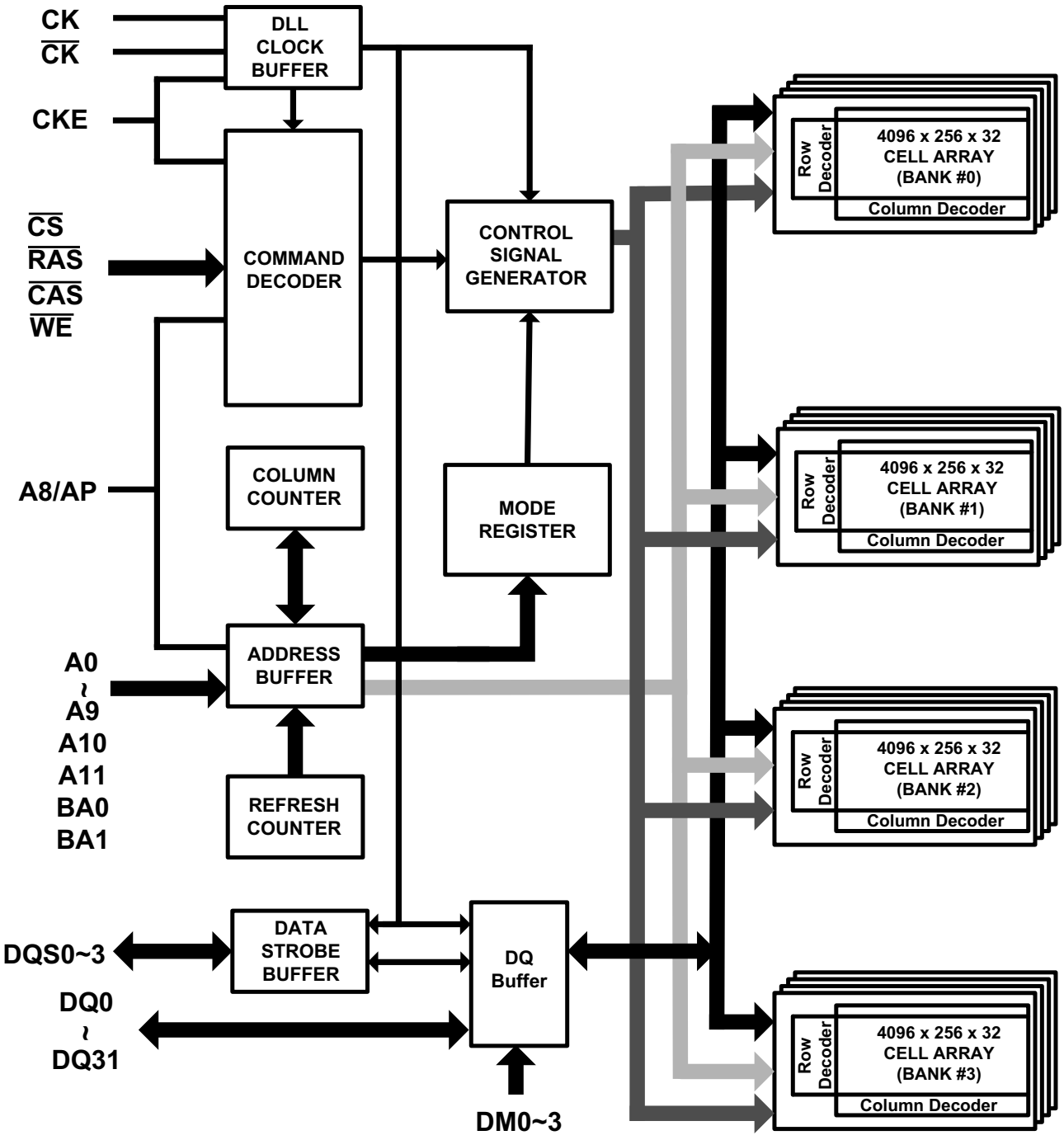
Figure 1. Pin Assignment (LFBGA 144Ball Top View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	DQS0	DM0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	DM3	DQS3
B	DQ4	VDDQ	NC	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	NC	VDDQ	DQ27
C	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
D	DQ7	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ24
E	DQ17	DQ16	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ15	DQ14
F	DQ19	DQ18	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ13	DQ12
G	DQS2	DM2	NC	VSSQ	VSS	VSS	VSS	VSS	VSSQ	NC	DM1	DQS1
H	DQ21	DQ20	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ11	DQ10
J	DQ22	DQ23	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ8
K	$\overline{CAS}$	$\overline{WE}$	VDD	VSS	A10	VDD	VDD	NC	VSS	VDD	NC	NC
L	$\overline{RAS}$	NC	NC	BA1	A2	A11	A9	A5	NC	CK	$\overline{CK}$	NC
M	$\overline{CS}$	NC	BA0	A0	A1	A3	A4	A6	A7	A8	CKE	VREF

Table 3. Pin Assignment by Name (LFBGA 144Ball)

Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbo	Location	Symbol	Location
A0	M4	DQ6	C1	DQ24	D12	CK	L10	VDDQ	B6	VSS	E5	VSS	J7	VSSQ	G4
A1	M5	DQ7	D1	DQ25	C12	$\overline{CK}$	L11	VDDQ	B7	VSS	E6	VSS	J8	VSSQ	G9
A2	L5	DQ8	J12	DQ26	C11	CKE	M11	VDDQ	B9	VSS	E7	VSS	K4	VSSQ	H4
A3	M6	DQ9	J11	DQ27	B12	$\overline{CS}$	M1	VDDQ	B11	VSS	E8	VSS	K9	VSSQ	H9
A4	M7	DQ10	H12	DQ28	A9	$\overline{RAS}$	L1	VDDQ	D2	VSS	F5	VSSQ	A3	VSSQ	J4
A5	L8	DQ11	H11	DQ29	A8	$\overline{CAS}$	K1	VDDQ	D11	VSS	F6	VSSQ	A10	VSSQ	J9
A6	M8	DQ12	F12	DQ30	B8	$\overline{WE}$	K2	VDDQ	E3	VSS	F7	VSSQ	C3	NC	B3
A7	M9	DQ13	F11	DQ31	A7	VREF	M12	VDDQ	E10	VSS	F8	VSSQ	C4	NC	B10
A8/AP	M10	DQ14	E12	DQS0	A1	VDD	C6	VDDQ	F3	VSS	G5	VSSQ	C5	NC	G3
A9	L7	DQ15	E11	DQS1	G12	VDD	C7	VDDQ	F10	VSS	G6	VSSQ	C8	NC	G10
A10	K5	DQ16	E2	DQS2	G1	VDD	D3	VDDQ	H3	VSS	G7	VSSQ	C9	NC	K8
A11	L6	DQ17	E1	DQS3	A12	VDD	D10	VDDQ	H10	VSS	G8	VSSQ	C10	NC	K11
DQ0	A6	DQ18	F2	DM0	A2	VDD	K3	VDDQ	J3	VSS	H5	VSSQ	D5	NC	K12
DQ1	B5	DQ19	F1	DM1	G11	VDD	K6	VDDQ	J10	VSS	H6	VSSQ	D8	NC	L2
DQ2	A5	DQ20	H2	DM2	G2	VDD	K7	VSS	D4	VSS	H7	VSSQ	E4	NC	L3
DQ3	A4	DQ21	H1	DM3	A11	VDD	K10	VSS	D6	VSS	H8	VSSQ	E9	NC	L9
DQ4	B1	DQ22	J1	BA0	M3	VDDQ	B2	VSS	D7	VSS	J5	VSSQ	F4	NC	L12
DQ5	C2	DQ23	J2	BA1	L4	VDDQ	B4	VSS	D9	VSS	J6	VSSQ	F9	NC	M2

Figure 2. Block Diagram



Pin Descriptions

Table 4. Pin Details

Symbol	Type	Description
CK, $\overline{CK}$	Input	**Differential Clock:** CK, $\overline{CK}$ are driven by the system clock. All SDRAM input commands are sampled on the positive edge of CK. Both CK and $\overline{CK}$ increment the internal burst counter and controls the output registers.
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes low synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0, BA1	Input	**Bank Activate:** BA0 and BA1 define to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied. They also define which Mode Register or Extended Mode Register is loaded during a Mode Register Set command.
A0-A11	Input	**Address Inputs:** A0-A11 are sampled during the Bank Activate command (row address A0-A11) and Read/Write command (column address A0-A7 with A8 defining Auto Precharge) to select one location out of the 1M available in the respective bank. During a Precharge command, A8 is sampled to determine if all banks are to be precharged (A8 = HIGH). The address inputs also provide the op-code during a Mode Register Set or Extended Mode Register Set command.
$\overline{CS}$	Input	**Chip Select:** $\overline{CS}$ enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when $\overline{CS}$ is sampled HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code.
$\overline{RAS}$	Input	**Row Address Strobe:** The $\overline{RAS}$ signal defines the operation commands in conjunction with the $\overline{CAS}$ and /WE signals and is latched at the positive edges of CK. When $\overline{RAS}$ and $\overline{CS}$ are asserted "LOW" and $\overline{CAS}$ is asserted "HIGH" either the BankActivate command or the Precharge command is selected by the $\overline{WE}$ signal. When the $\overline{WE}$ is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the $\overline{WE}$ is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
$\overline{CAS}$	Input	**Column Address Strobe:** The $\overline{CAS}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and /WE signals and is latched at the positive edges of CK. When /RAS is held "HIGH" and $\overline{CS}$ is asserted "LOW" the column access is started by asserting $\overline{CAS}$ "LOW" Then, the Read or Write command is selected by asserting $\overline{WE}$ "HIGH " or "LOW".
$\overline{WE}$	Input	**Write Enable:** The $\overline{WE}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ signals and is latched at the positive edges of CK. The $\overline{WE}$ input is used to select the BankActivate or Precharge command and Read or Write command.
DQS0-DQS3	Input / Output	**Bidirectional Data Strobe:** The DQSx signals are mapped to the following data bytes: DQS0 to DQ0-DQ7, DQS1 to DQ8-DQ15, DQS2 to DQ16-DQ23, and DQS3 to DQ24-DQ31.
DM0 - DM3	Input	**Data Input Mask:** DM0-DM3 are byte specific. Input data is masked when DM is sampled HIGH during a write cycle. DM3 masks DQ31-DQ24, DM2 masks DQ23-DQ16, DM1 masks DQ15-DQ8, and DM0 masks DQ7-DQ0.
DQ0 - DQ31	Input / Output	**Data I/O:** The DQ0-DQ31 input and output data are synchronized with positive and negative edges of DQS0~DQS3. The I/Os are byte-maskable during Writes.
V_{DD}	Supply	**Power Supply:** Power for the input buffers and core logic.
V_{SS}	Supply	**Ground:** Ground for the input buffers and core logic.
V_{DDQ}	Supply	**DQ Power:** Provide isolated power to DQs for improved noise immunity.

V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity.
V_{REF}	Supply	**Reference Voltage for Inputs:** +0.5 x V_{DDQ}
NC	-	**No Connect:** No internal connection, these pins suggest to be left unconnected.

Operation Mode

Table 5 shows the truth table for the operation commands.

Table 5. Truth Table (Note (1), (2))

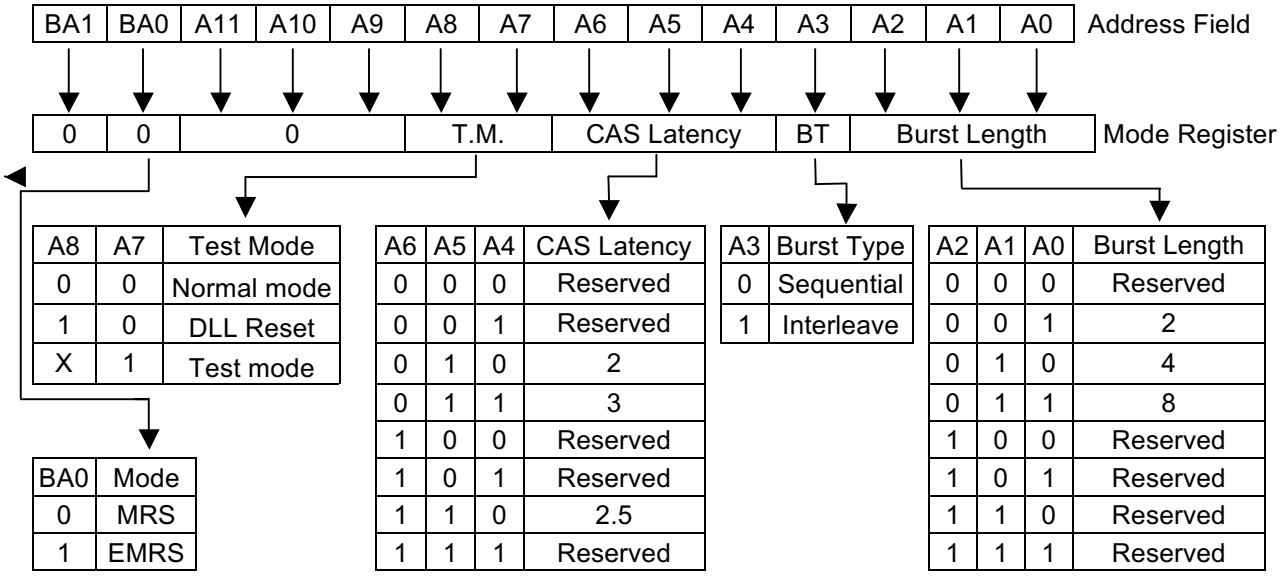
Command	State	CKEn-1	CKEn	DM	BA1	BA0	A8	A11-A9, A7-0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
BankActivate	Idle(3)	H	X	X	V	V	Row Address		L	L	H	H
BankPrecharge	Any	H	X	X	V	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	V	V	V	L	Column Address A0~A7	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	V	V	V	H		L	H	L	L
Read	Active(3)	H	X	X	V	V	L		L	H	L	H
Read and Autoprecharge	Active(3)	H	X	X	V	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	L	L	OP code		L	L	L	L
Extended Mode Register Set	Idle	H	X	X	L	H			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	X	L	H	H	H
Device Deselect	Any	H	X	X	X	X	X	X	H	X	X	X
Burst Stop	Active(4)	H	X	X	X	X	X	X	L	H	H	L
AutoRefresh	Idle	H	H	X	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	X	H	X	X	X
									L	H	H	H
Power Down Mode Entry	Idle/Active(5)	H	L	X	X	X	X	X	H	X	X	X
									L	H	H	H
Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	X	H	X	X	X
									L	H	H	H
Data Mask Enable(6)	Active	H	X	H	X	X	X	X	X	X	X	X
Data Mask Disable	Active	H	X	L	X	X	X	X	X	X	X	X

Note: 1. V = Valid data, X = Don't Care, L = Low level, H = High level
2. CKE_n signal is input level when commands are provided.
CKE_{n-1} signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BA0, BA1signals.
4. Read burst stop with BST command for all burst types.
5. Power Down Mode can not enter in the burst operation.
When this command is asserted in the burst cycle, device state is clock suspend mode.
6. DM0 – DM3 can be enabled respectively.

Mode Register Set (MRS)

The Mode Register stores the data for controlling various operating modes of a DDR SDRAM. It programs CAS Latency, Burst Type, and Burst Length to make the DDR SDRAM useful for a variety of applications. The default value of the Mode Register is not defined; therefore the Mode Register must be written by the user. Values stored in the register will be retained until the register is reprogrammed. The Mode Register is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of address pins A0~A11 and BA0, BA1 in the same cycle in which $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are asserted Low is written into the Mode Register. A minimum of two clock cycles, tMRD, are required to complete the write operation in the Mode Register. The Mode Register is divided into various fields depending on functionality. The Burst Length uses A0~A2, Burst Type uses A3, and CAS Latency (read latency from column address) uses A4~A6. A logic 0 should be programmed to all the undefined addresses to ensure future compatibility. Reserved states should not be used to avoid unknown device operation or incompatibility with future versions. Refer to the table for specific codes for various burst lengths, burst types and CAS latencies.

Table 6. Mode Register Bitmap



A8	A7	Test Mode
0	0	Normal mode
1	0	DLL Reset
X	1	Test mode

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

BA0	Mode
0	MRS
1	EMRS

- Burst Length Field (A2~A0)

  This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 2, 4, and 8.

Table 7. Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

- Addressing Mode Select Field (A3)

  The Addressing Mode can be one of two modes, either Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 2, 4, and 8.

Table 8. Addressing Mode

A3	Addressing Mode
0	Sequential
1	Interleave

- Burst Definition, Addressing Sequence of Sequential and Interleave Mode

Table 9. Burst Address ordering

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
2	X	X	0	0, 1	0, 1
	X	X	1	1, 0	1, 0
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

- CAS Latency Field (A6~A4)

  This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field. t_{CAC} (min) ≤ CAS Latency X t_{CK}

Table 10. CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5 clocks
1	1	1	Reserved

- Test Mode Field (A8~A7)
  These two bits are used to enter the test mode and must be programmed to "00" in normal operation.

Table 11. Test Mode

A8	A7	Test Mode
0	0	Normal mode
1	0	DLL Reset
X	1	Test mode

- (BA0, BA1)

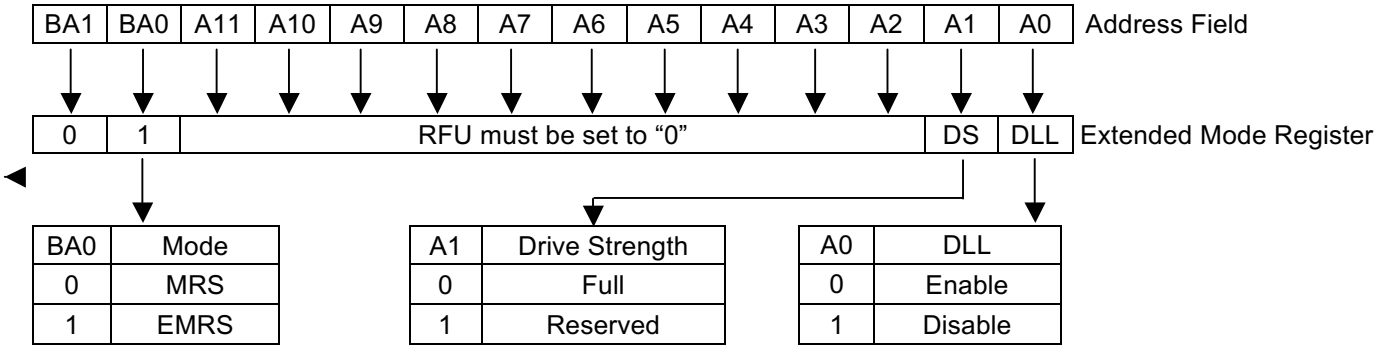
Table 12. MRS/EMRS

BA1	BA0	A11 ~ A0
RFU	0	MRS Cycle
RFU	1	Extended Functions (EMRS)

Extended Mode Register Set (EMRS)

The Extended Mode Register Set stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore must be written after power up for proper operation. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High)The state of A0 ~ A11 and BA1 are written in the mode register in the same cycle as $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ going low. The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. A1 is used for setting driver strength. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. Refer to the table for specific codes.

Table 13. Extended Mode Register Bitmap



BA0	Mode
0	MRS
1	EMRS

A1	Drive Strength
0	Full
1	Reserved

A0	DLL
0	Enable
1	Disable

Table 14. Absolute Maximum Rating

Symbol	Item		Rating	Unit	Note
			-5		
V_{IN}, V_{OUT}	Input, Output Voltage		- 0.5 ~ V_{DDQ}+0.5	V	1,2
V_{DD}, V_{DDQ}	Power Supply Voltage		-1 ~ 3.6	V	1,2
T_A	Ambient Temperature	Commercial	0~70	°C	1
		Industrial	-40~85	°C	1
T_{STG}	Storage Temperature		- 55~150	°C	1
T_{SOLDER}	Soldering Temperature (10s)		260	°C	1
P_D	Power Dissipation		2.0	W	1
I_{OS}	Short Circuit Output Current		50	mA	1

Note1: Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage of the devices
Note2: These voltages are relative to Vss

Table 15. Recommended D.C. Operating Conditions (SSTL_2 In/Out, T_A = -40 ~ 85 °C)

Symbol	Parameter	Min.	Max.	Unit	Note
V_{DD}	Power Supply Voltage	2.3	2.7	V	1
V_{DDQ}	Power Supply Voltage(for I/O)	2.3	2.7	V	1
V_{REF}	Input Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	
V_{TT}	Termination Voltage	V_{REF} – 0.04	V_{REF} + 0.04	V	
$V_{IH(DC)}$	Input High Voltage	V_{REF} + 0.15	V_{DDQ} + 0.3	V	
$V_{IL(DC)}$	Input Low Voltage	V_{SSQ} - 0.3	V_{REF}- 0.15	V	
I_{IL}	Input Leakage Current	- 2	2	μA	
I_{OZ}	Output Leakage Current	- 5	5	μA	
I_{OH}	Output High Current	-16.2	-	mA	V_{OH} = 1.95V
I_{OL}	Output Low Current	16.2	-	mA	V_{OL} = 0.35V

Table 16. Capacitance (V_{DD} = 2.5V, f = 1MHz, T_A = 25 °C)

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Input Capacitance (CK, $\overline{CK}$)	1.5	2.5	pF
C_{IN2}	Input Capacitance (All other input-only pins)	1.5	2.5	pF
$C_{I/O}$	DM, DQ, DQS Input/Output Capacitance	3.5	4.5	pF

Note: These parameters are guaranteed by design, periodically sampled and are not 100% tested.

Table 17. Decoupling Capacitance Guide Line

Symbol	Parameter	Value	Unit
C_{DC1}	Decouping Capacitance between V_{DD} and V_{SS}	0.1+0.01	μF
C_{DC2}	Decouping Capacitance between V_{DDQ} and V_{SSQ}	0.1+0.01	μF

Table 18. D.C. Characteristics (V_{DD}=2.5V ± 0.2V, T_A =-40~85°C)

Parameter & Test Condition	Symbol	-5	Unit
		Max.	
OPERATING CURRENT: One bank; Active-Precharge; t_{RC}=t_{RC} (min); t_{CK}=t_{CK} (min); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0	210	mA
OPERATING CURRENT : One bank; Active-Read-Precharge; BL=4; t_{RC}=t_{RC}(min); t_{CK}=t_{CK}(min); Iout=0mA; Address and control inputs changing once per clock cycle	IDD1	240	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; t_{CK}=t_{CK}(min); CKE=LOW	IDD2P	75	mA
IDLE STANDBY CURRENT : CKE = HIGH; $\overline{CS}$=HIGH(DESELECT); All banks idle; t_{CK}=t_{CK}(min); Address and control inputs changing once per clock cycle; V_{IN}=V_{REF} for DQ, DQS and DM	IDD2N	100	mA
ACTIVE POWER-DOWN STANDBY CURRENT : one bank active; power-down mode; CKE=LOW; t_{CK}=t_{CK}(min)	IDD3P	75	mA
ACTIVE STANDBY CURRENT : $\overline{CS}$=HIGH;CKE=HIGH; one bank active ; t_{RC}=t_{RC}(max);t_{CK}=t_{CK}(min);Address and control inputs changing once per clock cycle; DQ,DQS,and DM inputs changing twice per clock cycle	IDD3N	220	mA
OPERATING CURRENT BURST READ : BL=2; READs; Continuous burst; one bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK}(min); Iout=0mA;50% of data changing on every transfer	IDD4R	420	mA
OPERATING CURRENT BURST Write : BL=2; WRITES; Continuous Burst ;one bank active; address and control inputs changing once per clock cycle; t_{CK}=t_{CK}(min); DQ,DQS,and DM changing twice per clock cycle; 50% of data changing on every transfer	IDD4W	420	mA
AUTO REFRESH CURRENT : t_{RC}=t_{RFC}(min); t_{CK}=t_{CK}(min)	IDD5	300	mA
SELF REFRESH CURRENT: Self Refresh Mode ; CKE≦0.2V;t_{CK}=t_{CK}(min)	IDD6	6	mA
BURST OPERATING CURRENT 4 bank operation: Four bank interleaving READs; BL=4;with Auto Precharge; t_{RC}=t_{RC}(min); t_{CK}=t_{CK}(min); Address and control inputs change only during Active, READ , or WRITE command	IDD7	570	mA

Note:
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage of the device.
2. All voltages are referenced to V_{SS}.
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.
4. Power-up sequence is described in later page.

Table 19. Electrical Characteristics and Recommended A.C. Operating Conditions

(V_{DD} = 2.5V ± 0.2V, T_A = -40~85 °C)

Symbol	Parameter		-5		Unit
			Min.	Max.	
t_{CK}	Clock cycle time	CL = 2	7.5	12	ns
		CL = 2.5	6	12	ns
		CL = 3	5	7.5	ns
t_{CH}	Clock high level width		0.45	0.55	t_{CK}
t_{CL}	Clock low level width		0.45	0.55	t_{CK}
t_{DQSCK}	DQS-out access time from CK, $\overline{CK}$		-0.6	0.6	ns
t_{AC}	Output access time from CK, $\overline{CK}$		-0.7	0.7	ns
t_{DQSQ}	DQS-DQ Skew		-	0.4	ns
t_{RPRE}	Read preamble		0.9	1.1	t_{CK}
t_{RPST}	Read postamble		0.4	0.6	t_{CK}
t_{DQSS}	CK to valid DQS-in		0.72	1.25	t_{CK}
t_{WPRES}	DQS-in setup time		0	-	ns
t_{WPRE}	DQS Write preamble		0.25	-	t_{CK}
t_{WPST}	DQS write postamble		0.4	0.6	t_{CK}
t_{DQSH}	DQS in high level pulse width		0.4	-	t_{CK}
t_{DQSL}	DQS in low level pulse width		0.4	-	t_{CK}
t_{IS}	Address and Control input setup time		0.7	-	ns
t_{IH}	Address and Control input hold time		0.7	-	ns
t_{DS}	DQ & DM setup time to DQS		0.4	-	ns
t_{DH}	DQ & DM hold time to DQS		0.4	-	ns
t_{HP}	Clock half period		t_{CLMIN} or t_{CHMIN}	-	ns
t_{QH}	DQ/DQS output hold time from DQS		t_{HP} - t_{QHS}	-	ns
t_{RC}	Row cycle time		55	-	ns
t_{RFC}	Refresh row cycle time		70	-	ns
t_{RAS}	Row active time		40	100K	ns
t_{RCD}	Active to Read or Write delay		15	-	ns
t_{RP}	Row precharge time		15	-	ns
t_{RRD}	Row active to Row active delay		2	-	t_{CK}
t_{WR}	Write recovery time		3	-	t_{CK}
t_{MRD}	Mode register set cycle time		2	-	t_{CK}
t_{DAL}	Auto precharge write recovery + Precharge time		t_{WR} + t_{RP}	-	t_{CK}
t_{XSRD}	Self refresh exit to read command delay		200	-	t_{CK}
t_{PDEX}	Power down exit time		t_{CK} + t_{IS}	-	ns
t_{REFI}	Average Refresh interval time		-	15.6	µs
t_{IPW}	Control and Address input pulse width		2.2	-	ns
t_{DIPW}	DQ & DM input pulse width (for each input)		1.75	-	ns
t_{HZ}	Data-out high-impedance window from CK/$\overline{CK}$		-	0.7	ns
t_{LZ}	Data-out low-impedance window from CK/$\overline{CK}$		-0.7	0.7	ns
t_{QHS}	Data Hold Skew Factor		-	0.5	ns
DVW	Output data valid window		t_{QH} - t_{DQSQ}	-	ns
t_{XSNR}	Exit Self-Refresh to non-Read command		75	-	ns
t_{CCD}	CAS# to CAS# Delay time		1	-	t_{CK}
t_{DSS}	DQS falling edge to CK setup time		0.2	-	t_{CK}
t_{DSH}	DQS falling edge hold time from CK		0.2	-	t_{CK}

Table 20. Recommended A.C. Operating Conditions (T_A = -40~85 °C, V_{DD}=2.5V ± 0.2V)

Parameter	Symbol	-5		Unit
		Min.	Max.	
Input High Voltage (AC)	V_{IH} (AC)	V_{REF} + 0.31	-	V
Input Low Voltage (AC)	V_{IL} (AC)	-	V_{REF} – 0.31	V
Input Different Voltage, CK and $\overline{CK}$ inputs	V_{ID} (AC)	0.7	V_{DDQ} + 0.6	V
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	V_{IX} (AC)	0.5*V_{DDQ}-0.2	0.5*V_{DDQ}+0.2	V

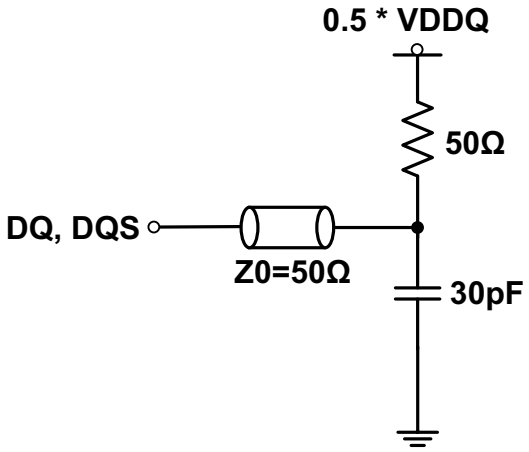
Note:

1. All voltages are referenced to V_{SS}.
2. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.
3. Power-up sequence is described in Note 5.
4. A.C. Test Conditions

Table 21. SSTL_2 Interface

Reference Level of Output Signals (V_{REF})	0.5 * V_{DDQ}
Output Load	Reference to the Test Load
Input Signal Levels	V_{REF}+0.31 V / V_{REF}-0.31 V
Input Signals Slew Rate	1 V/ns
Reference Level of Input Signals	0.5 * V_{DDQ}

Figure 3. SSTL_2 A.C. Test Load



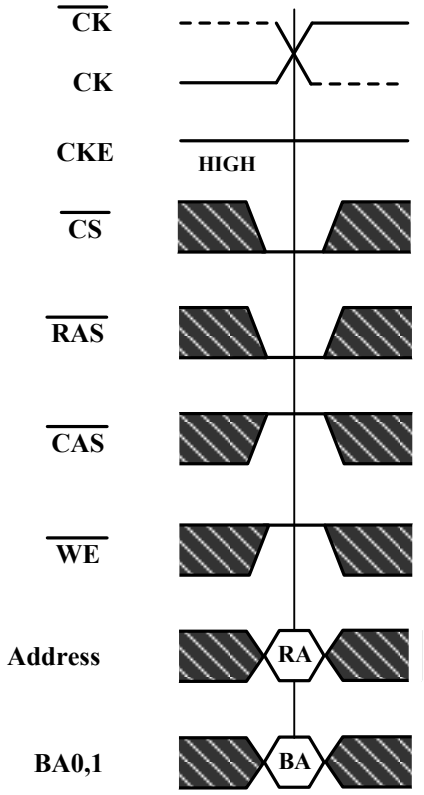
5. **Power up Sequence**

Power up must be performed in the following sequence.

1) Apply power to V_{DD} before or at the same time as V_{DDQ}, V_{TT} and V_{REF} when all input signals are held "NOP" state and maintain CKE “LOW”.
2) Start clock and maintain stable condition for minimum 200us.
3) Issue a “NOP” command and keep CKE “HIGH”
4) Issue a “Precharge All” command.
5) Issue EMRS – enable DLL.
6) Issue MRS – reset DLL. (An additional 200 clock cycles are required to lock the DLL).
7) Precharge all banks of the device.
8) Issue two or more Auto Refresh commands.
9) Issue MRS – with A8 to low to initialize the mode register.

Timing Waveforms

Figure 4. Activating a Specific Row in a Specific Bank



RA=Row Address

BA=Bank Address

Don't Care

Figure 5. tRCD and tRRD Definition

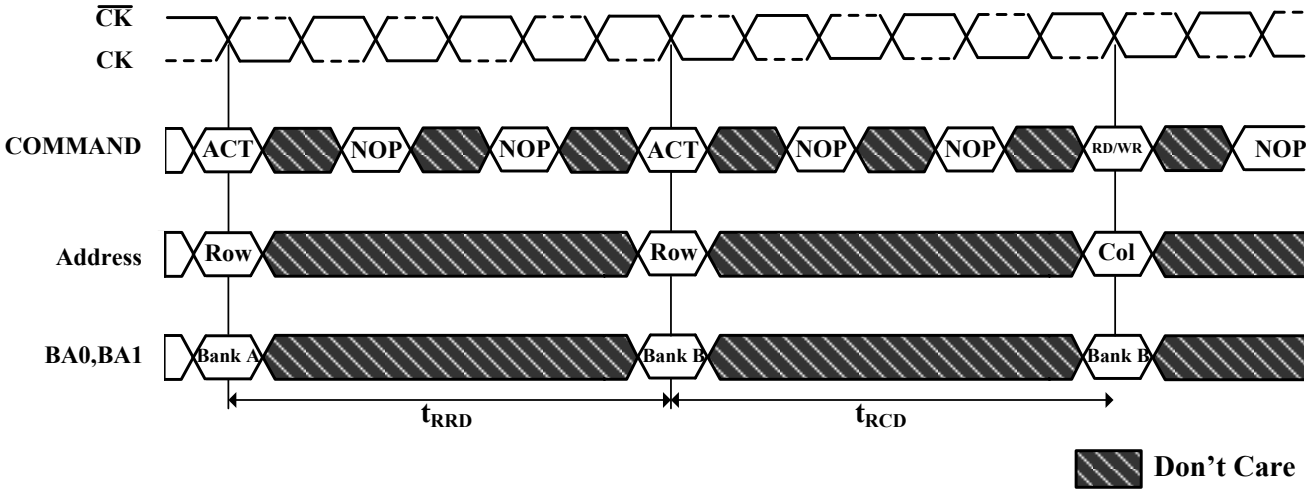
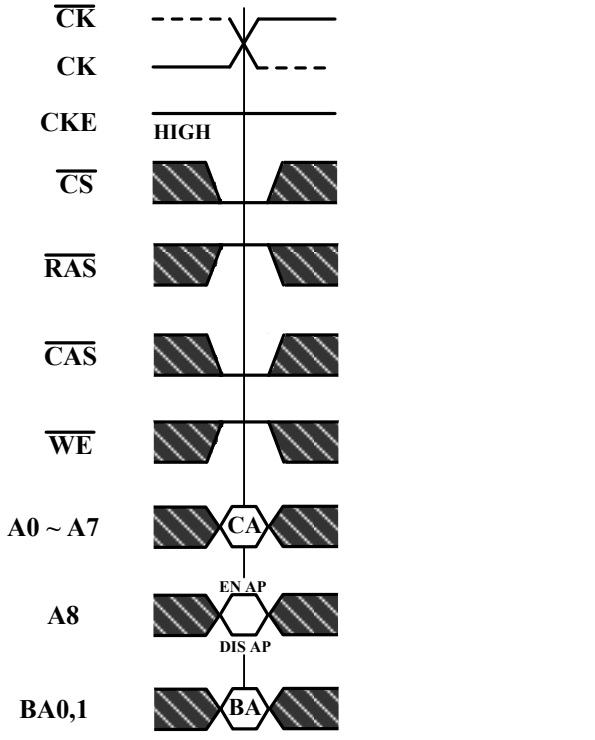


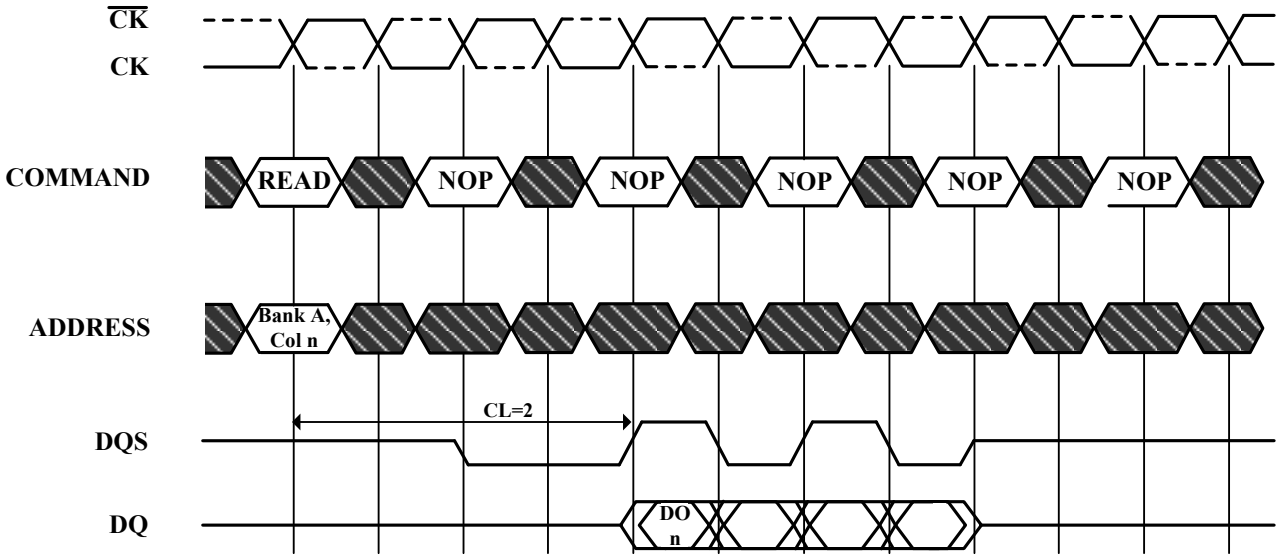
Figure 6. READ Command



CA=Column Address
BA=Bank Address
EN AP=Enable Autoprecharge
DIS AP=Disable Autoprecharge

Don't Care

Figure 7. Read Burst Required CAS Latencies (CL=2)



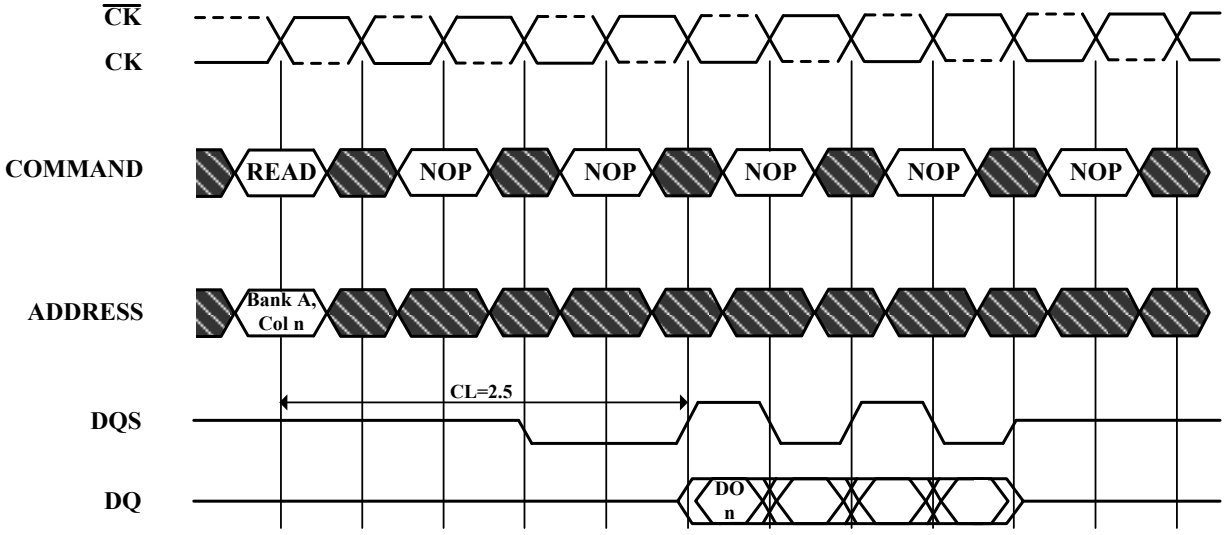
DO n=Data Out from column n

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n

Don't Care

Read Burst Required CAS Latencies (CL=2.5)



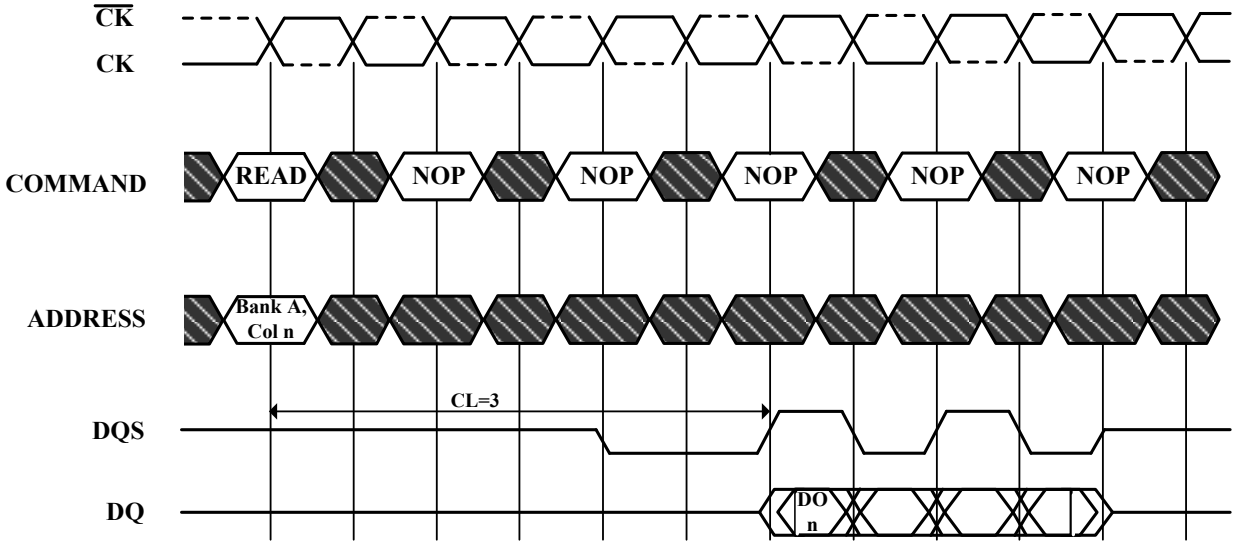
DO n=Data Out from column n

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n

Don't Care

Read Burst Required CAS Latencies (CL=3)



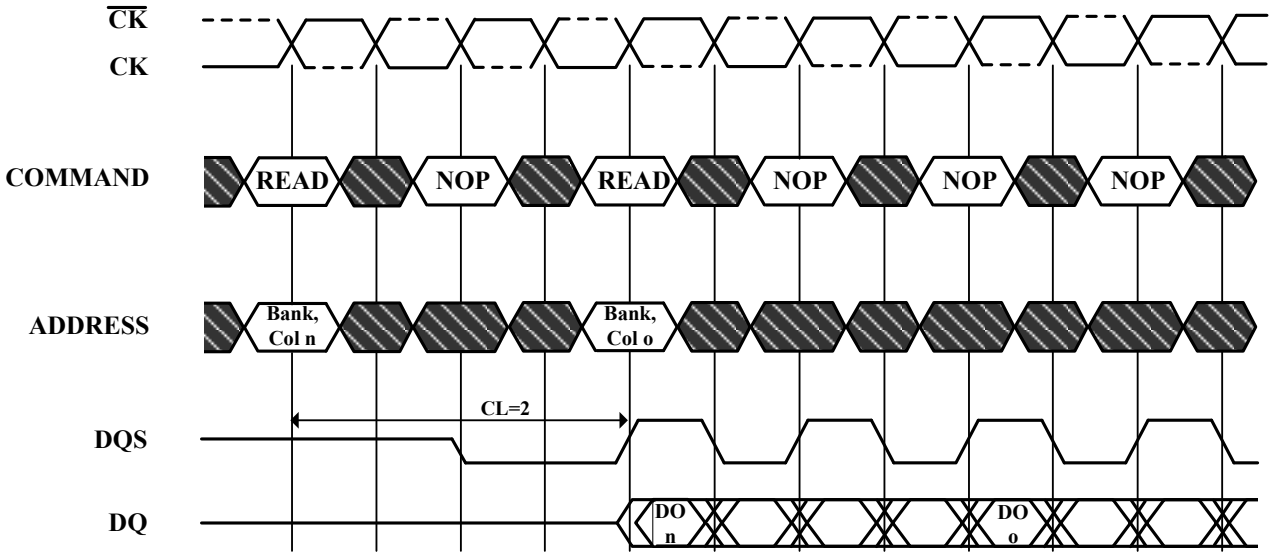
DO n=Data Out from column n

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n

Don't Care

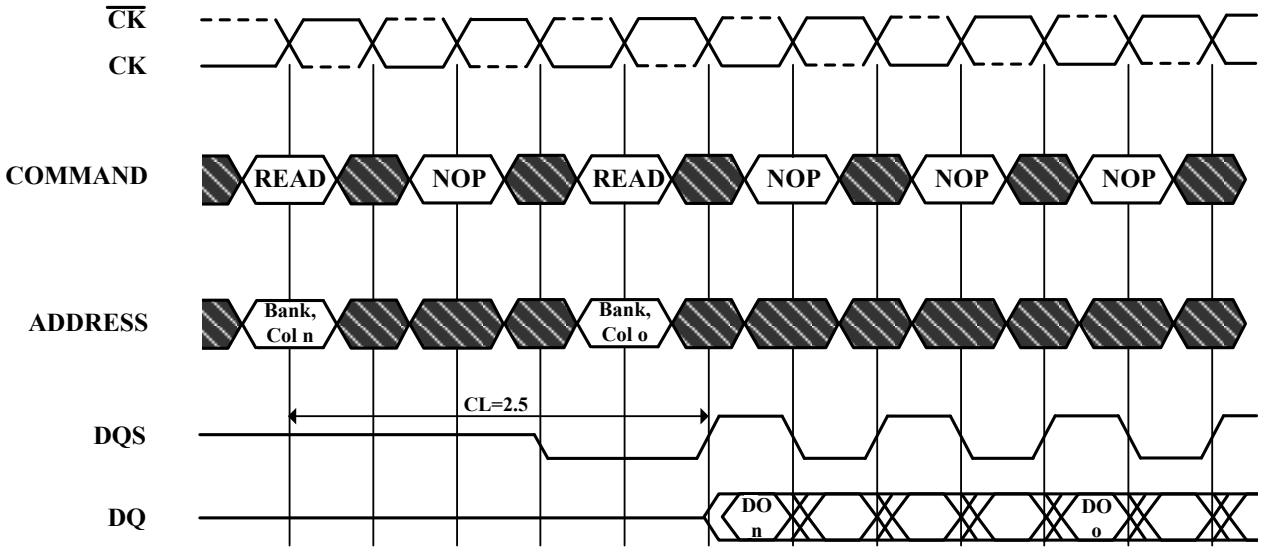
Figure 8. Consecutive Read Bursts Required CAS Latencies (CL=2)



DO n (or o)=Data Out from column n (or column o)
Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o
Read commands shown must be to the same device

Don't Care

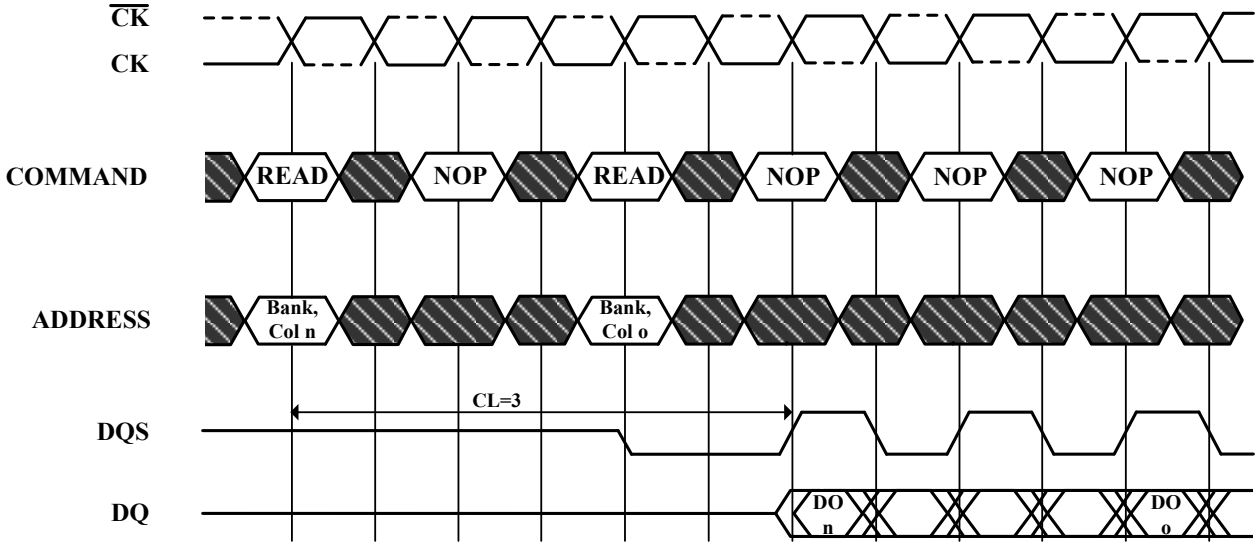
Consecutive Read Bursts Required CAS Latencies (CL=2.5)



DO n (or o)=Data Out from column n (or column o)
Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o
Read commands shown must be to the same device

Don't Care

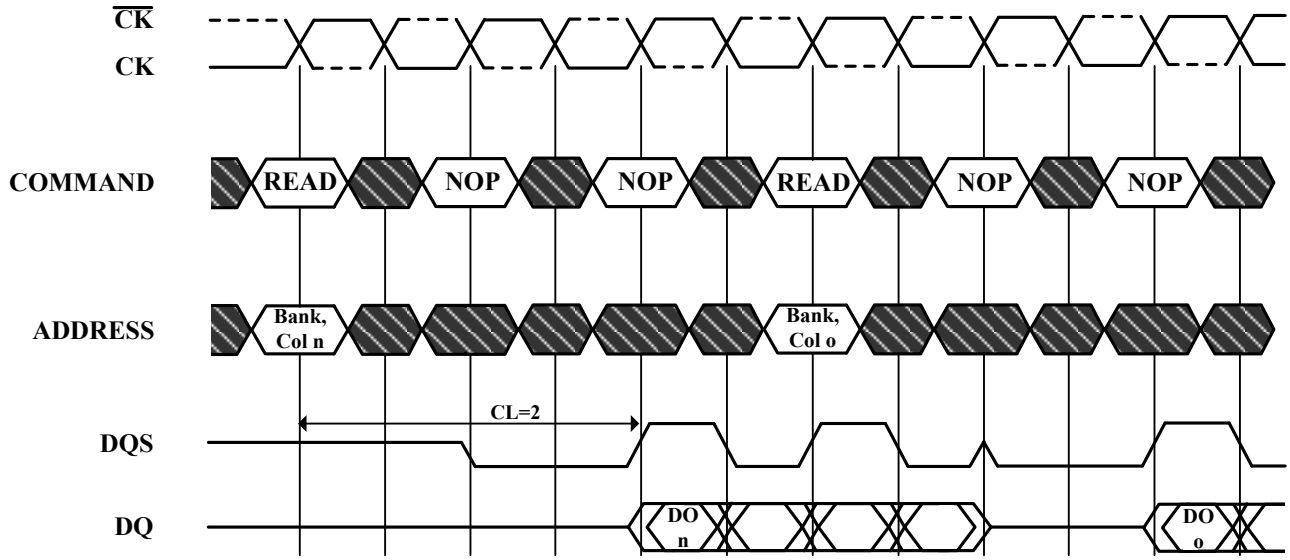
Consecutive Read Bursts Required CAS Latencies (CL=3)



DO n (or o)=Data Out from column n (or column o)
Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o
Read commands shown must be to the same device

Don't Care

Figure 9. Non-Consecutive Read Bursts Required CAS Latencies (CL=2)



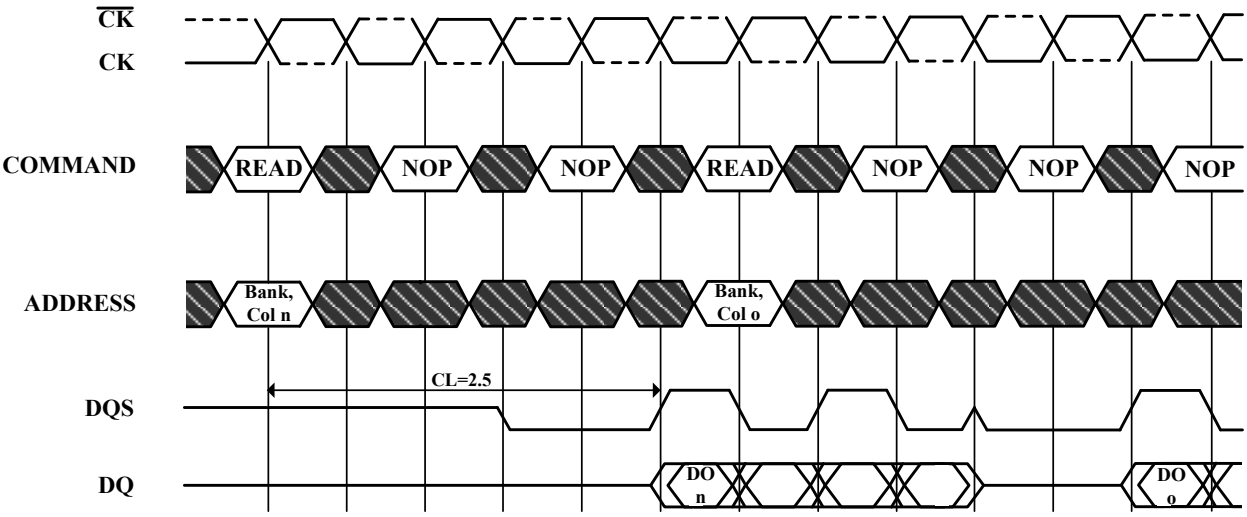
DO n (or o)=Data Out from column n (or column o)

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO o)

Don't Care

Non-Consecutive Read Bursts Required CAS Latencies (CL=2.5)



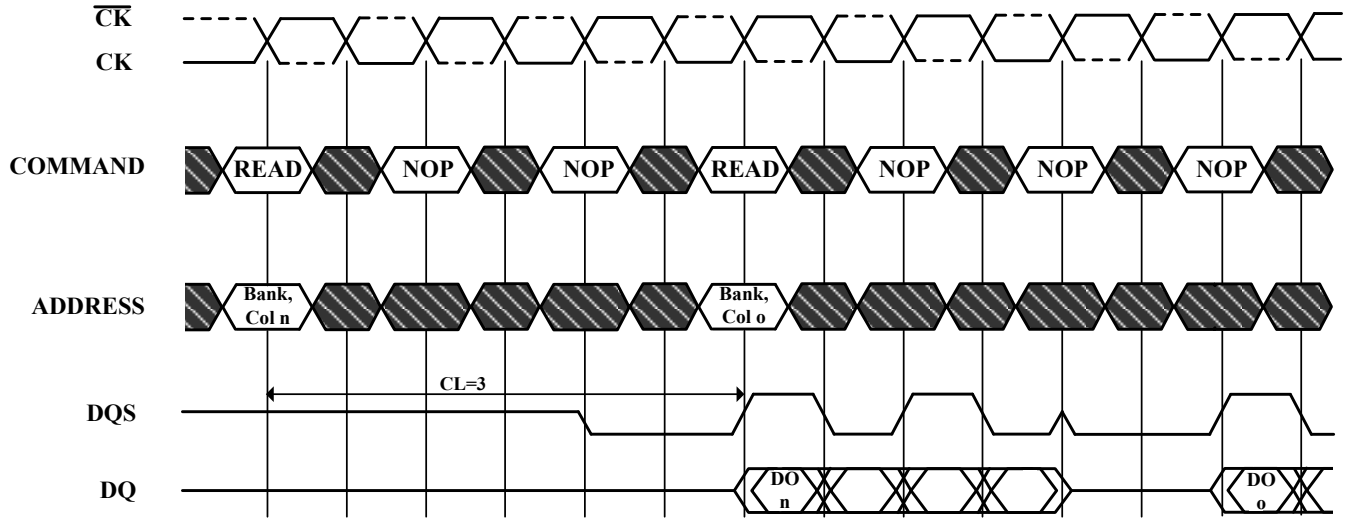
DO n (or o)=Data Out from column n (or column o)

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO o)

Don't Care

Non-Consecutive Read Bursts Required CAS Latencies (CL=3)



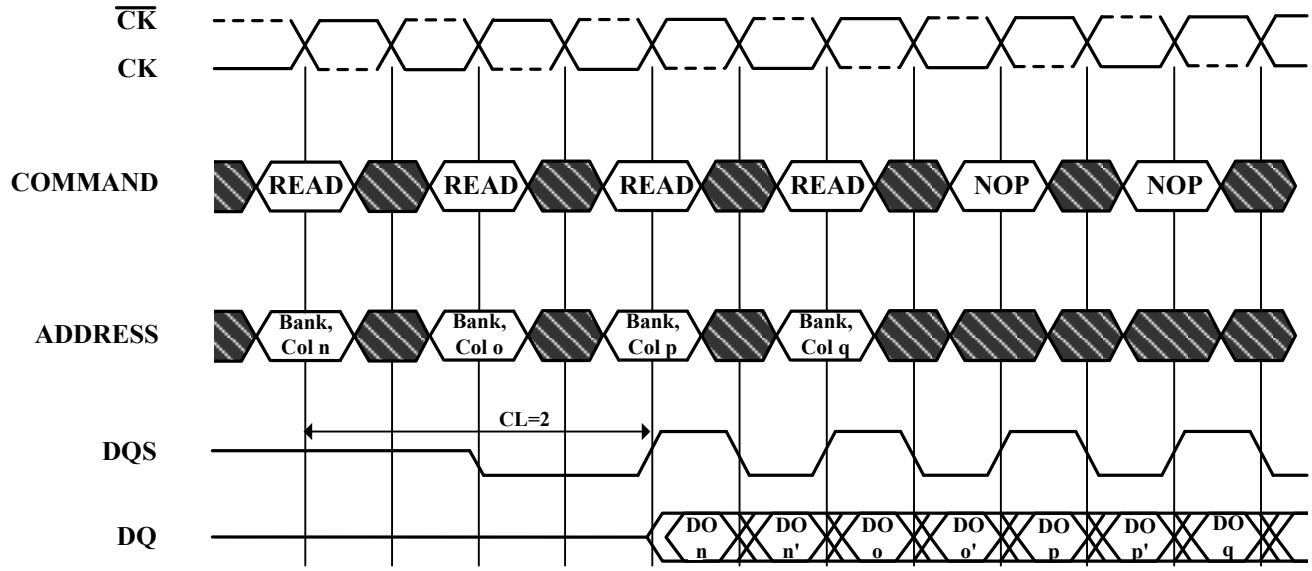
DO n (or o)=Data Out from column n (or column o)

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO o)

Don't Care

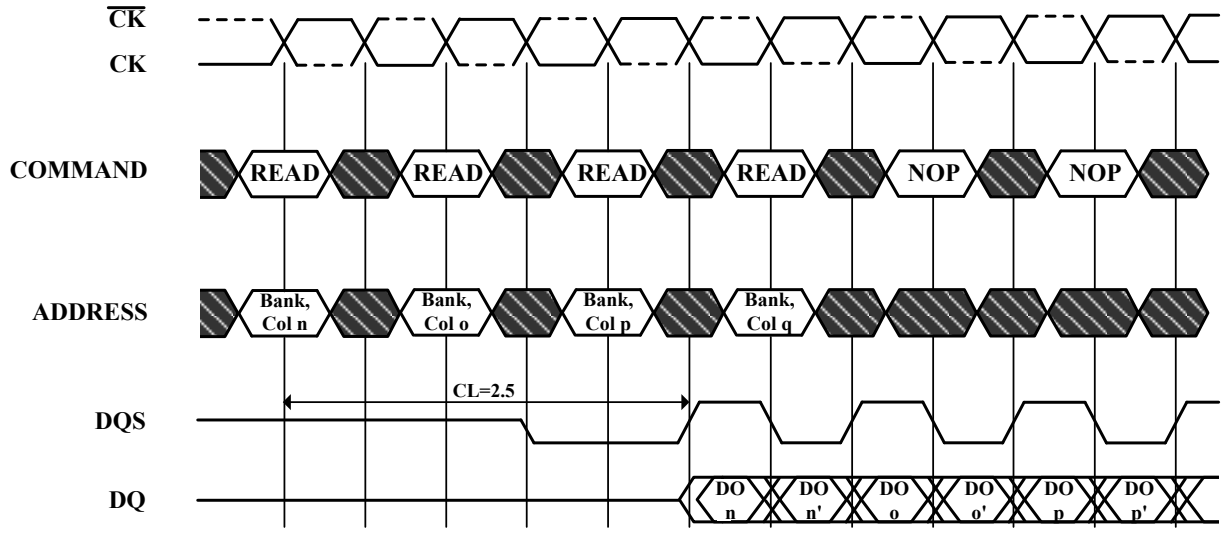
Figure 10. Random Read Accesses Required CAS Latencies (CL=2)



DO n, etc. =Data Out from column n, etc.
n', etc. =the next Data Out following DO n, etc. according to the programmed burst order
Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted
Reads are to active rows in any banks

Don't Care

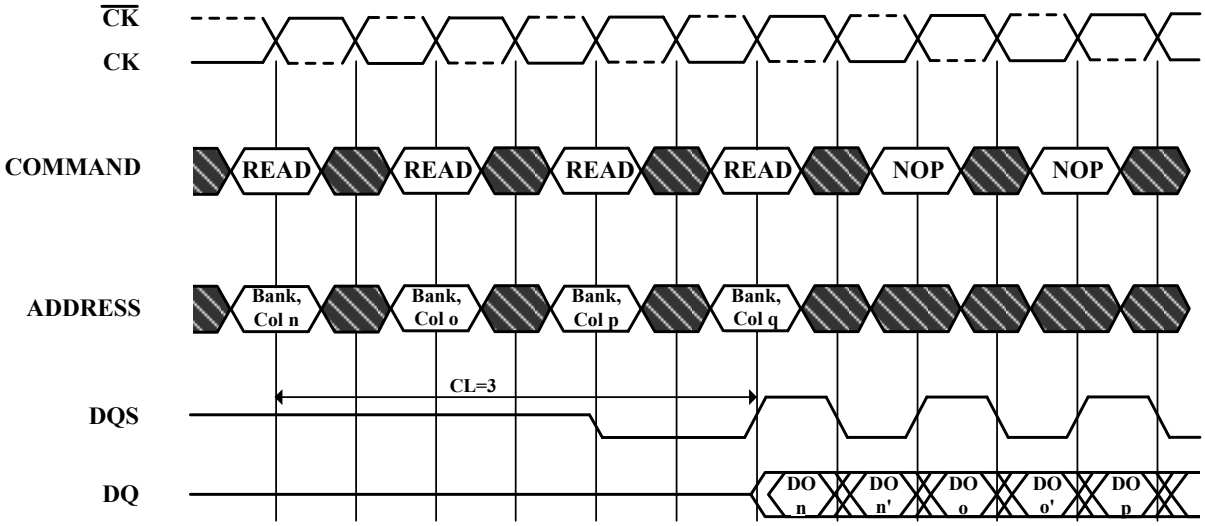
Random Read Accesses Required CAS Latencies (CL=2.5)



DO n, etc. =Data Out from column n, etc.
n', etc. =the next Data Out following DO n, etc. according to the programmed burst order
Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted
Reads are to active rows in any banks

Don't Care

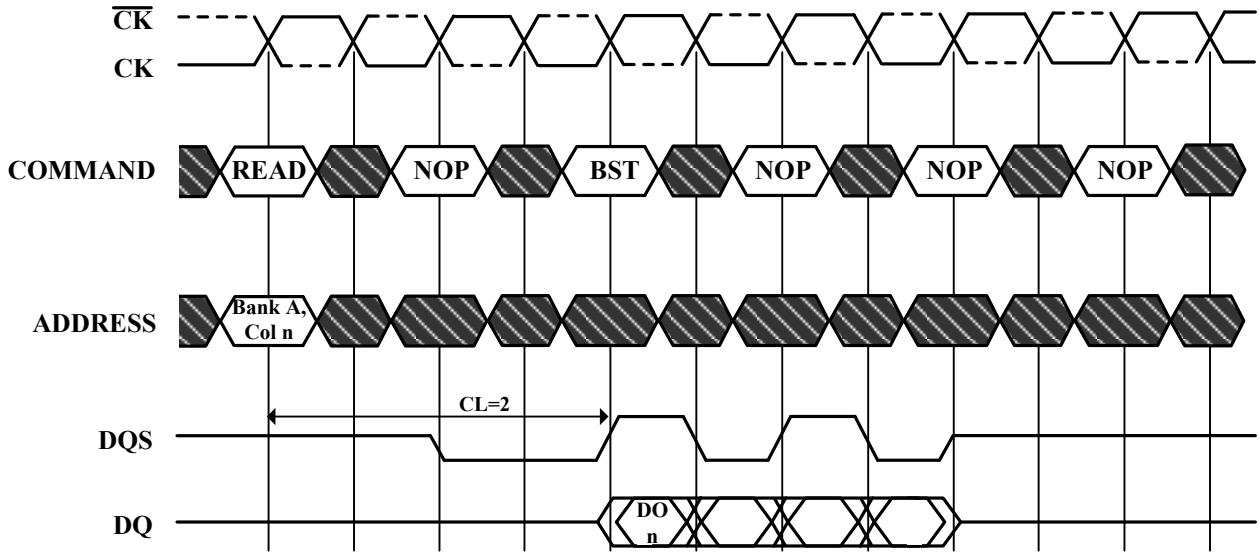
Random Read Accesses Required CAS Latencies (CL=3)



DO n, etc. =Data Out from column n, etc.
n', etc. =the next Data Out following DO n, etc. according to the programmed burst order
Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted
Reads are to active rows in any banks

Don't Care

Figure 11. Terminating a Read Burst Required CAS Latencies (CL=2)



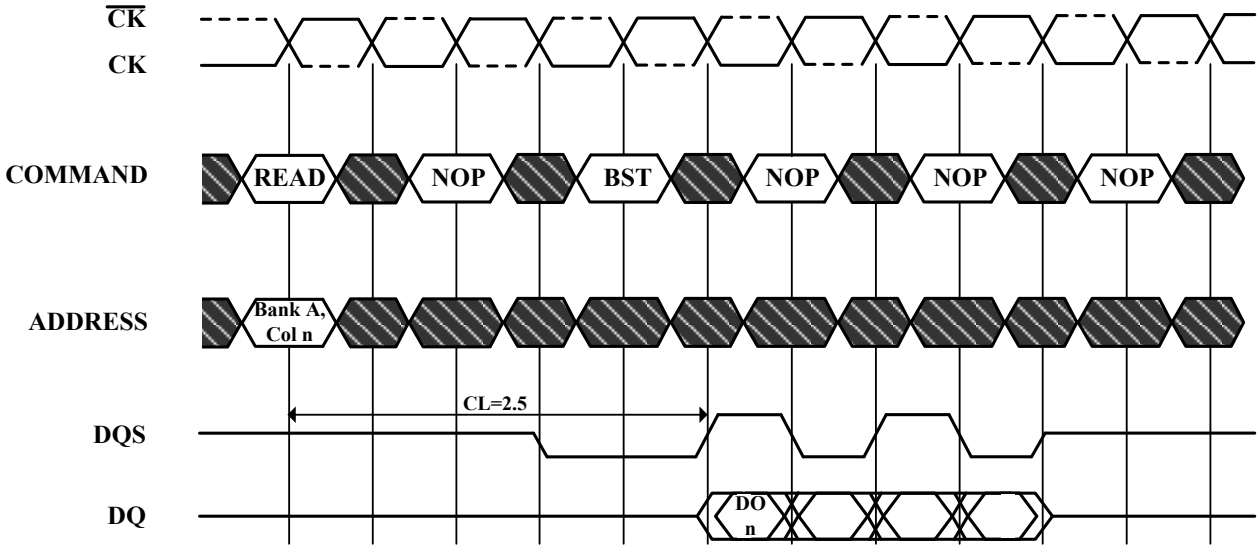
DO n = Data Out from column n

Cases shown are bursts of 8 terminated after 4 data elements

3 subsequent elements of Data Out appear in the programmed order following DO n

Don't Care

Terminating a Read Burst Required CAS Latencies (CL=2.5)



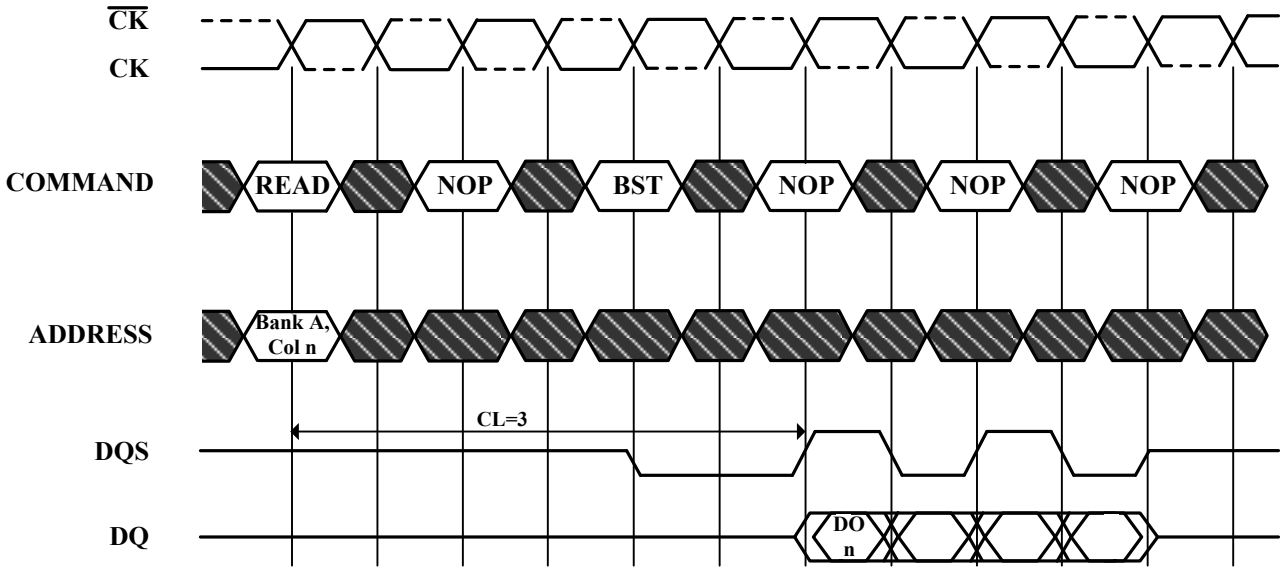
DO n = Data Out from column n

Cases shown are bursts of 8 terminated after 4 data elements

3 subsequent elements of Data Out appear in the programmed order following DO n

Don't Care

Terminating a Read Burst Required CAS Latencies (CL=3)



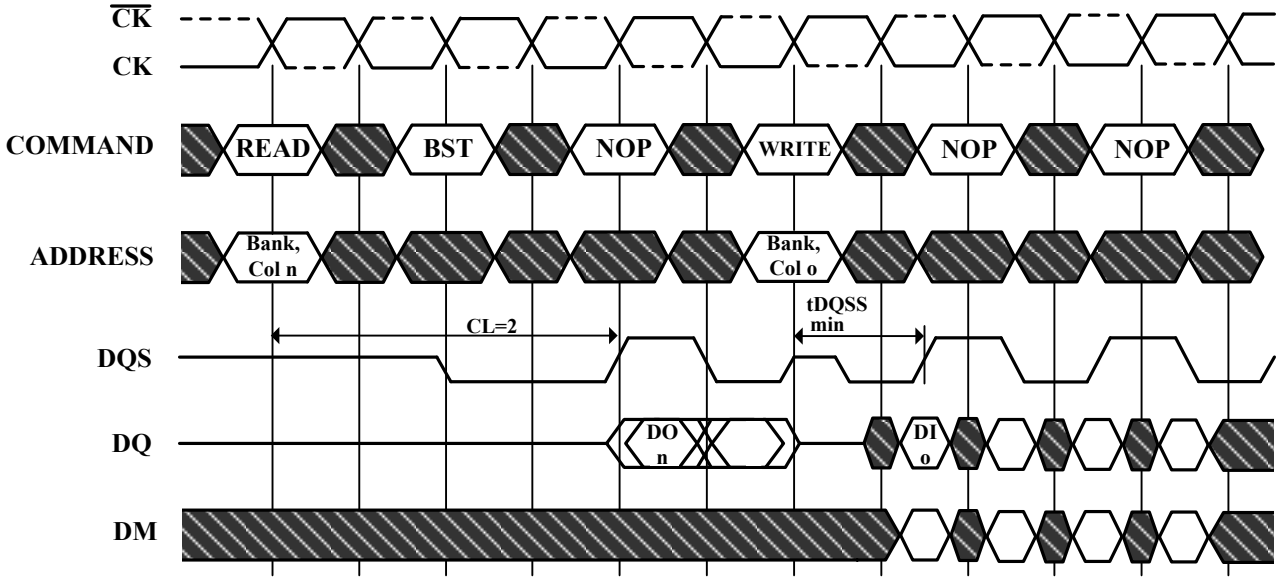
DO n = Data Out from column n

Cases shown are bursts of 8 terminated after 4 data elements

3 subsequent elements of Data Out appear in the programmed order following DO n

Don't Care

Figure 12. Read to Write Required CAS Latencies (CL=2)



DO n (or o)= Data Out from column n (or column o)

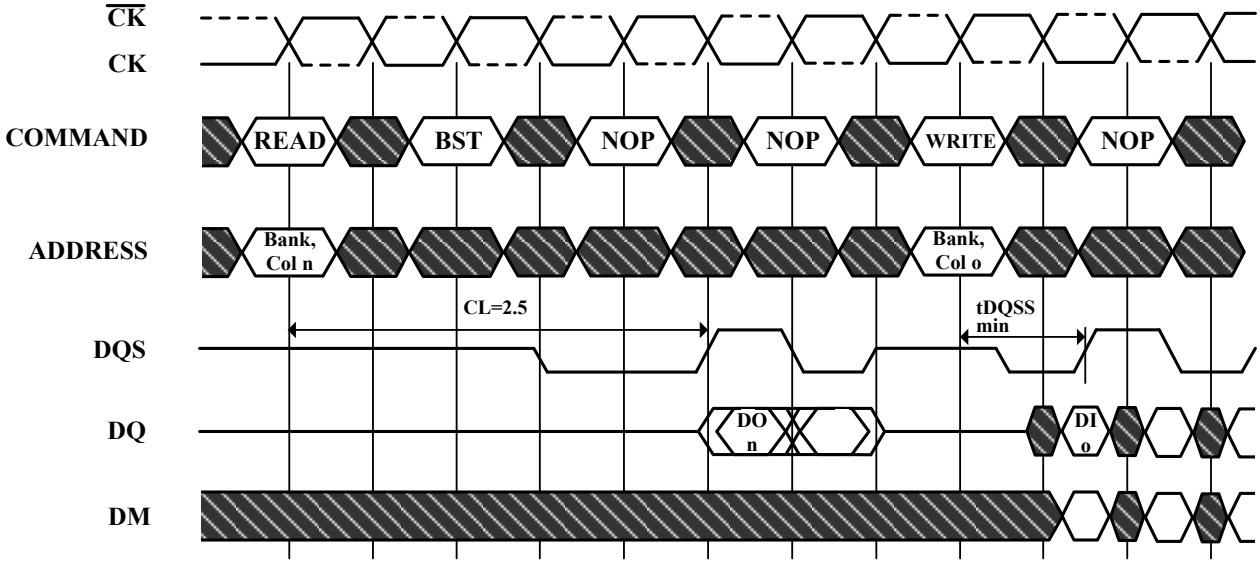
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

Don't Care

Read to Write Required CAS Latencies (CL=2.5)



DO n (or o)= Data Out from column n (or column o)

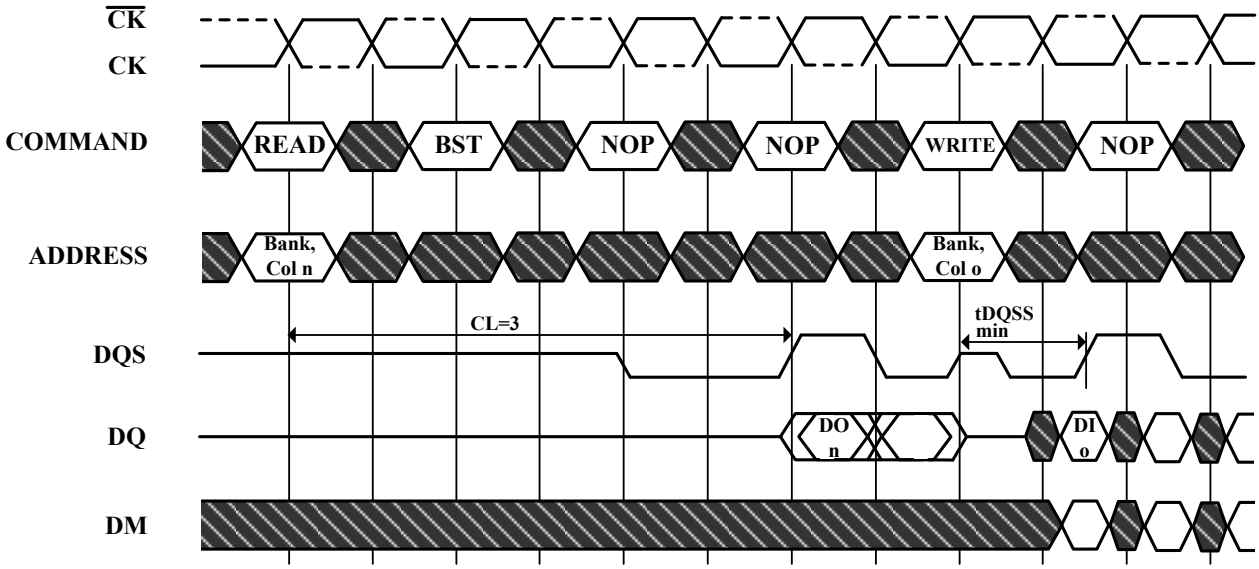
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

Don't Care

Read to Write Required CAS Latencies (CL=3)



DO n (or o)= Data Out from column n (or column o)

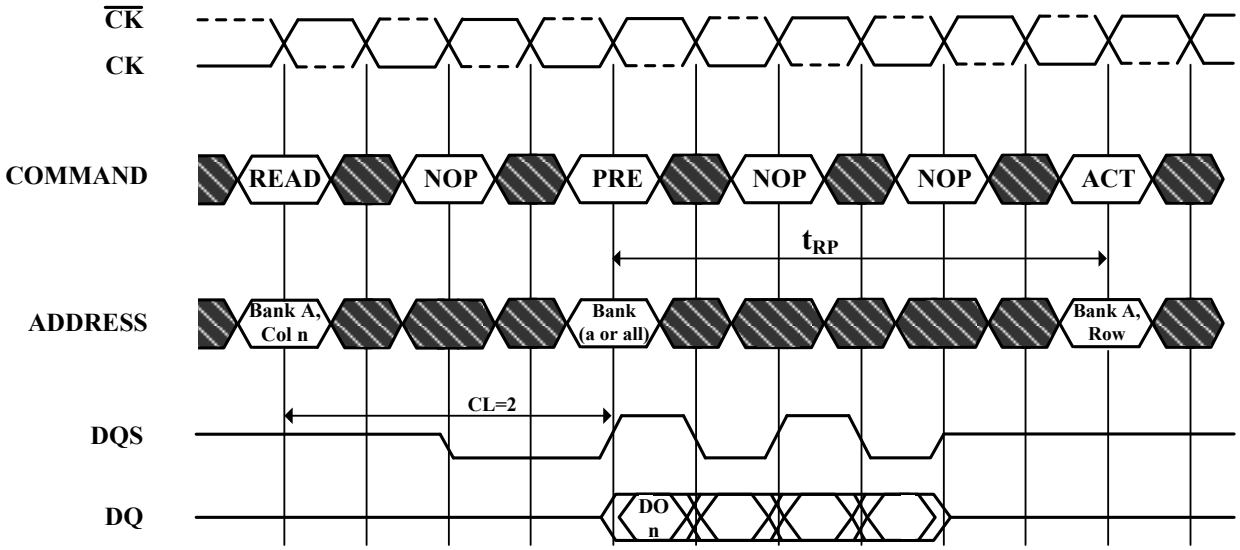
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

Don't Care

Figure 13. Read to Precharge Required CAS Latencies (CL=2)



DO n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8

3 subsequent elements of Data Out appear in the programmed order following DO n

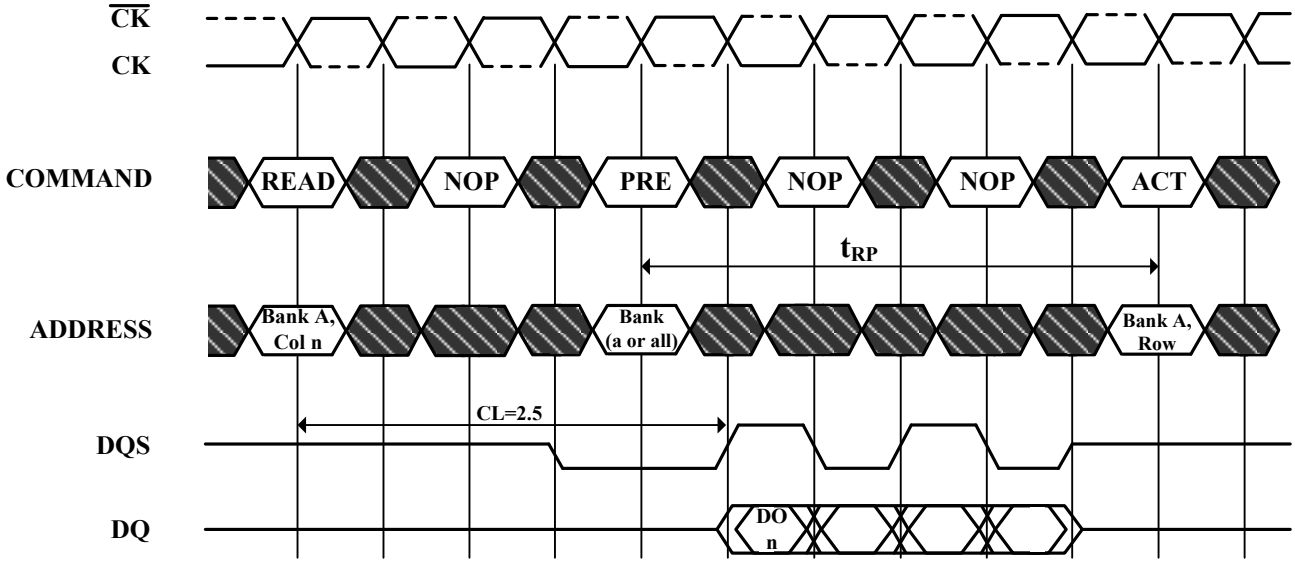
Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

The Active command may be applied if tRC has been met

Don't Care

Read to Precharge Required CAS Latencies (CL=2.5)



DO n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8

3 subsequent elements of Data Out appear in the programmed order following DO n

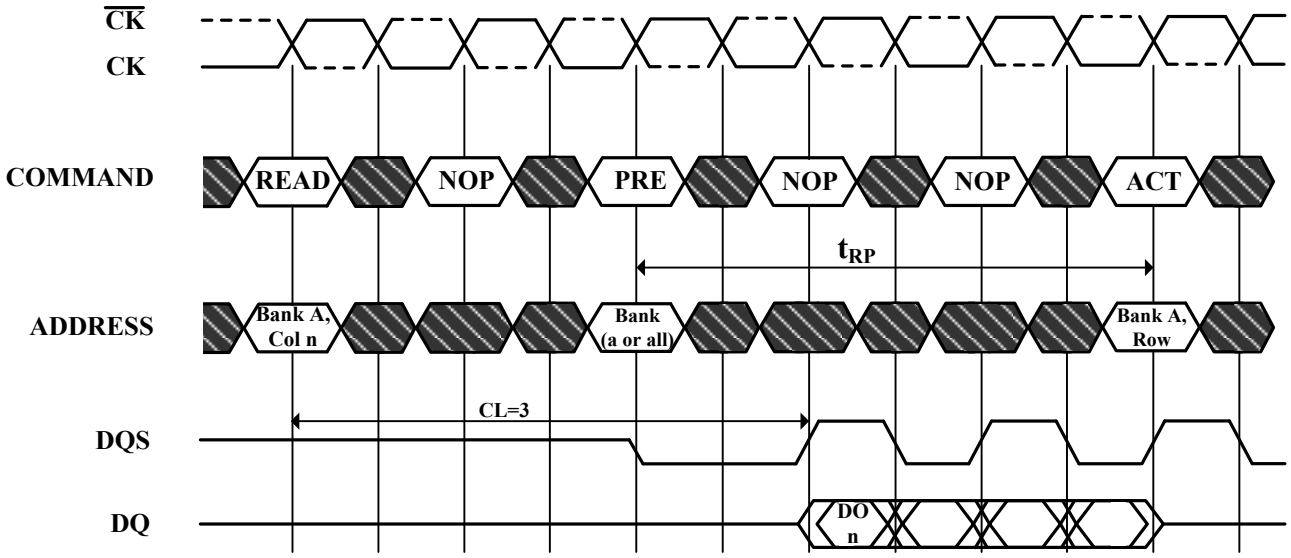
Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

The Active command may be applied if tRC has been met

Don't Care

Read to Precharge Required CAS Latencies (CL=3)



DO n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8

3 subsequent elements of Data Out appear in the programmed order following DO n

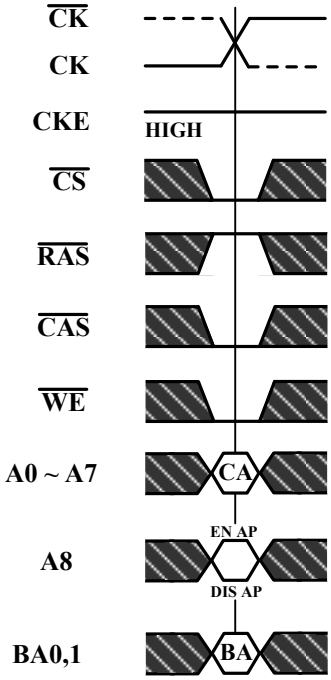
Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

The Active command may be applied if tRC has been met

Don't Care

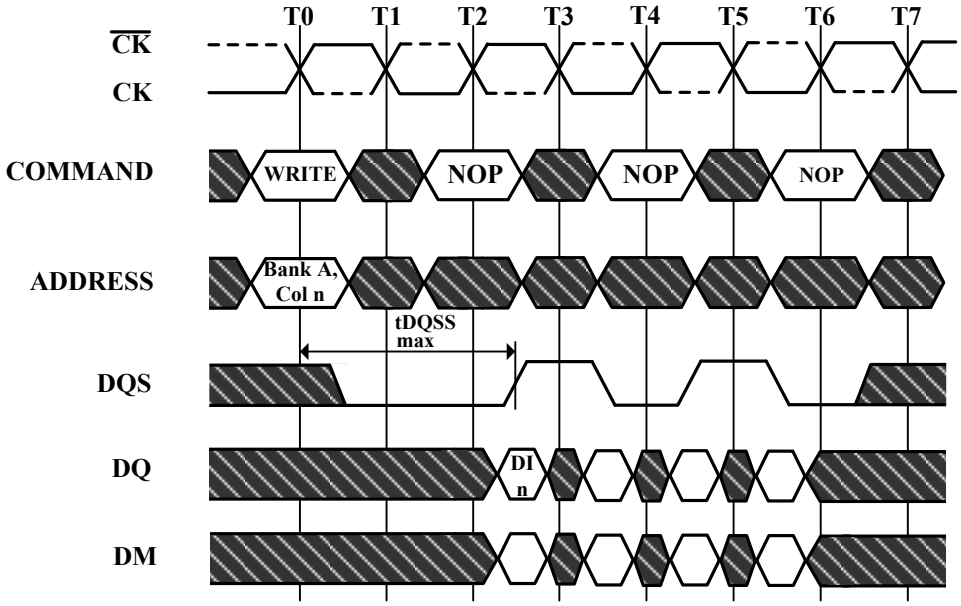
Figure 14. Write Command



CA=Column Address
BA=Bank Address
EN AP=Enable Autoprecharge
DIS AP=Disable Autoprecharge

Don't Care

Figure 15. Write Max DQSS



DI n = Data In for column n

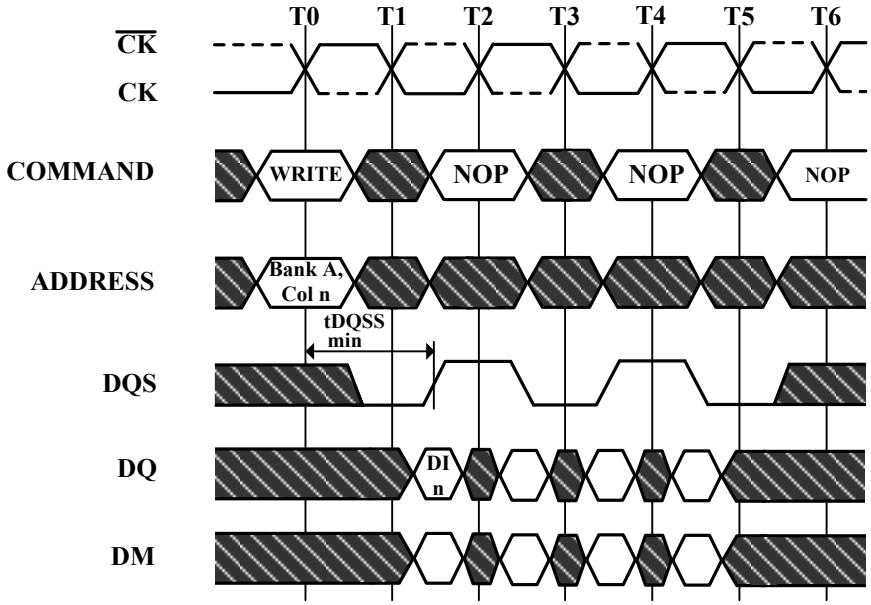
3 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A8 is LOW with the WRITE command (AUTO PRECHARGE disabled)

Don't Care

Figure 16. Write Min DQSS



DI n = Data In for column n

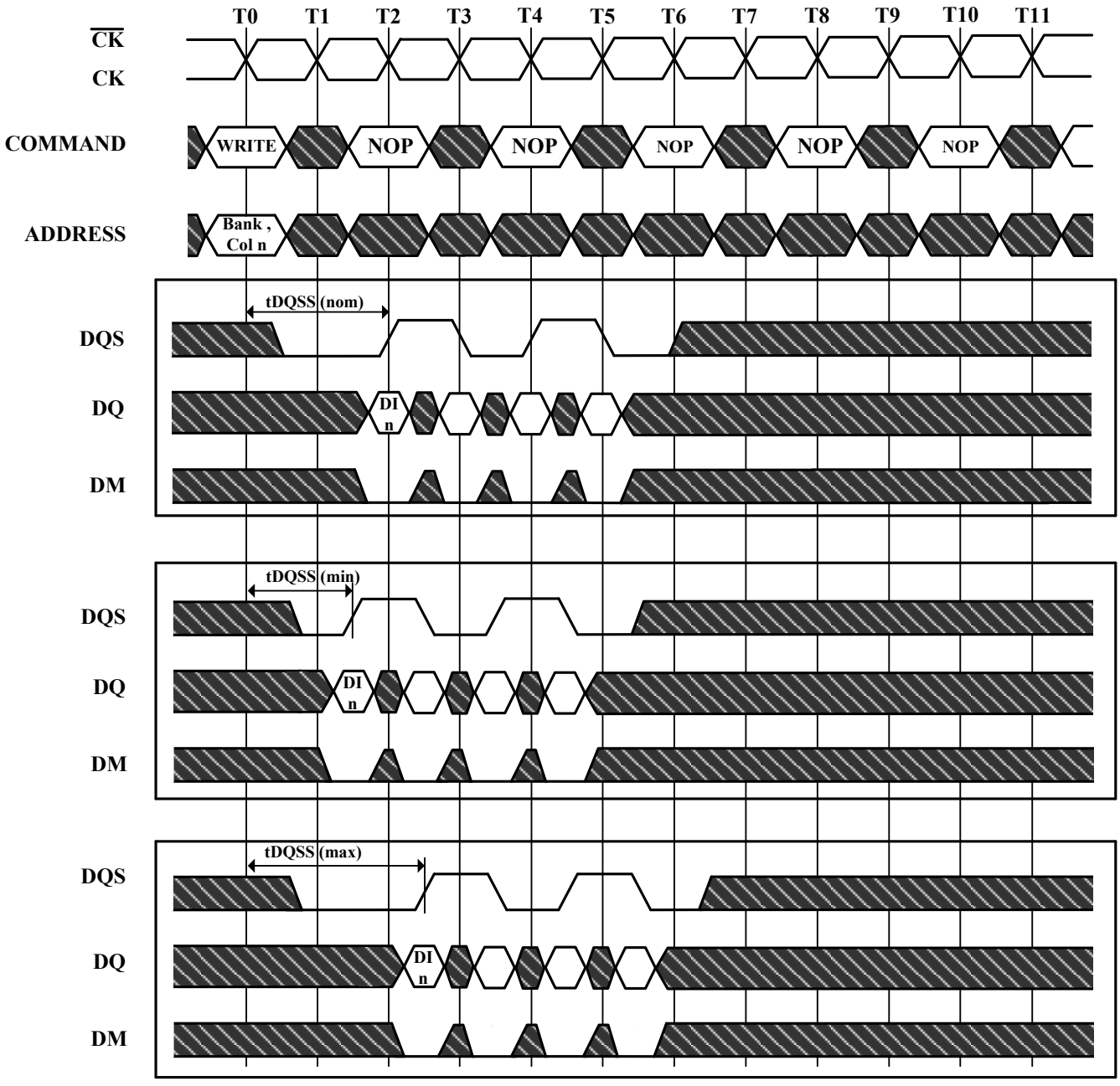
3 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A8 is LOW with the WRITE command (AUTO PRECHARGE disabled)

Don't Care

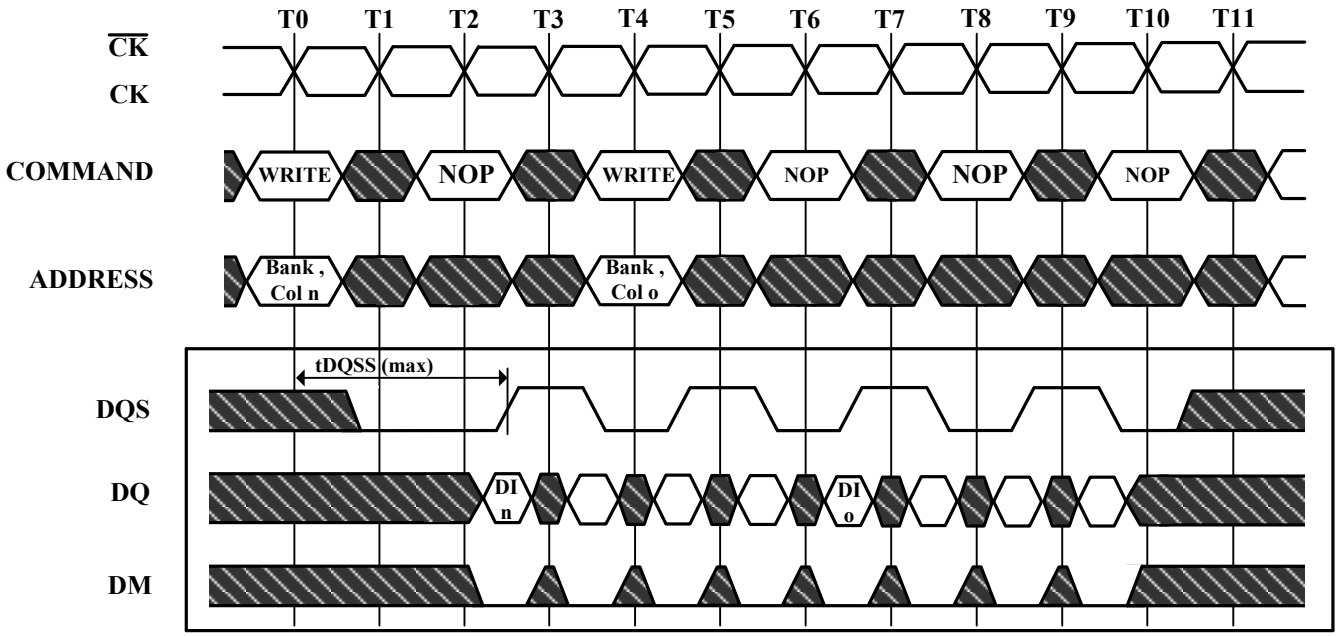
Figure 17. Write Burst Nom, Min, and Max tDQSS



DI n = Data In for column n
3 subsequent elements of Data are applied in the programmed order following DI n
A non-interrupted burst of 4 is shown
A8 is LOW with the WRITE command (AUTO PRECHARGE disabled)
DM=DM0 ~ DM3

Don't Care

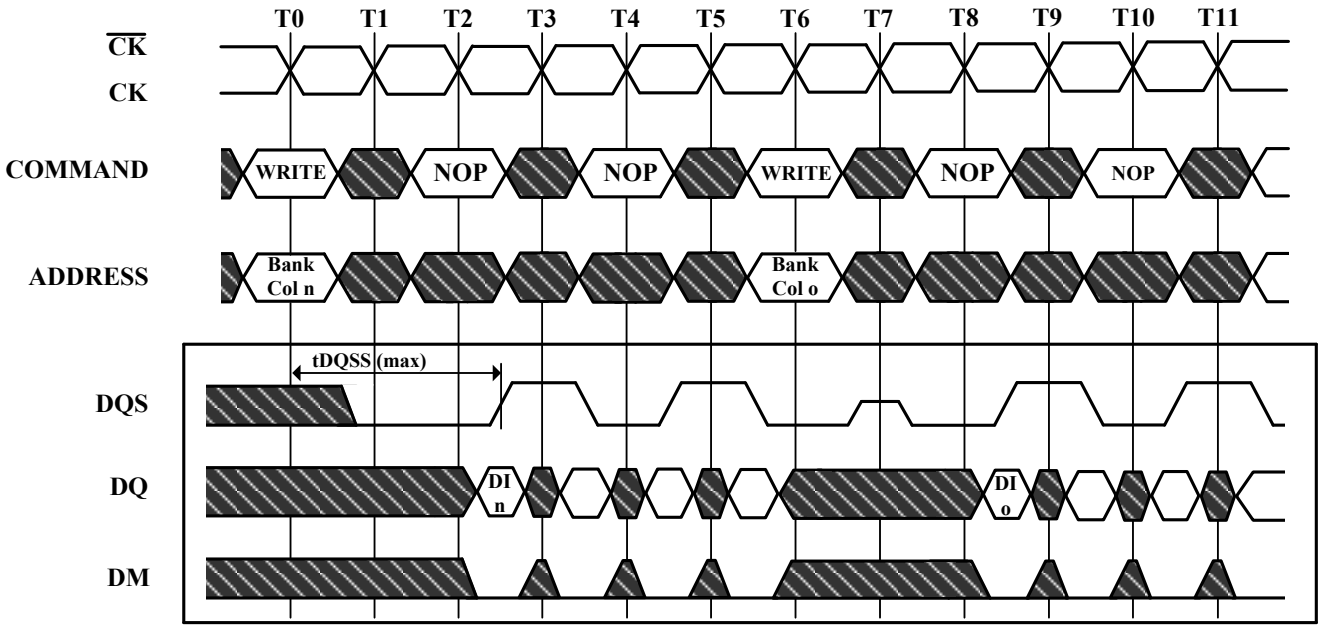
Figure 18. Write to Write Max tDQSS



DI n , etc. = Data In for column n,etc.
3 subsequent elements of Data In are applied in the programmed order following DI n
3 subsequent elements of Data In are applied in the programmed order following DI o
Non-interrupted bursts of 4 are shown
DM= DM0 ~ DM3

Don't Care

Figure 19. Write to Write Max tDQSS, Non Consecutive



DI n, etc. = Data In for column n, etc.

3 subsequent elements of Data In are applied in the programmed order following DI n

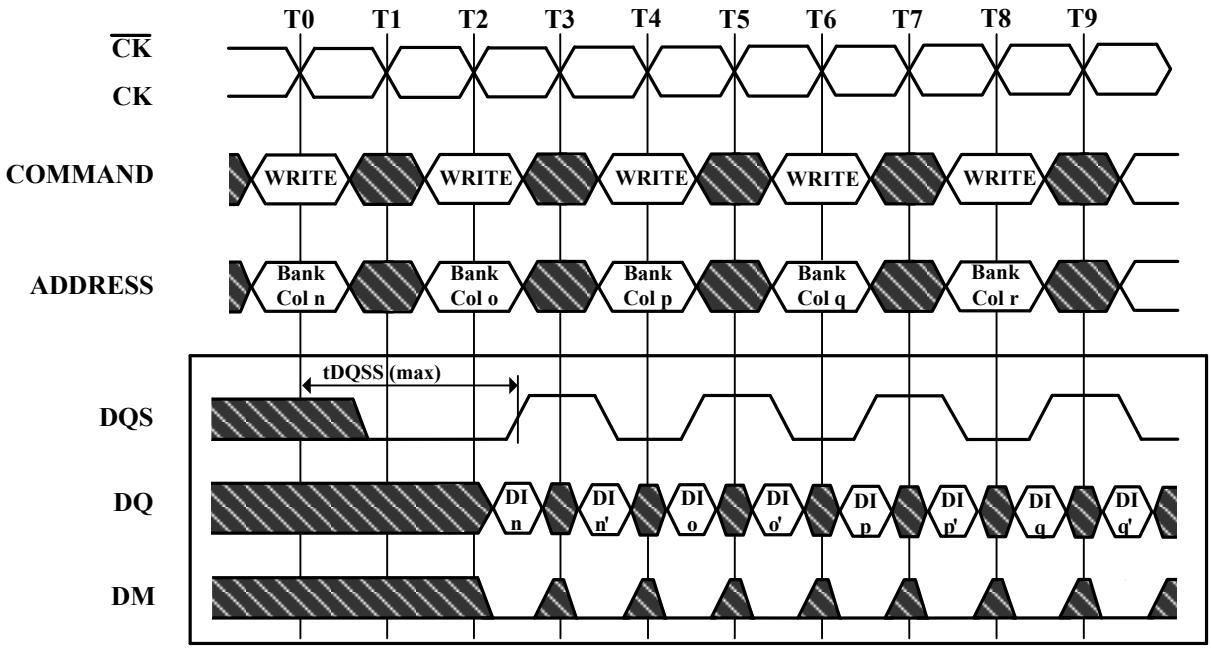
3 subsequent elements of Data In are applied in the programmed order following DI o

Non-interrupted bursts of 4 are shown

DM= DM0 ~ DM3

Don't Care

Figure 20. Random Write Cycles Max tDQSS



DI n, etc. = Data In for column n, etc.

n', etc. = the next Data In following DI n, etc. according to the programmed burst order

Programmed Burst Length 2, 4, or 8 in cases shown

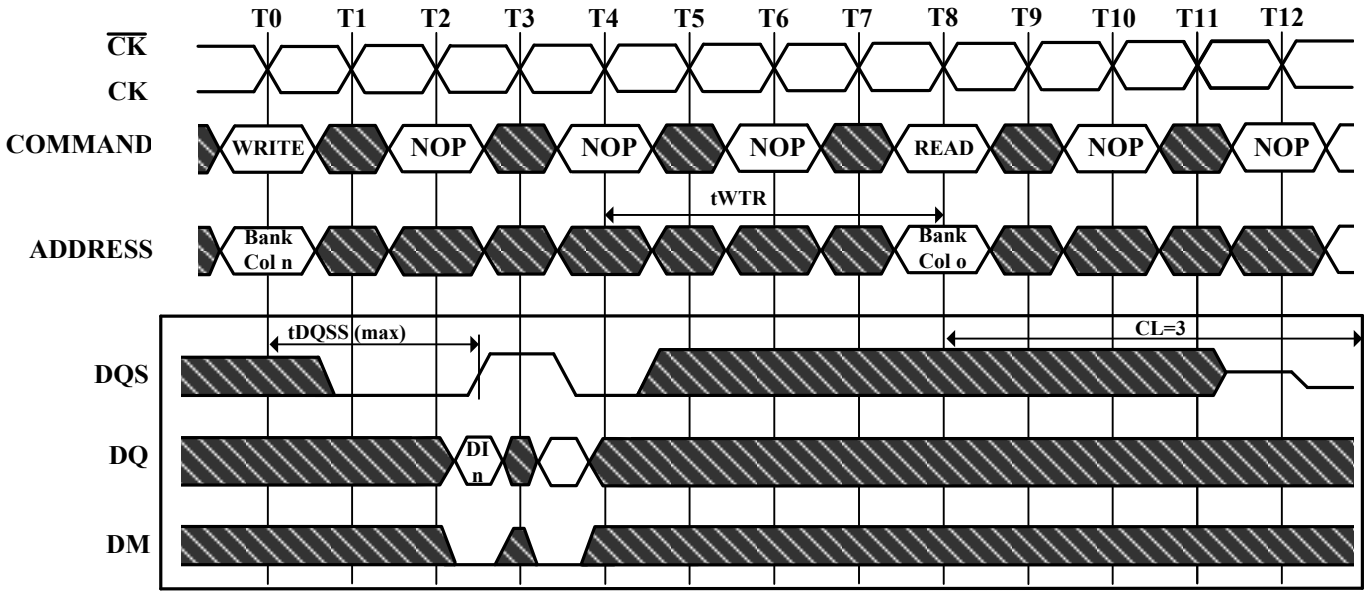
If burst of 4 or 8, the burst would be truncated

Each WRITE command may be to any bank and may be to the same or different devices

DM= DM0 ~ DM3

Don't Care

Figure 21. Write to Read Max tDQSS Non Interrupting



DI n, etc. = Data In for column n, etc.

1 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 2 is shown

tWTR is referenced from the first positive CK edge after the last Data In Pair

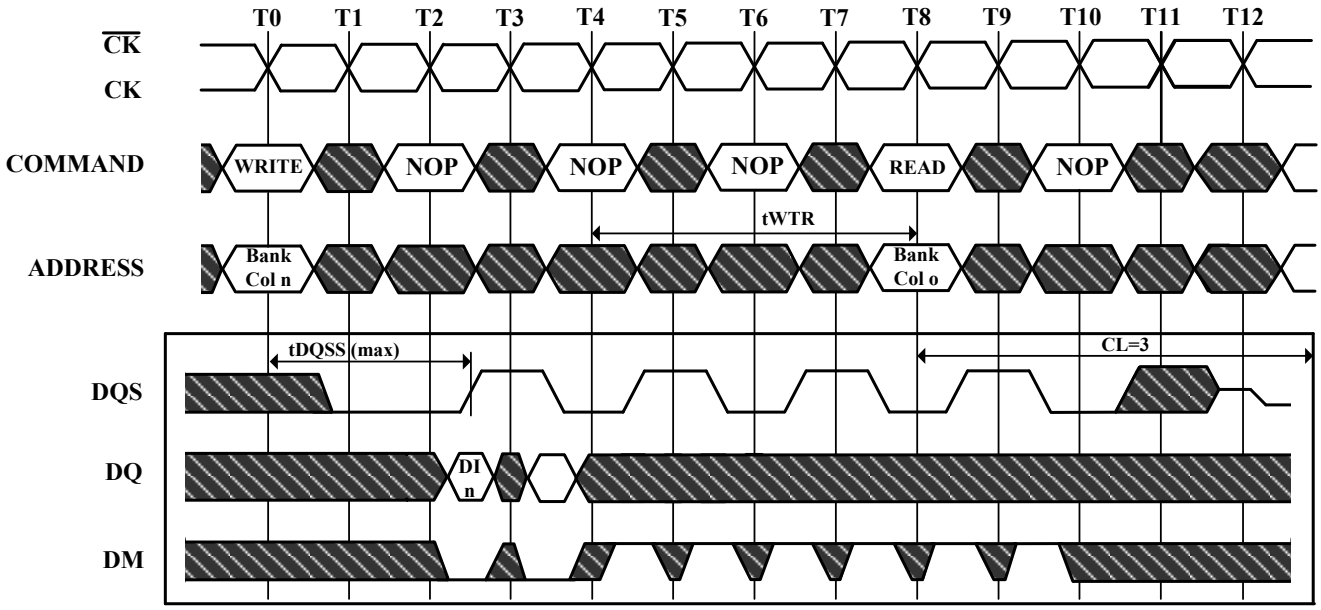
A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= DM0 ~ DM3

Don't Care

Figure 22. Write to Read Max tDQSS Interrupting



DI n, etc. = Data In for column n, etc.

1 subsequent elements of Data In are applied in the programmed order following DI n

An interrupted burst of 8 is shown, 2 data elements are written

tWTR is referenced from the first positive CK edge after the last Data In Pair

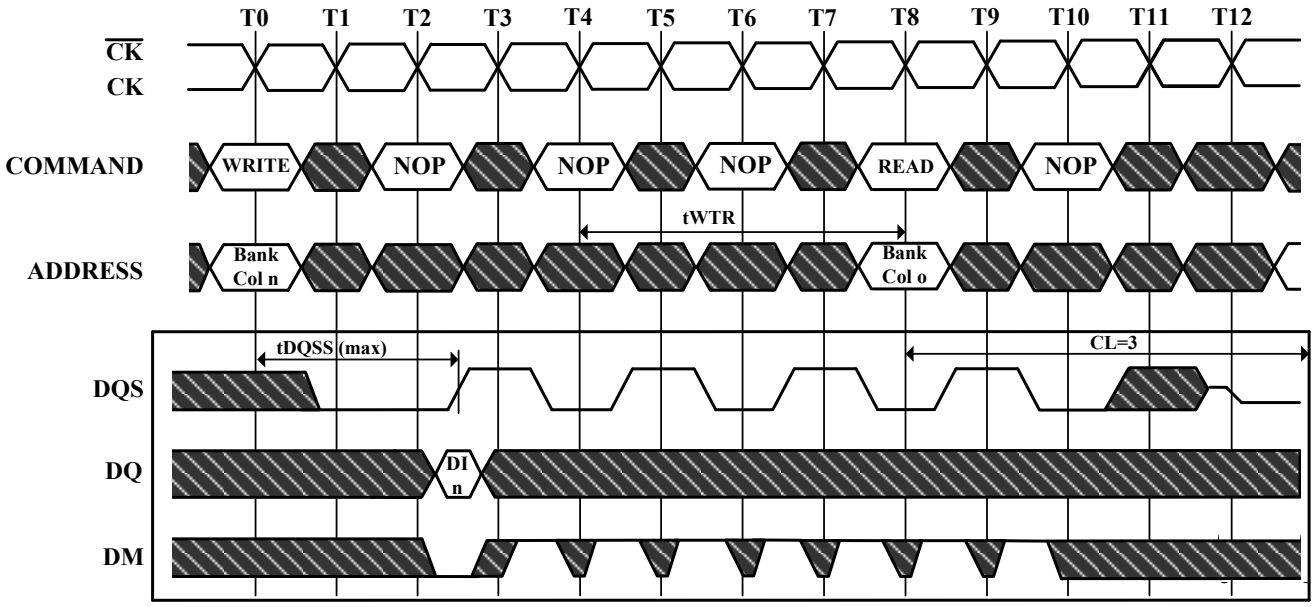
A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= DM0 ~ DM3

Don't Care

Figure 23. Write to Read Max tDQSS, ODD Number of Data, Interrupting



DI n = Data In for column n

An interrupted burst of 8 is shown, 1 data elements are written

tWTR is referenced from the first positive CK edge after the last Data In Pair (not the last desired Data In element)

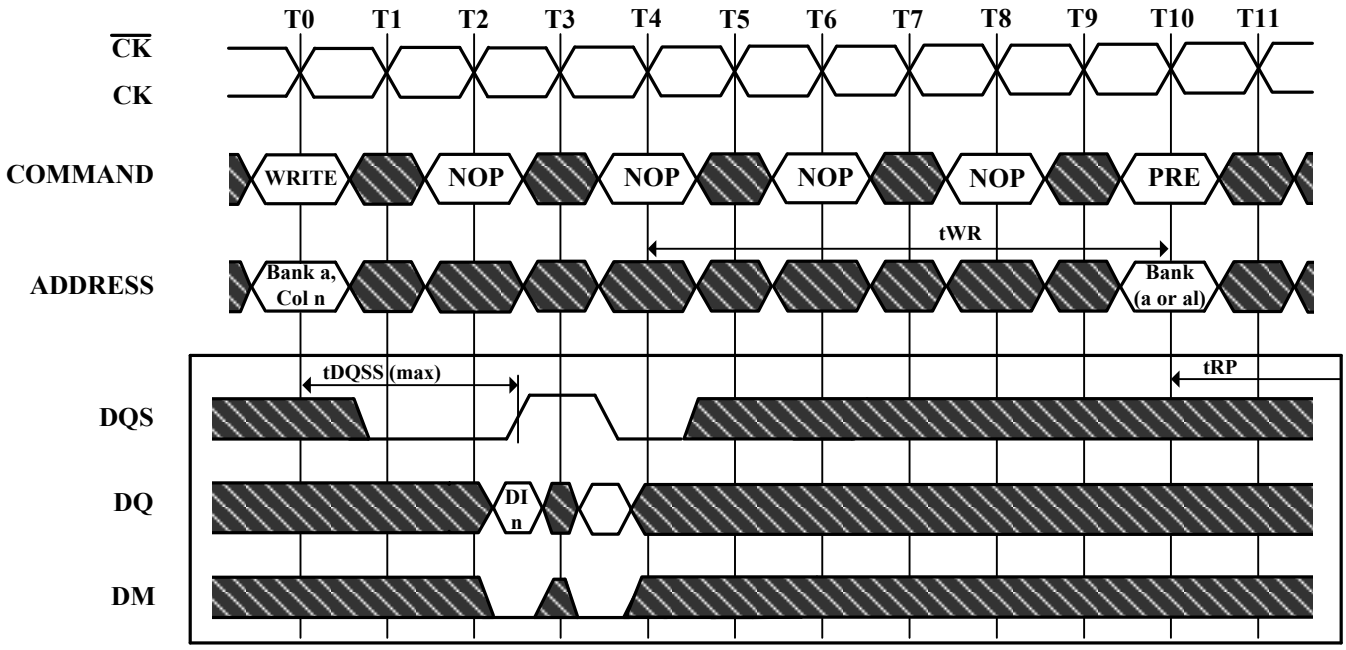
A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= DM0 ~ DM3

Don't Care

Figure 24. Write to Precharge Max tDQSS, NON- Interrupting



DI n = Data In for column n

1 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 2 is shown

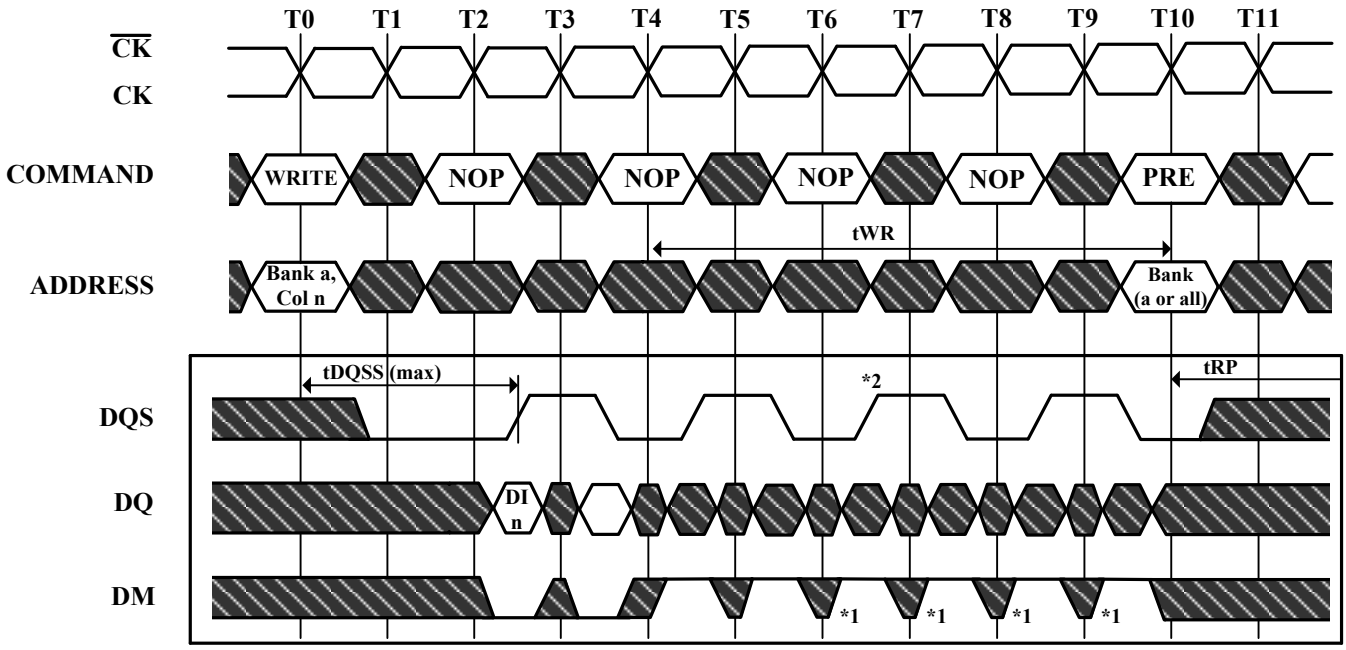
tWR is referenced from the first positive CK edge after the last Data In Pair

A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

DM= DM0 ~ DM3

Don't Care

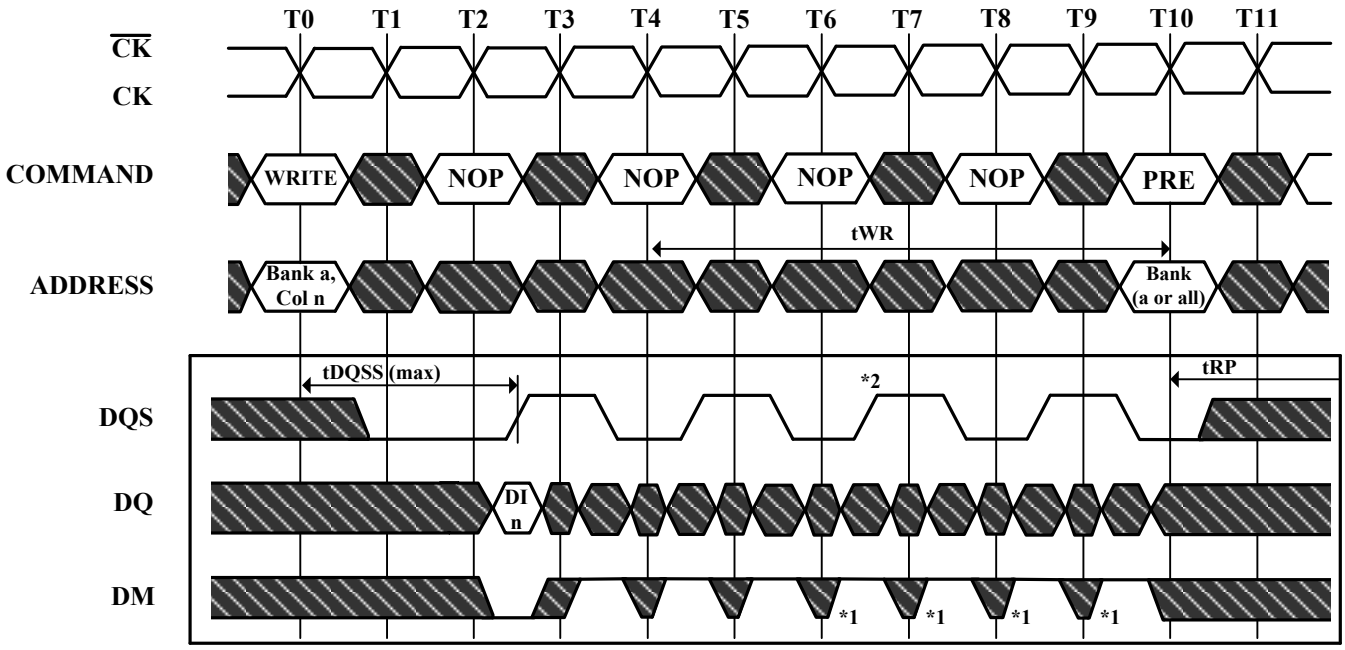
Figure 25. Write to Precharge Max tDQSS, Interrupting



DI n = Data In for column n
An interrupted burst of 4 or 8 is shown, 2 data elements are written
tWR is referenced from the first positive CK edge after the last Data In Pair
A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
***1 = can be don't care for programmed burst length of 4**
***2 = for programmed burst length of 4, DQS becomes don't care at this point**
DM= DM0 ~ DM3

Don't Care

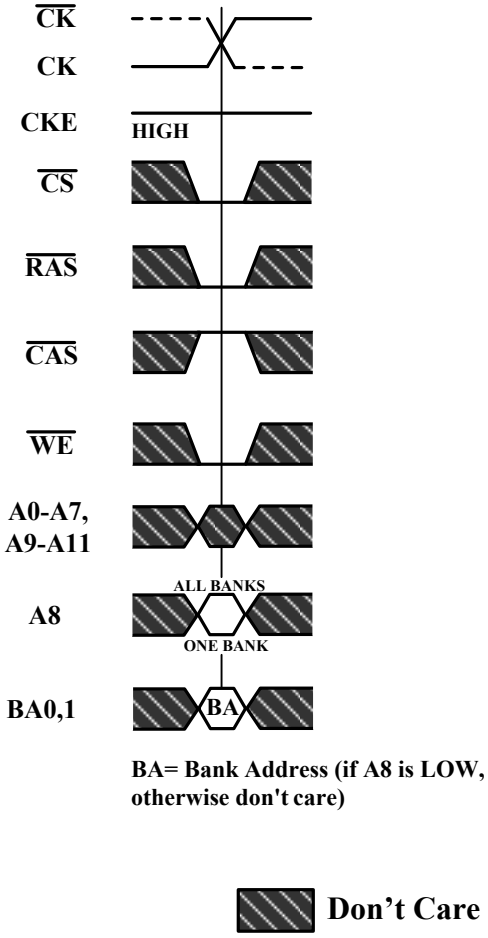
Figure 26. Write to Precharge Max tDQSS ODD Number of Data Interrupting



DI n = Data In for column n
An interrupted burst of 4 or 8 is shown, 1 data element is written
tWR is referenced from the first positive CK edge after the last Data In Pair
A8 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
***1 = can be don't care for programmed burst length of 4**
***2 = for programmed burst length of 4, DQS becomes don't care at this point**
DM= DM0 ~ DM3

Don't Care

Figure 27. Precharge Command



BA= Bank Address (if A8 is LOW, otherwise don't care)

Don't Care

Figure 28. Power-Down

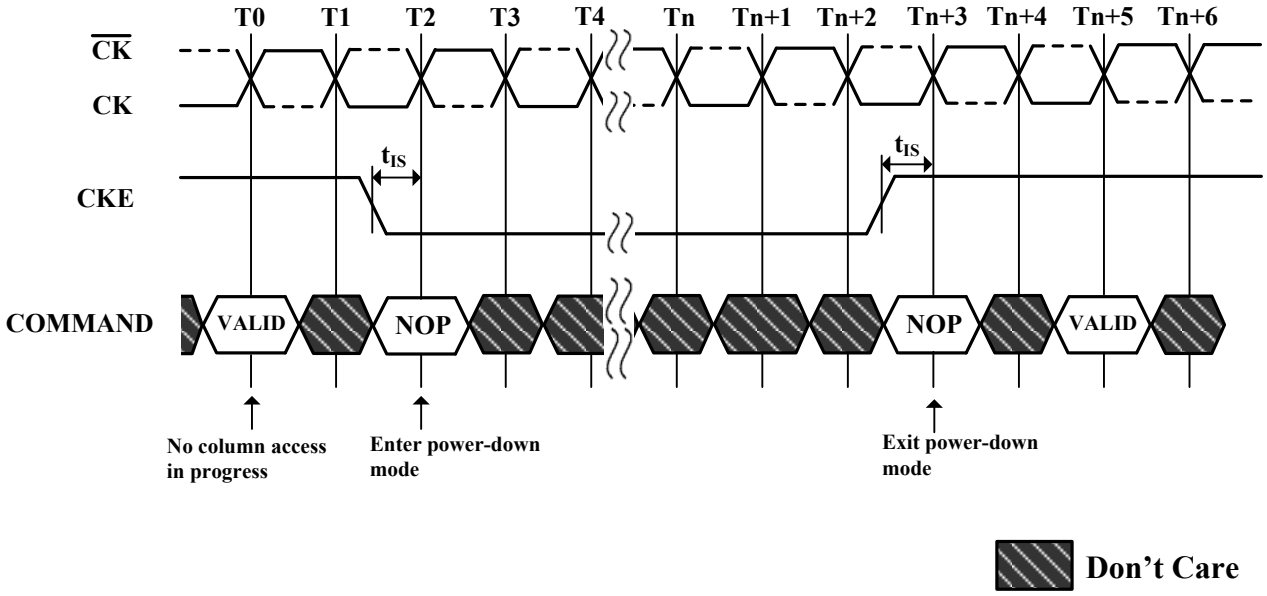


Figure 29. Clock Frequency Change in Precharge

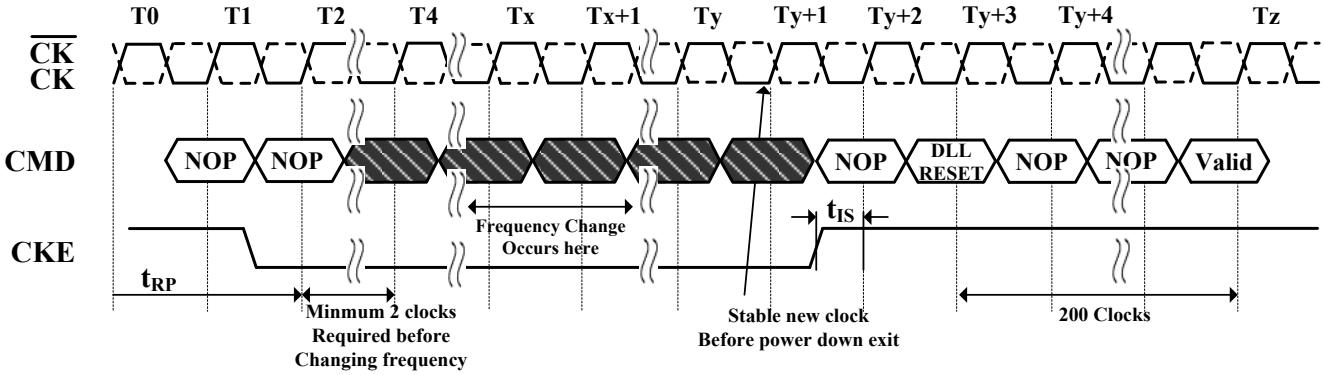
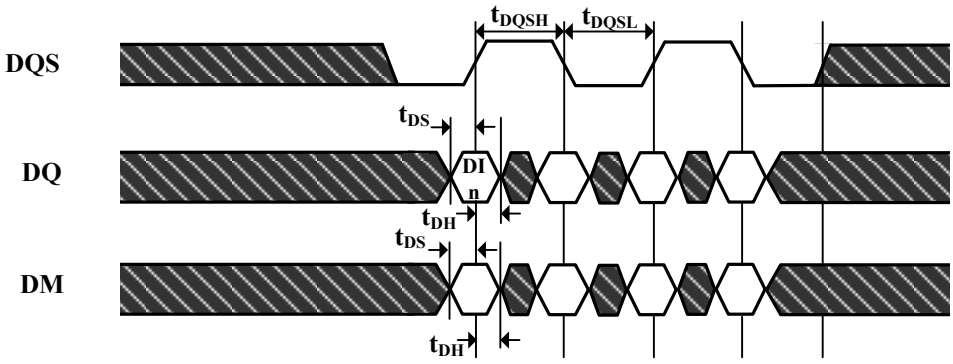


Figure 30. Data input (Write) Timing



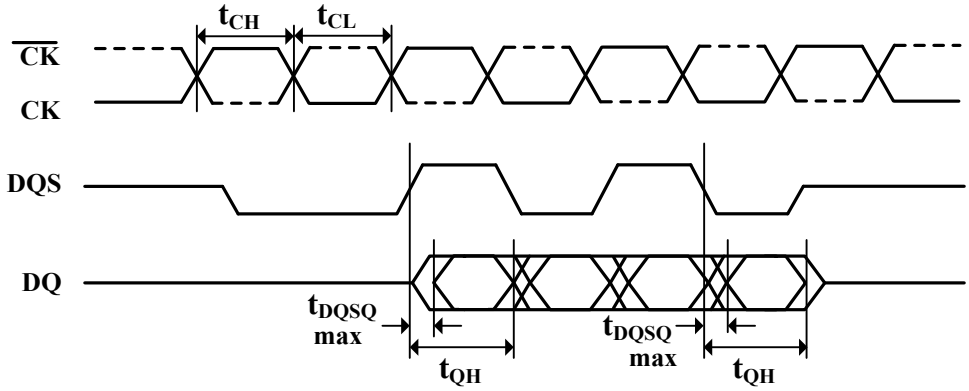
DI n = Data In for column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI n

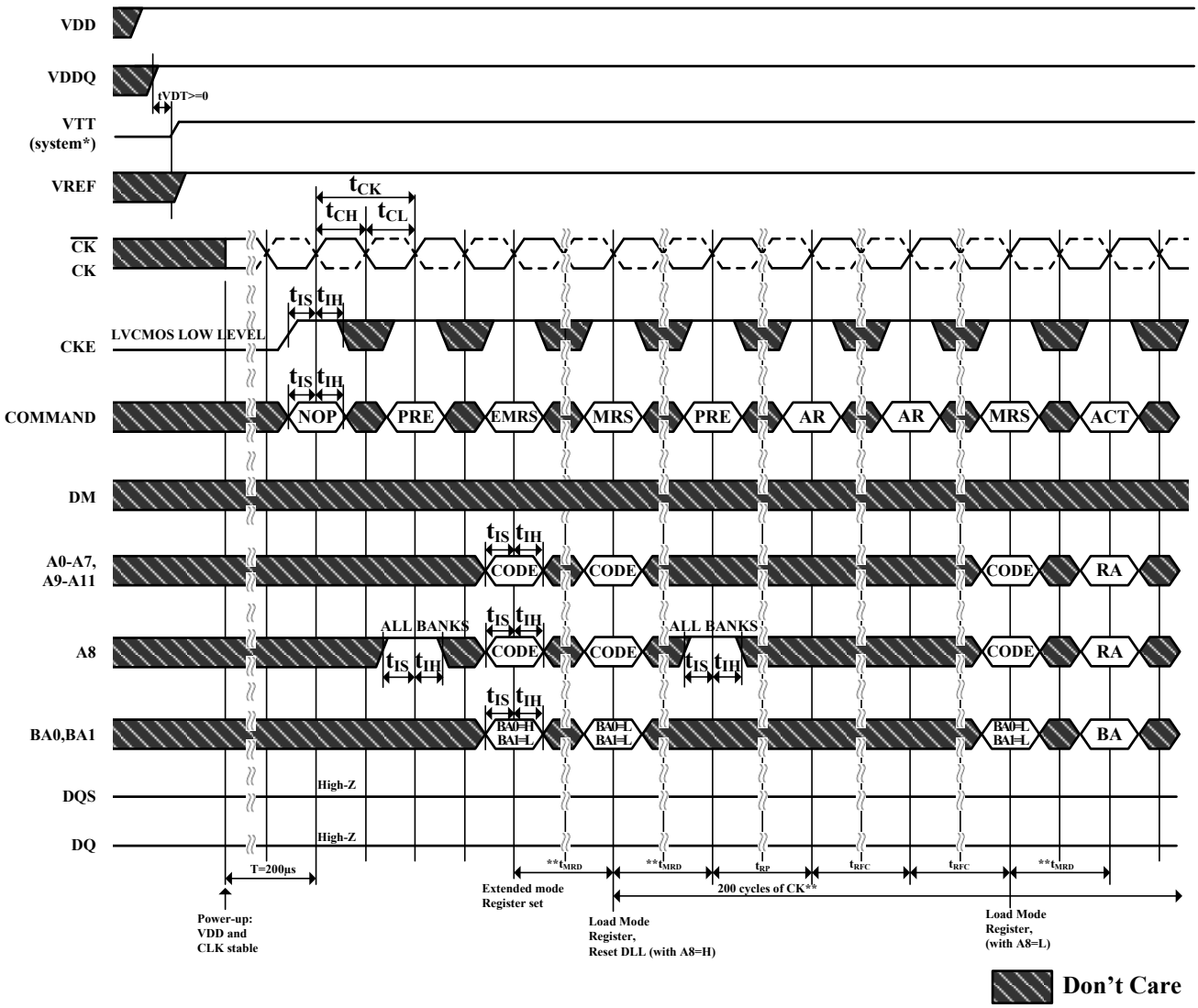
Don't Care

Figure 31. Data Output (Read) Timing



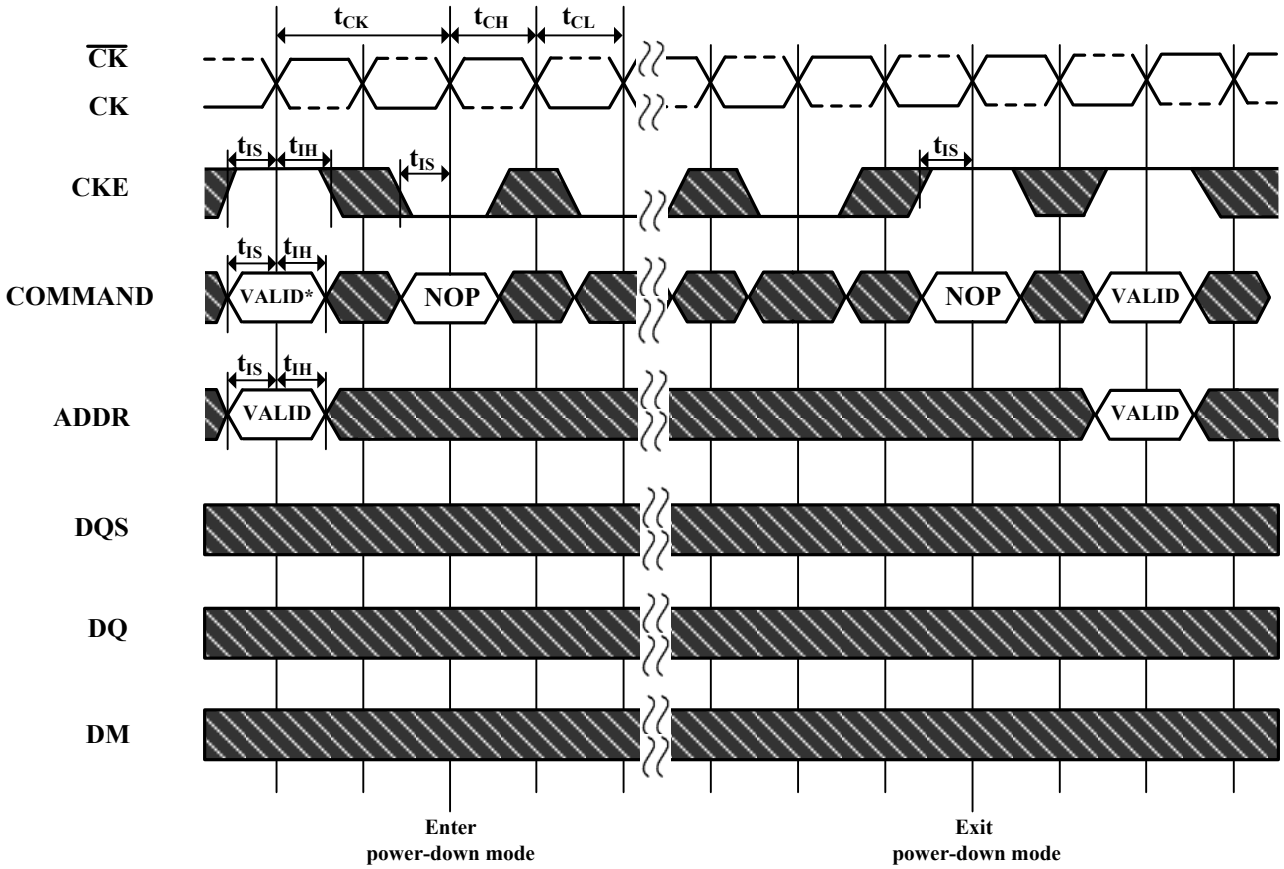
Burst Length = 4 in the case shown

Figure 32. Initialize and Mode Register Sets



*=VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch-up.
** = tMRD is required before any command can be applied, and 200 cycles of CK are required before any executable command can be applied the two auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.

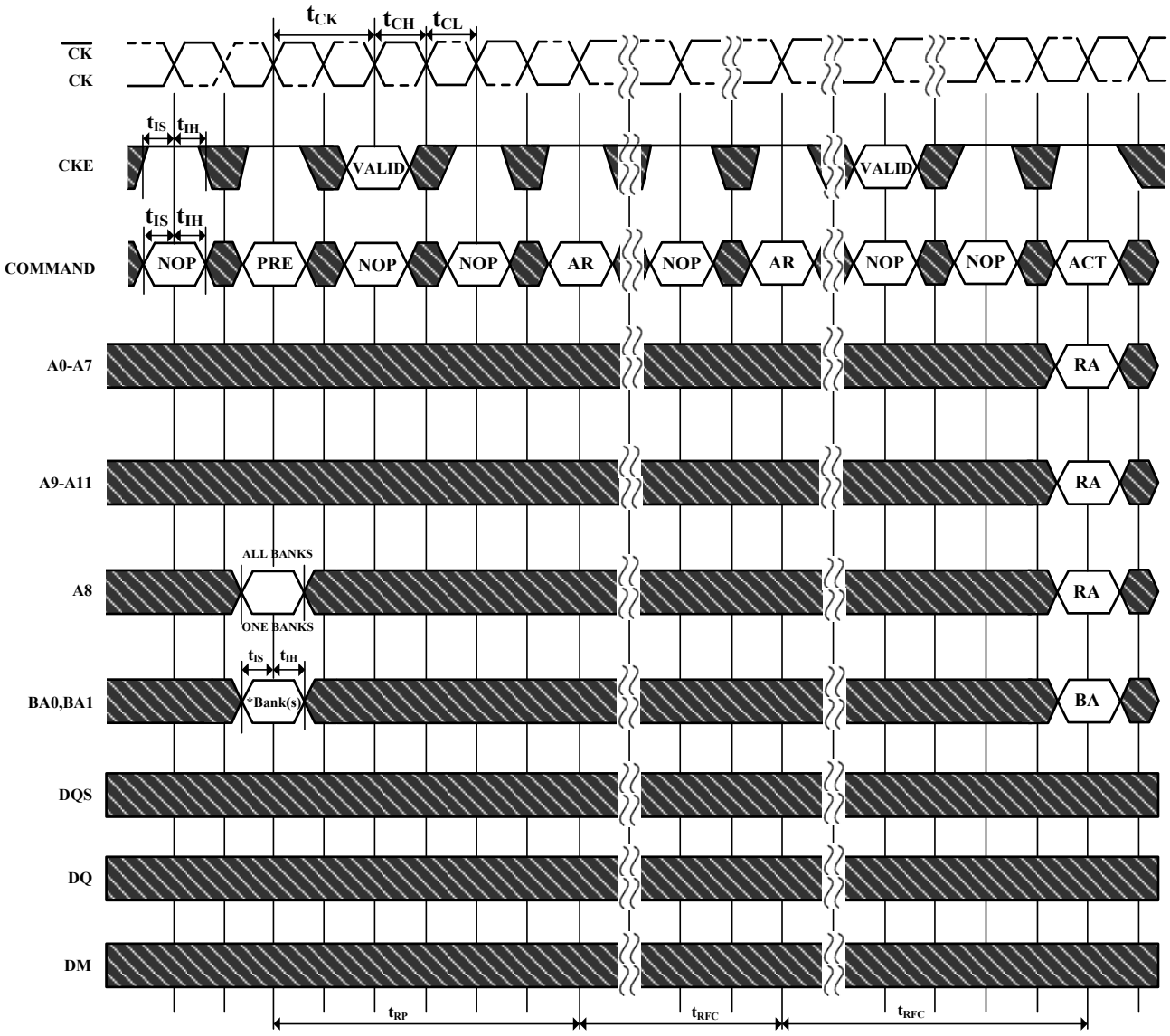
Figure 33. Power Down Mode



No column accesses are allowed to be in progress at the time Power-Down is entered
***=If this command is a PRECHARGE ALL (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is active Power Down.**

Don't Care

Figure 34. Auto Refresh Mode



*** = " Don't Care", if A8 is HIGH at this point; A8 must be HIGH if more than one bank is active (i.e., must precharge all active banks)**

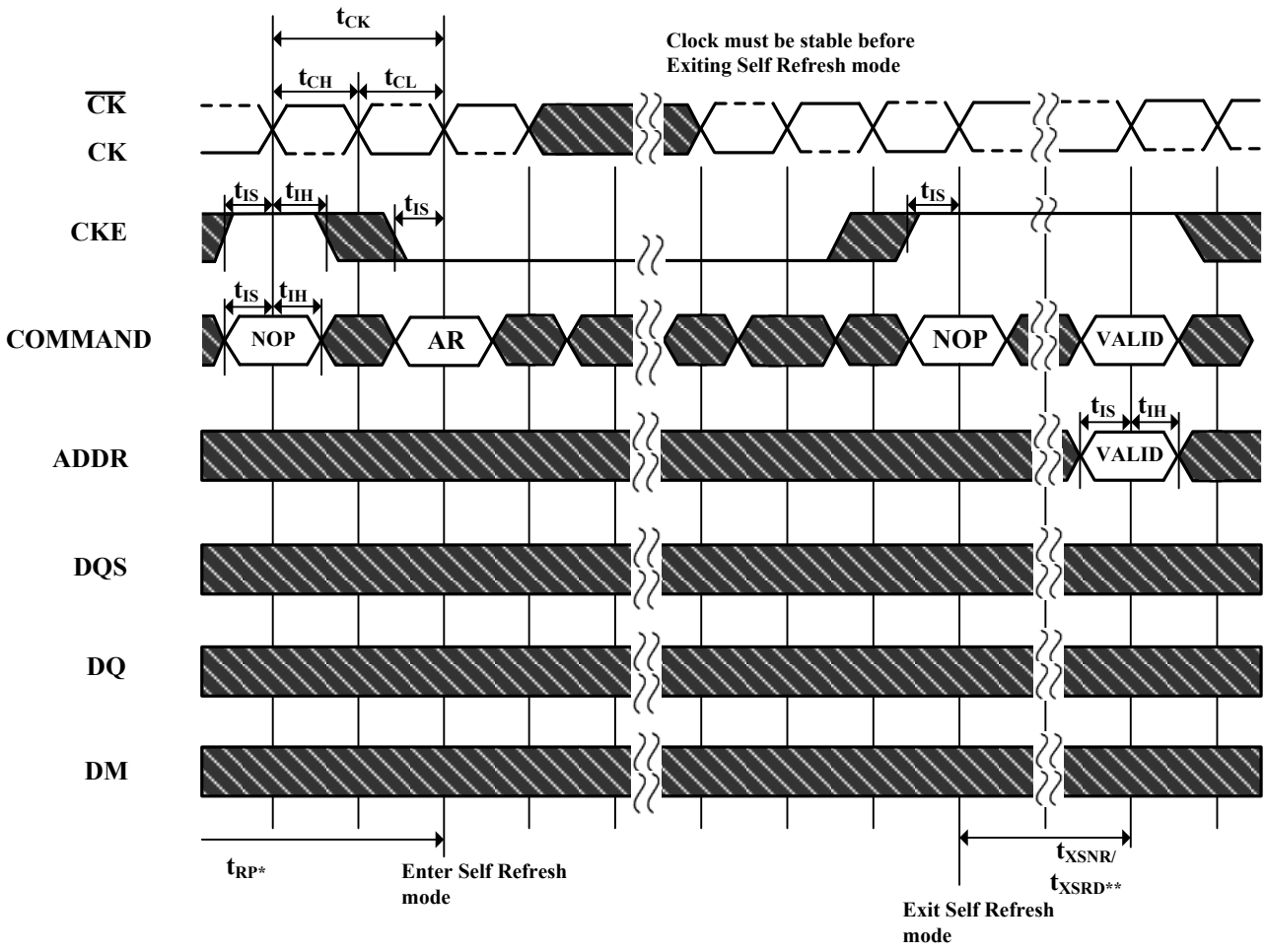
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH

NOP commands are shown for ease of illustration; other valid commands may be possible after tRFC

DM, DQ and DQS signals are all " Don't Care" /High-Z for operations shown

Don't Care

Figure 35. Self Refresh Mode

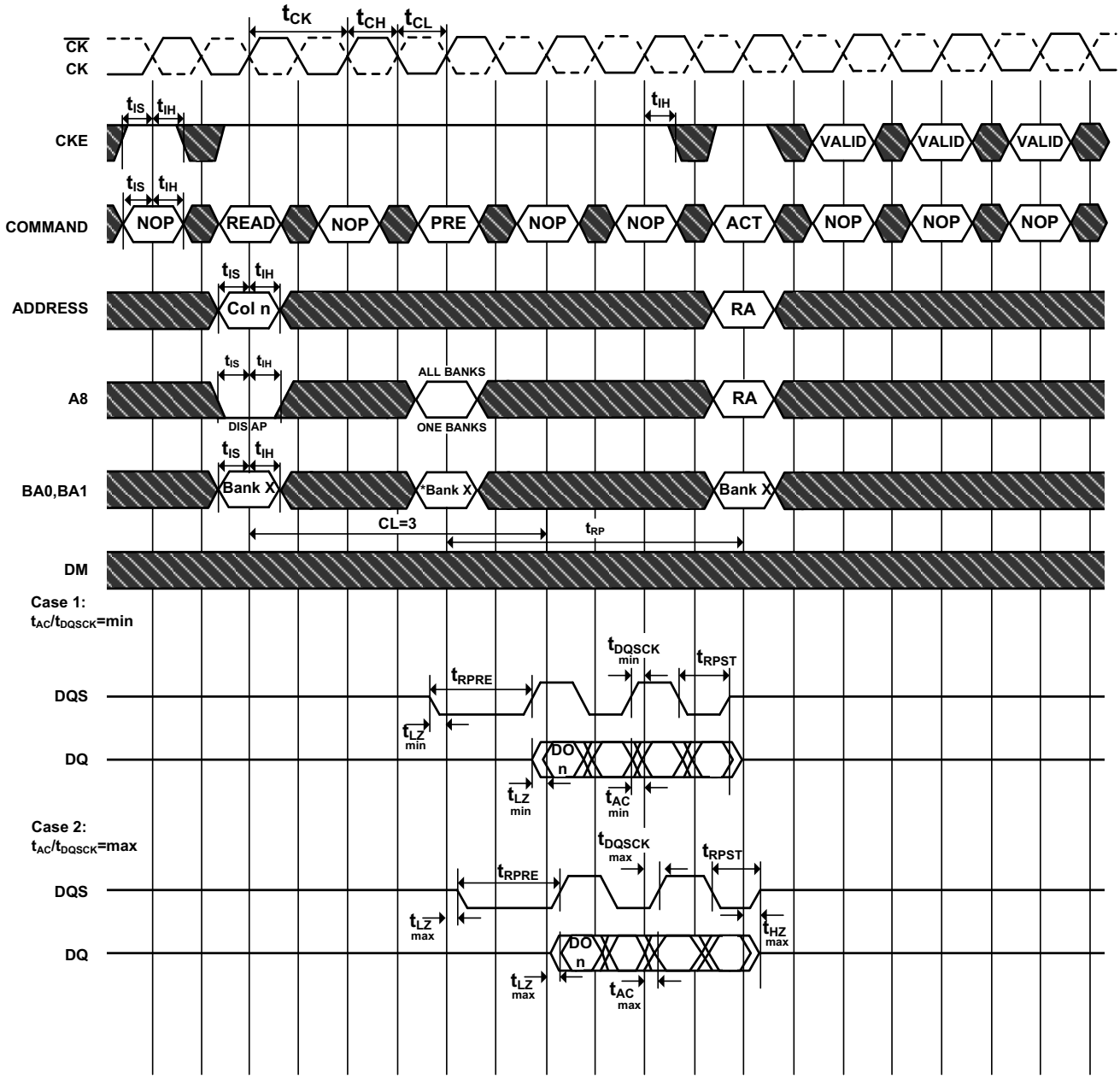


* = Device must be in the " All banks idle" state prior to entering Self Refresh mode

** = tXSNR is required before any non-READ command can be applied, and tXSRD (200 cycles of CK) is required before a READ command can be applied.

Don't Care

Figure 36. Read without Auto Precharge



DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge

* =" Don't Care" , if A8 is HIGH at this point

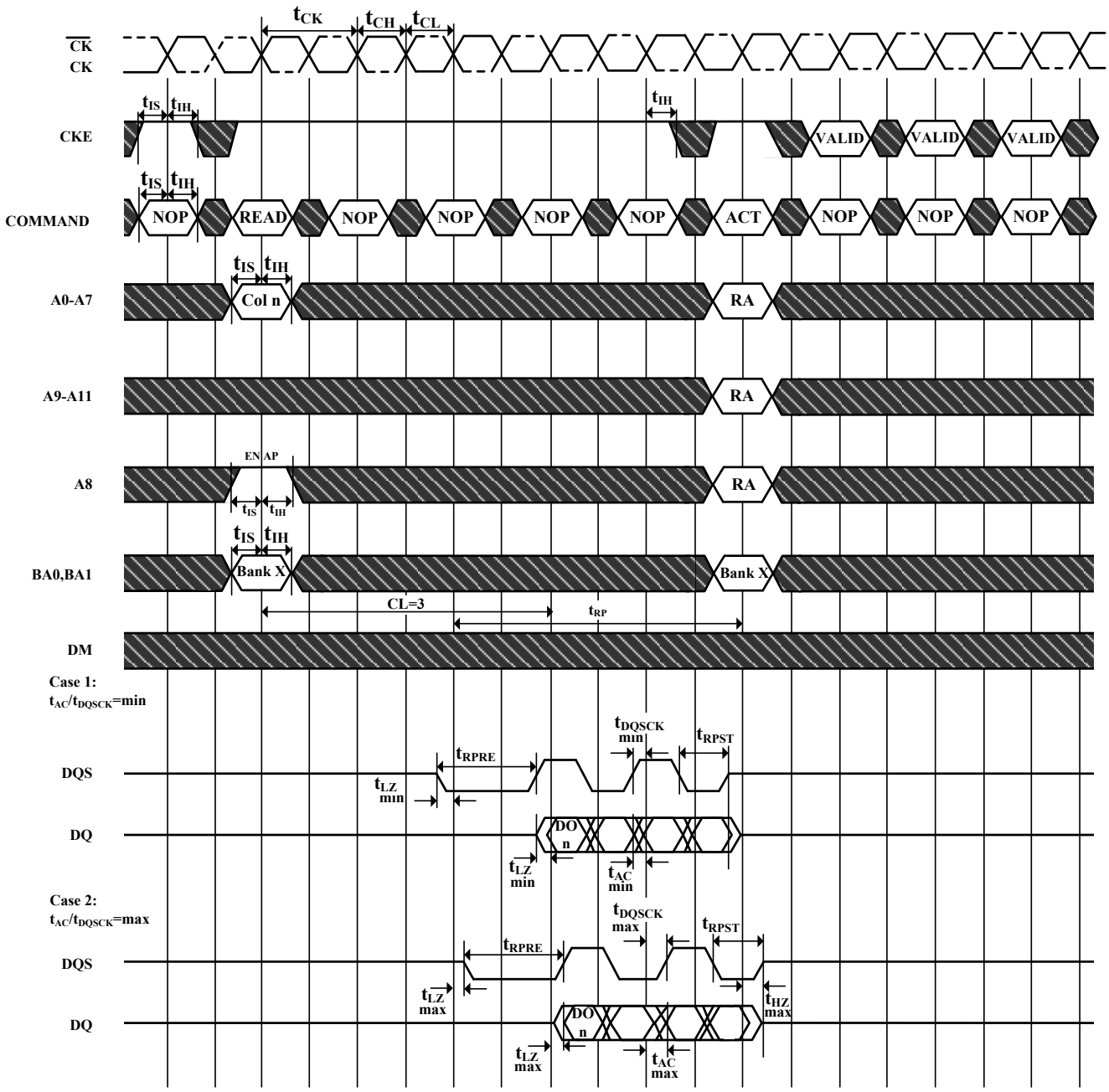
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH

NOP commands are shown for ease of illustration; other commands may be valid at these times

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

Don't Care

Figure 37. Read with Auto Precharge



DO n = Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

EN AP = Enable Autoprecharge

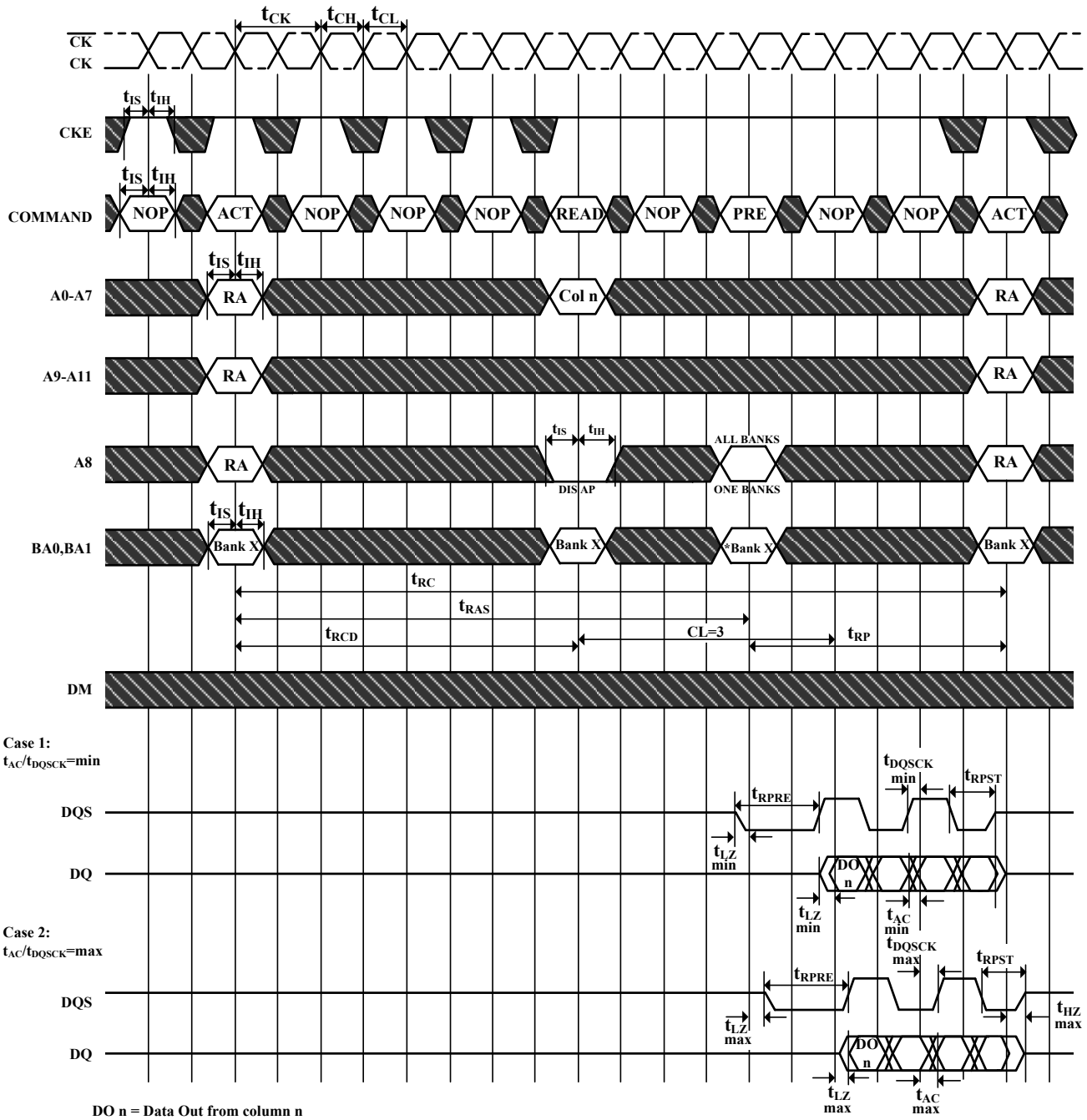
ACT = ACTIVE, RA = Row Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

The READ command may not be issued until tRAP has been satisfied. If Fast Autoprecharge is supported, tRAP = tRCD, else the READ may not be issued prior to tRASmin – (BL*tCK/2)

Don't Care

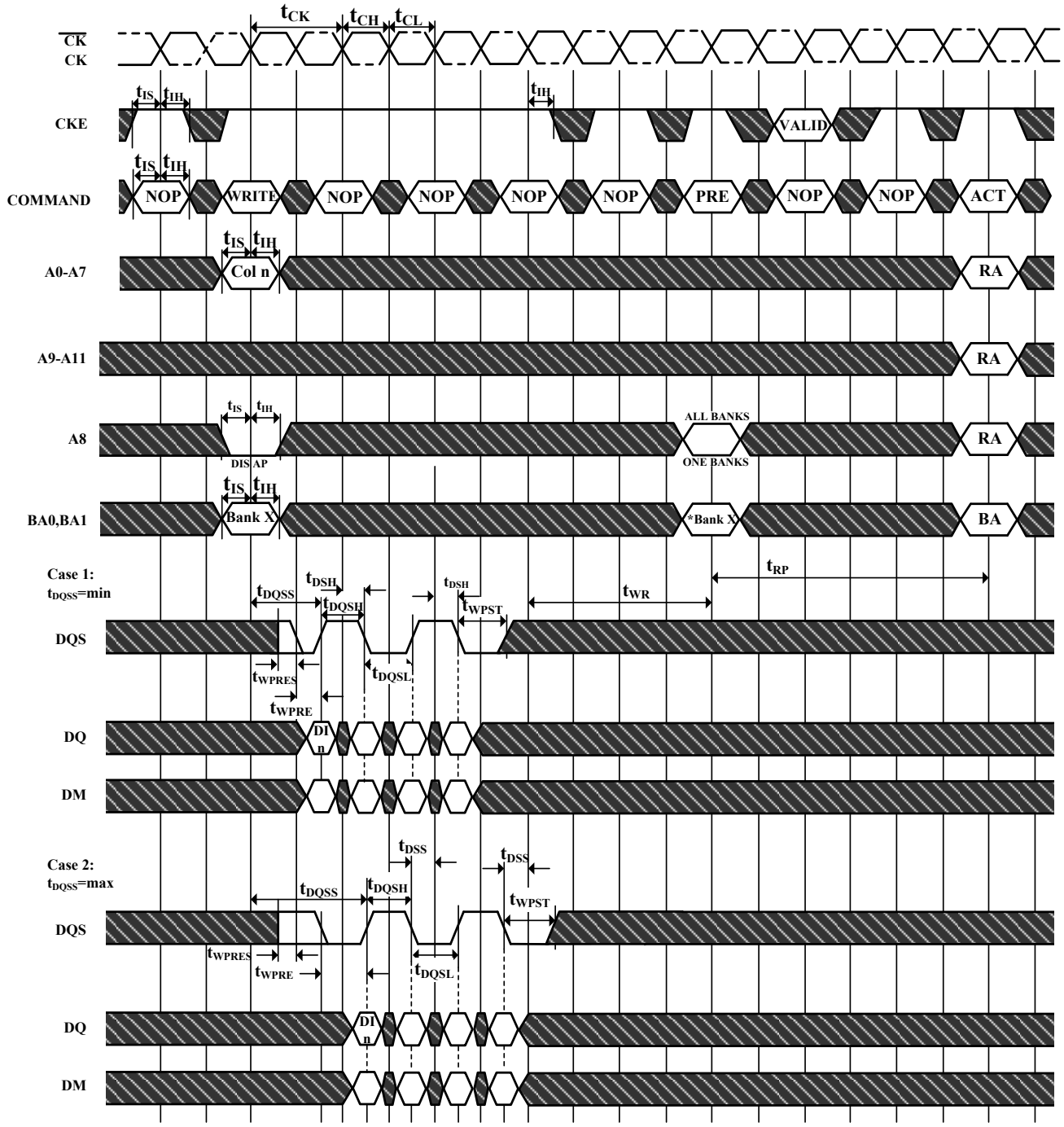
Figure 38. Bank Read Access



DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = ” Don't Care”, if A8 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Note that tRCD > tRCD MIN so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)

Don’t Care

Figure 39. Write without Auto Precharge



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

*=" Don't Care" , if A8 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH

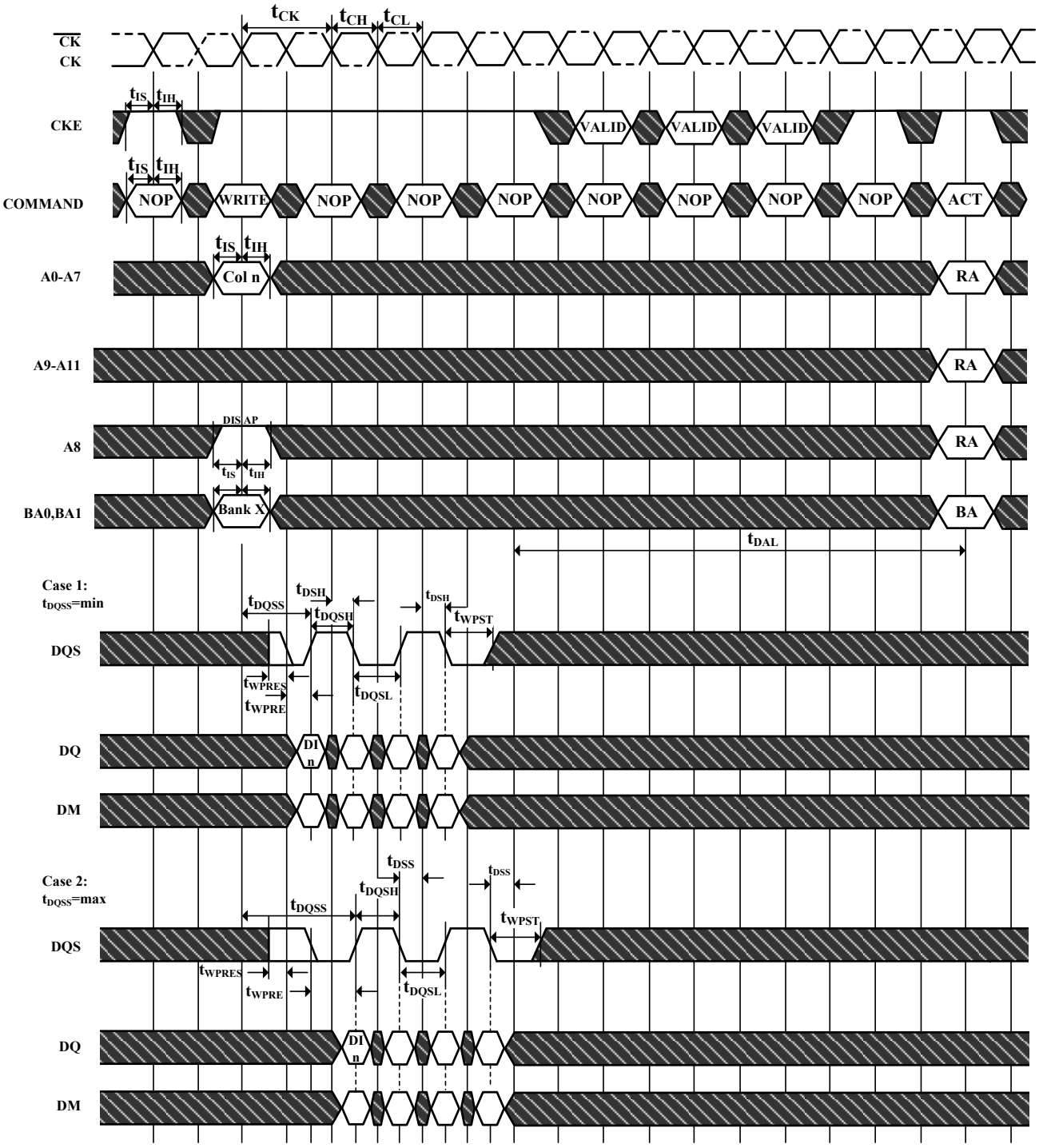
NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

Don't Care

Figure 40. Write with Auto Precharge



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DI n

EN AP = Enable Autoprecharge

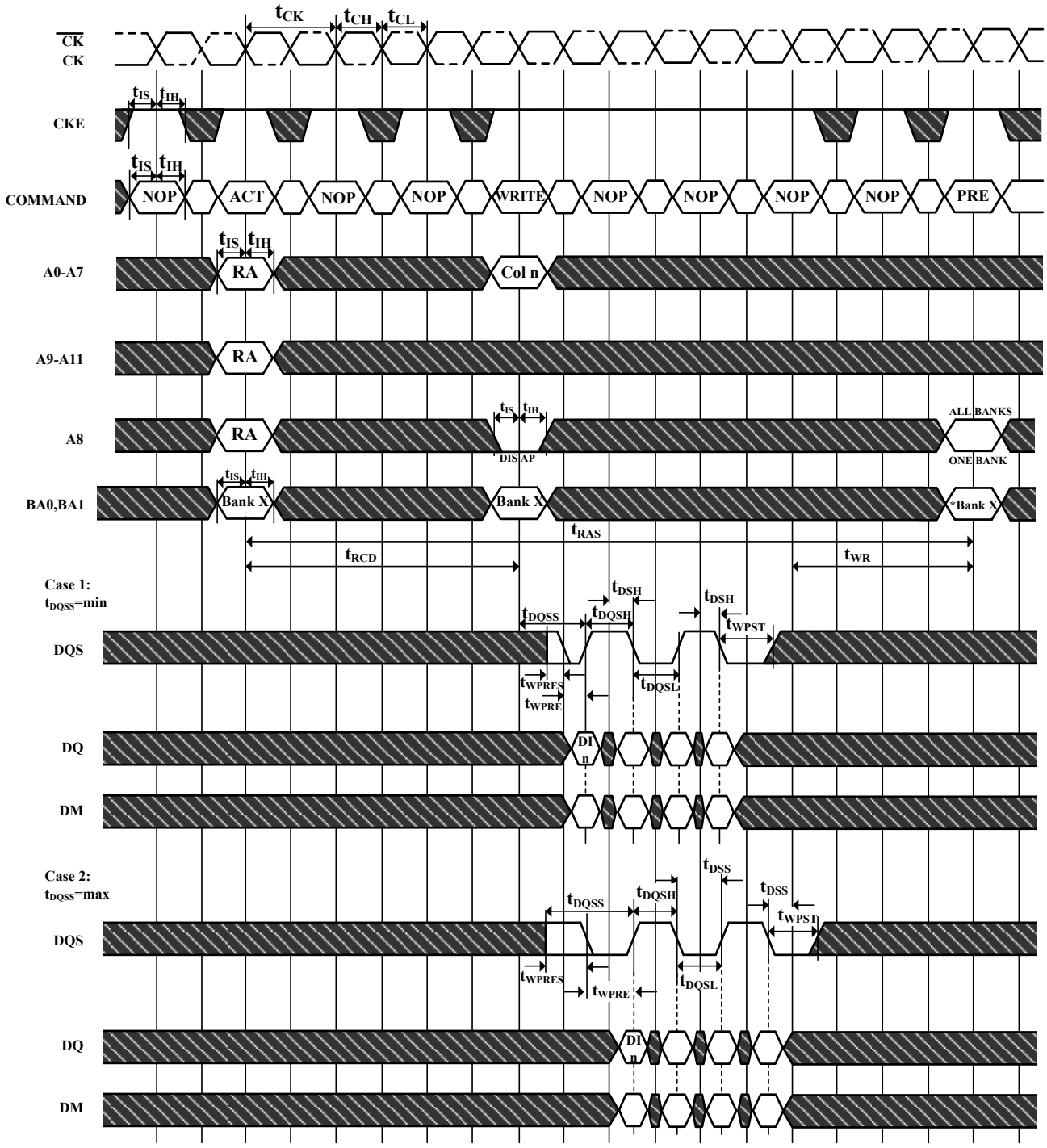
ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge

Don't Care

Figure 41. Bank Write Access



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

*=" Don't Care" , if A8 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

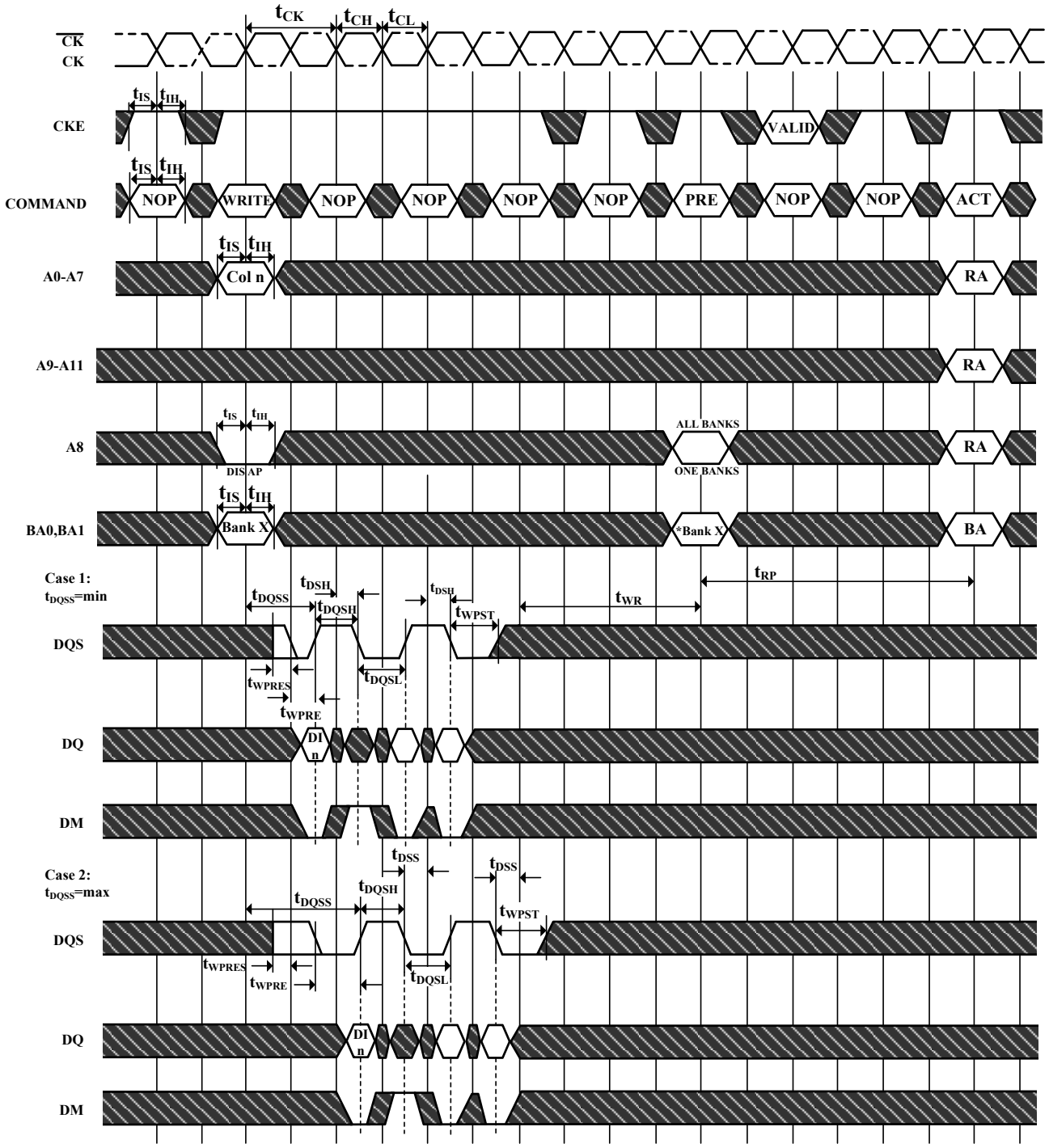
NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

Don't Care

Figure 42. Write DM Operation



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

*=" Don't Care" , if A8 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

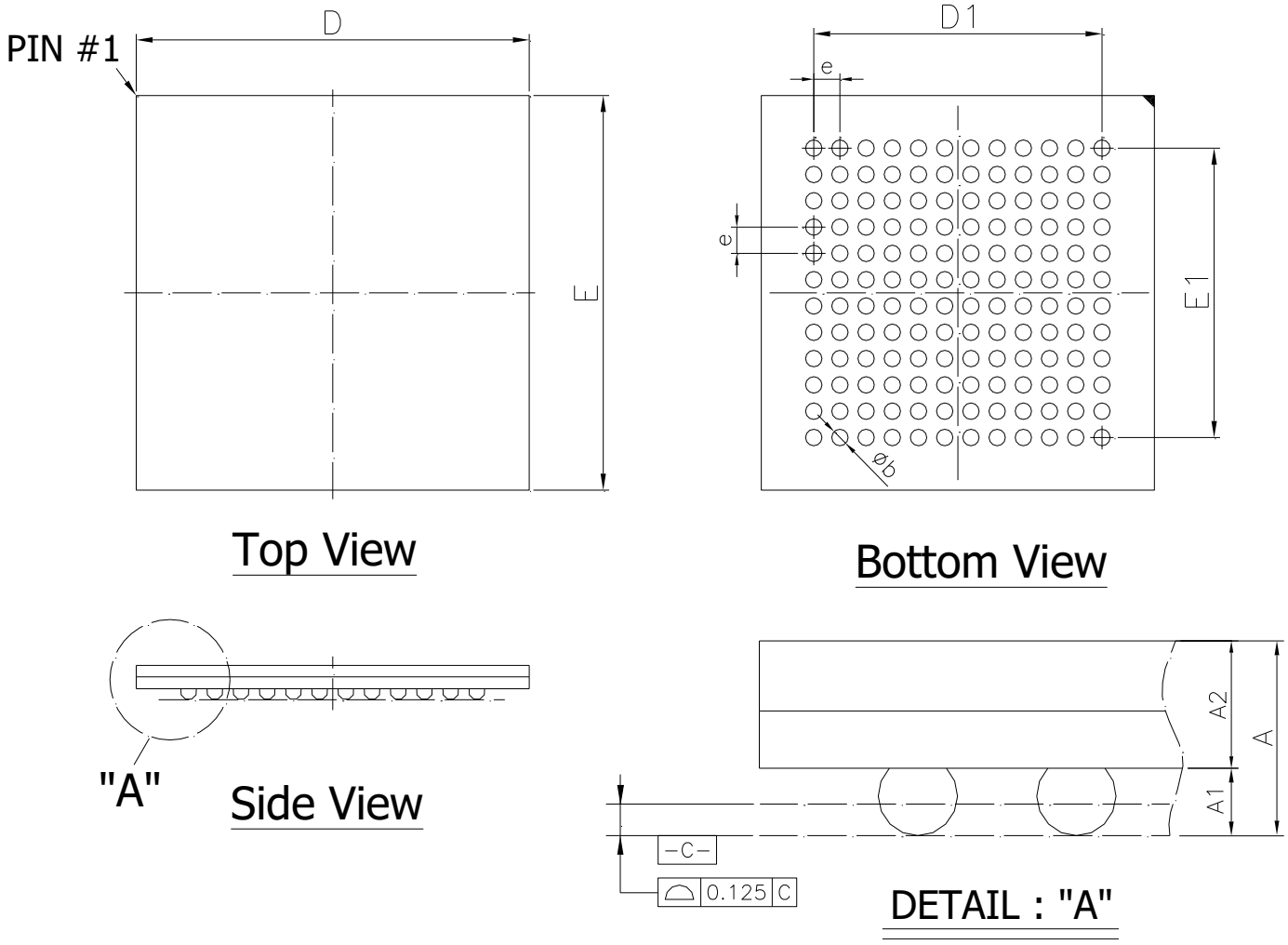
NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

Don't Care

Figure 43. 144 ball LFBGA Package Outline Drawing Information
Units: mm



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.055	--	--	1.40
A1	0.012	0.014	0.016	0.30	0.35	0.40
A2	0.036	0.038	0.040	0.91	0.96	1.01
D	0.469	0.472	0.476	11.90	12.00	12.10
E	0.469	0.472	0.476	11.90	12.00	12.10
D1	--	0.346	--	--	8.80	--
E1	--	0.346	--	--	8.80	--
e	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50

PART NUMBERING SYSTEM

AS4C	4M32D1A	5	B	C/I	N
DRAM	4M32=4Mx32 D1=DDR1 A= A die version	5=200MHz	B = FBGA	C= Commercial (0° C~70° C) I= Industrial (-40° C~85° C)	Indicates Pb and Halogen Free

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