60V N-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI3333-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$ max	I_D max T_A = +25°C
60V	13mΩ @ V_{GS} = 10V	10.3A
	18mΩ @ V_{GS} = 4.5V	8.8A

Features and Benefits

- Low $R_{DS(ON)}$ – Ensures on state losses are minimized
- Small form factor thermally efficient package enables higher density end products
- Occupies just 33% of the board area occupied by SO-8 enabling smaller end product
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DMN6013LFGQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

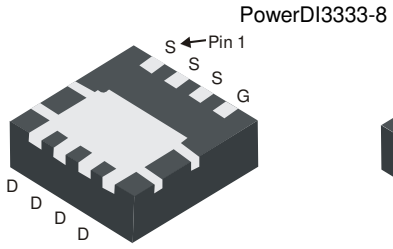
Description and Applications

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP, and is ideal for use in:

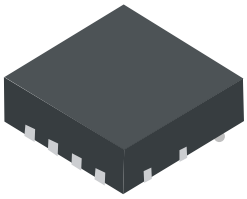
- Motor control
- DC to DC converters
- Reverse polarity protection

Mechanical Data

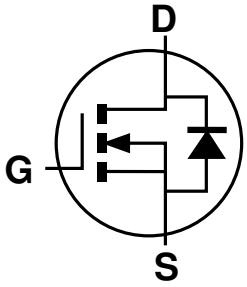
- Package: PowerDI®3333-8
- Package Material: Molded Plastic, "Green" Molding Compound, UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish—Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.072 grams (Approximate)



Bottom View



Top View



Equivalent Circuit

Ordering Information (Note 4)

Orderable Part Number	Package	Packing	
		Quantity	Carrier
DMN6013LFGQ-7	PowerDI3333-8	2,000	Tape & Reel
DMN6013LFGQ-13	PowerDI3333-8	3,000	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

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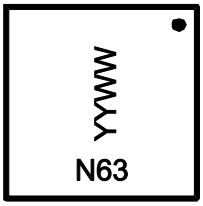
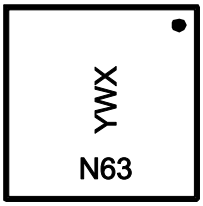
Marking Information

Site1



N63 = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 23 = 2023)
WW = Week Code (01 to 53)

Site2:



N63 = Product Type Marking Code
YWX = Date Code Marking
Y = Year (ex: 3 = 2023)
W = Week (ex: a = Week 27, z Represents Week 52 and 53)
X = Internal Code (ex: U = Monday)

Date Code Key

Year	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034
Code	3	4	5	6	7	8	9	0	1	2	3	4

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = 10V	T_A = +25°C T_A = +70°C	I_D	10.3 8.3	A
	T_C = +25°C T_C = +100°C	I_D	45 28	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	58.3	A
Maximum Continuous Body Diode Forward Current (Note 6)		I_S	3	A
Avalanche Current, L = 0.1mH		I_{AS}	33.3	A
Avalanche Energy, L = 0.1mH		E_{AS}	56.8	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	123	°C/W
	t < 10s		69	
Total Power Dissipation (Note 6)		P_D	2.1	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	60	°C/W
	t < 10s		34	
Total Power Dissipation (Note 6)		P_D	40	W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	3.2	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

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Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current, T_J = +25°C	I_{DSS}	—	—	1	µA	V_{DS} = 60V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	1.8	3	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	9.3	13	mΩ	V_{GS} = 10V, I_D = 10A
		—	12.3	18		V_{GS} = 4.5V, I_D = 8A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 1.7A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	2577	—	pF	V_{DS} = 30V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	162	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	132	—	pF	
Gate Resistance	R_g	—	0.9	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	26.6	—	nC	V_{DS} = 30V, I_D = 10A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	55.4	—	nC	
Gate-Source Charge	Q_{gs}	—	9.3	—	nC	
Gate-Drain Charge	Q_{gd}	—	12.6	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	6.2	—	ns	V_{GS} = 10V, V_{DS} = 30V, R_G = 3Ω, I_D = 10A
Turn-On Rise Time	t_R	—	9.9	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	27.6	—	ns	
Turn-Off Fall Time	t_F	—	11.7	—	ns	
Body Diode Reverse Recovery Time	t_{RR}	—	9.4	—	ns	I_F = 10A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	18.6	—	nC	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

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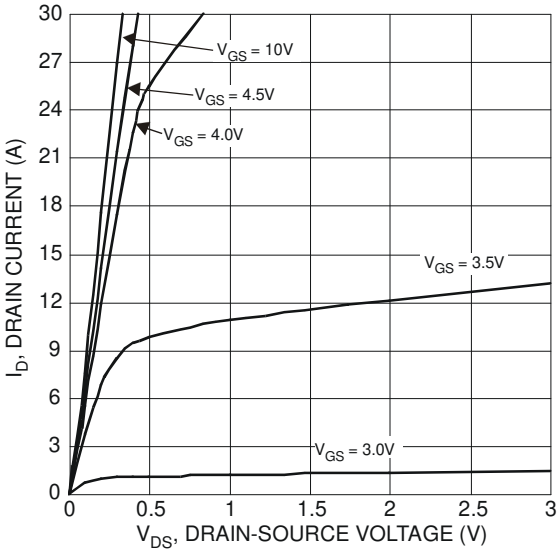

Figure 1 Typical Output Characteristics

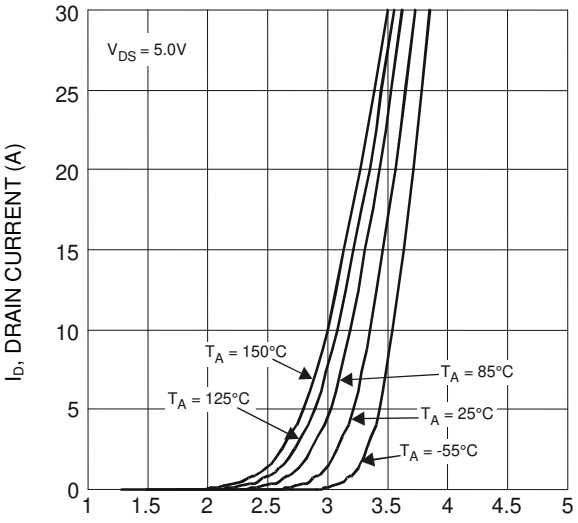

Figure 2 Typical Transfer Characteristics

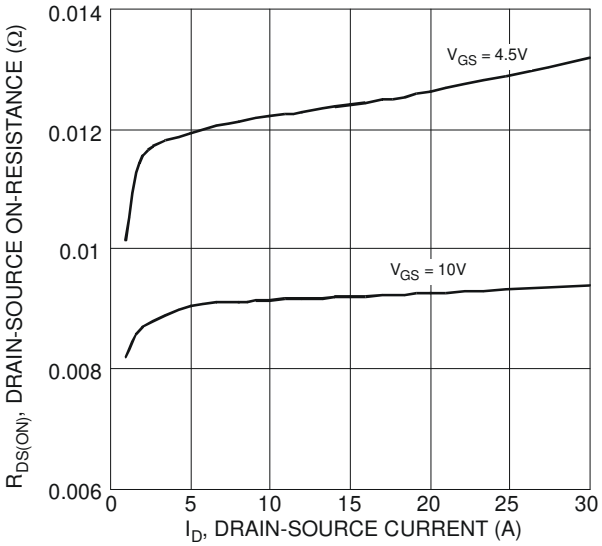

Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

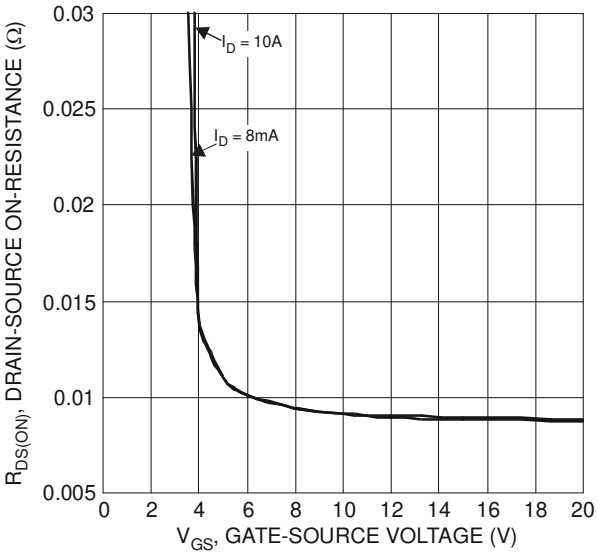

Figure 4 Typical Drain-Source On-Resistance vs. Gate-Source Voltage

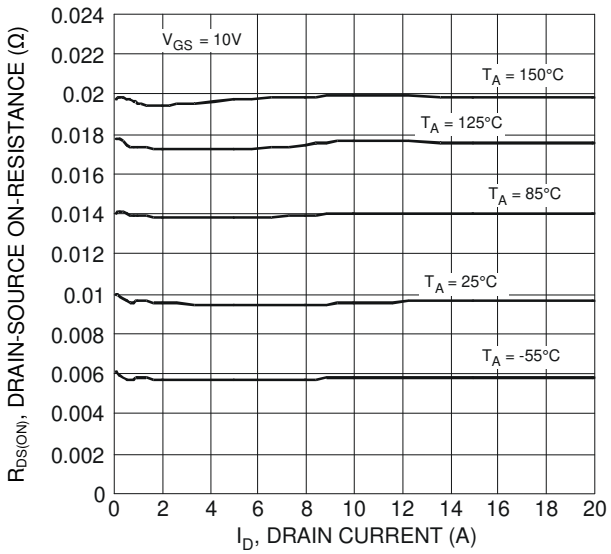

Figure 5 Typical On-Resistance vs. Drain Current and Temperature

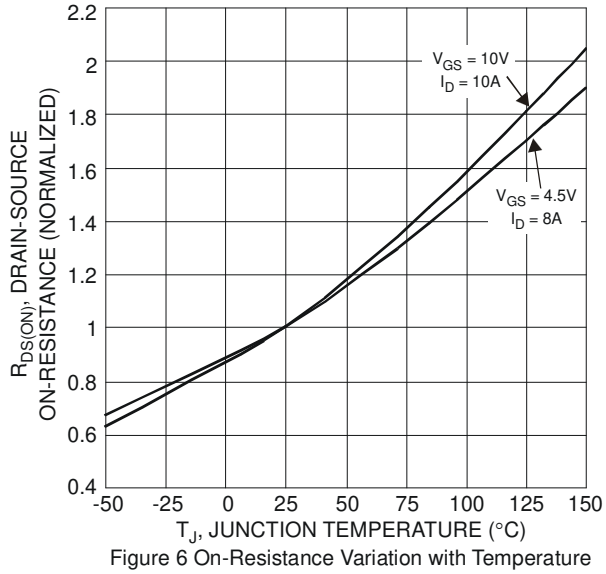

Figure 6 On-Resistance Variation with Temperature

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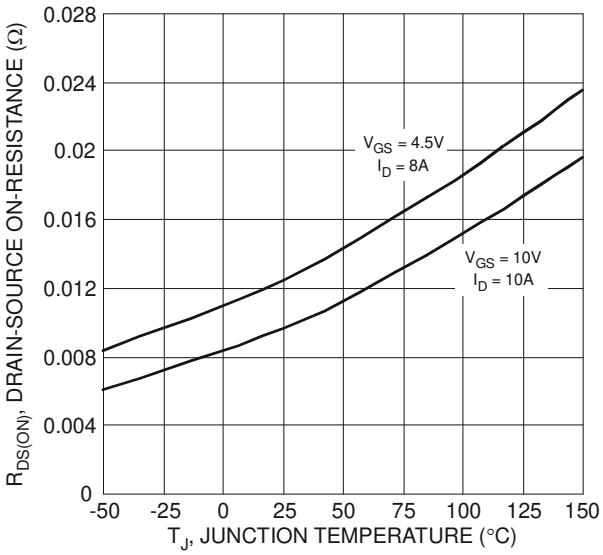

Figure 7 On-Resistance Variation with Temperature

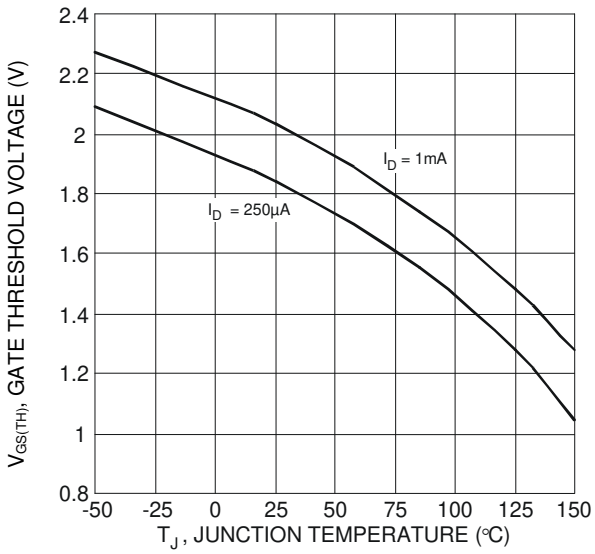

Figure 8 Gate Threshold Variation vs. Junction Temperature

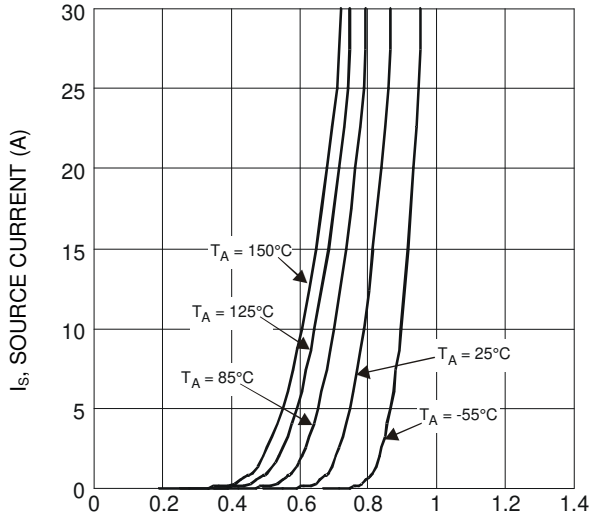

Figure 9 Diode Forward Voltage vs. Current

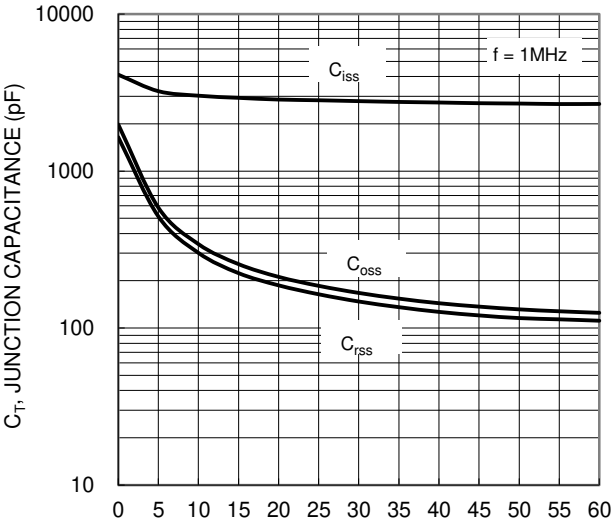

Figure 10 Typical Junction Capacitance

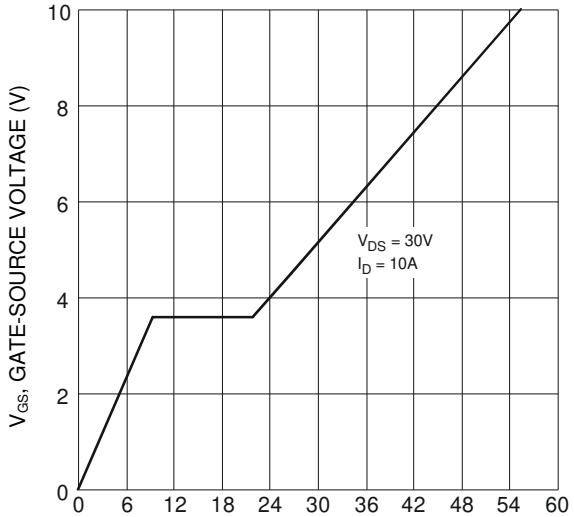

Figure 11 Gate Charge

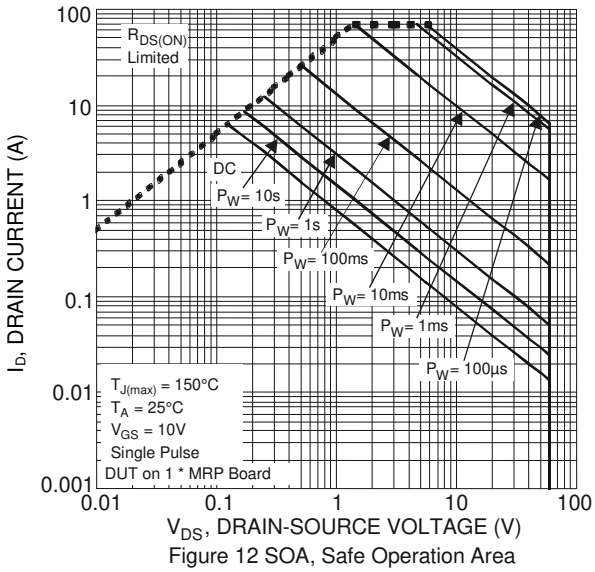

Figure 12 SOA, Safe Operation Area

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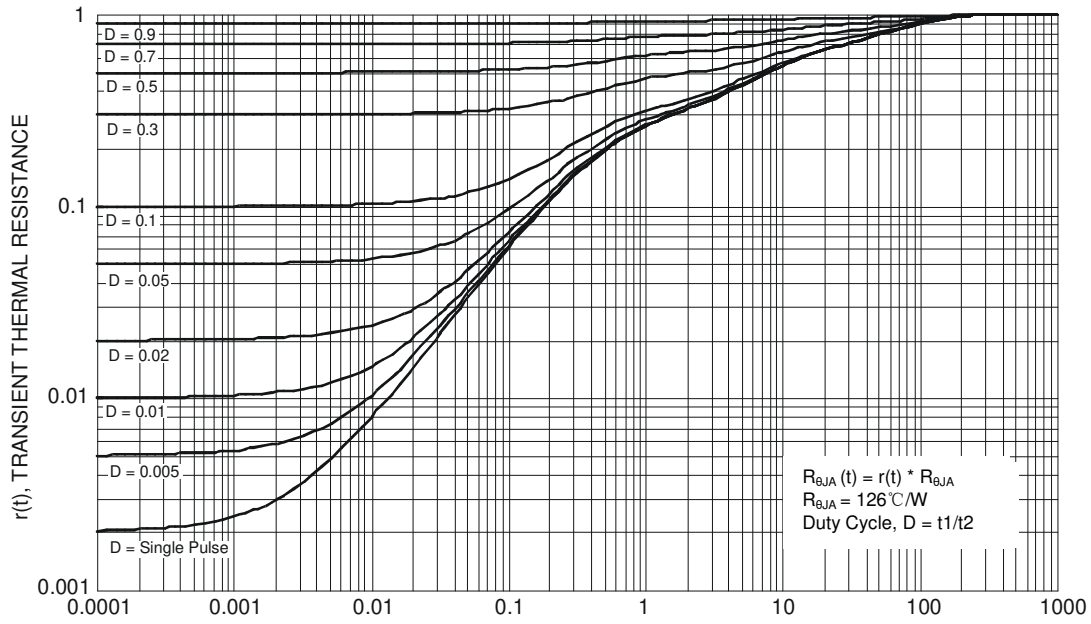

Figure 13 Transient Thermal Resistance

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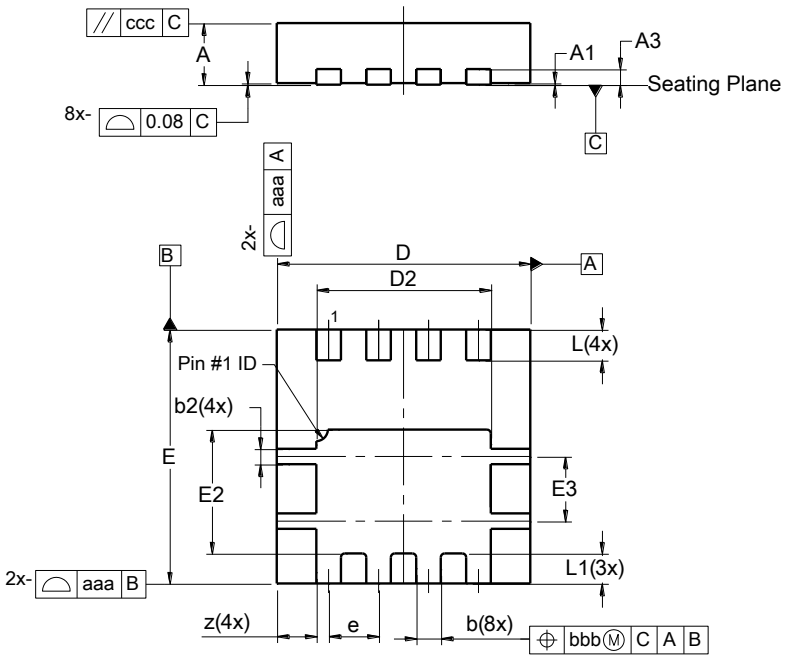
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8

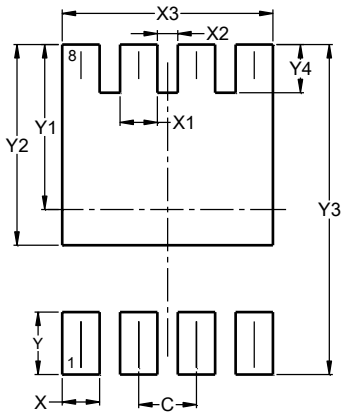


PowerDI3333-8			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	–	–	0.203
b	0.27	0.37	0.32
b2	–	–	0.20
D	3.25	3.35	3.30
D2	2.22	2.32	2.27
E	3.25	3.35	3.30
E2	1.56	1.66	1.61
E3	0.79	0.89	0.84
e	–	–	0.65
L	0.35	0.45	0.40
L1	–	–	0.39
z	–	–	0.515
aaa	0.25		
bbb	0.10		
ccc	0.10		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	0.420
X2	0.230
X3	2.370
Y	0.700
Y1	1.850
Y2	2.250
Y3	3.700
Y4	0.540

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