MAX77342

1.6A Adaptive DC-DC Step-Up Converter with High-Side Flash Driver

General Description

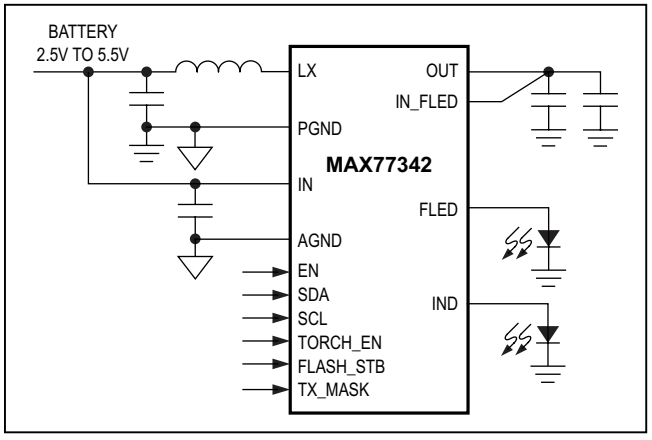
The MAX77342 provides a highly efficient solution for cell phone camera flash applications by integrating a 1.6A PWM DC-DC step-up converter and three programmable high-side, low-dropout LED current regulators. An I²C interface provides flexible control of the step-up converter, indicator, assist, torch, and flash mode selection, and flash safety timer duration settings.

The device operates down to 2.5V, making it future proof for new battery technologies. The step-up converter features an internal switching MOSFET and synchronous rectifier to improve efficiency and minimize external component count. Three high-side, high-current regulators provide support for indicator, assist, torch, and flash modes. They can source up to 1600mA in flash mode, 100mA in torch and assist light mode, and 16mA for indicator. The output voltage is adaptively controlled, stepping up voltage only as high as necessary to support the required LED forward voltage in flash mode. This approach reduces IC power dissipation by optimizing the step-up ratio and by minimizing the losses in the current regulator. In torch, assist light, and indicator, the current regulators are powered directly from IN, providing the highest system efficiency.

Additionally, the device includes a low input voltage protection function that reduces flash current during low battery conditions to prevent system undervoltage lockup.

Other features include shorted LED detection, overvoltage and thermal shutdown protection, and low-power standby and shutdown modes. The MAX77342 is available in a 16-bump, 0.5mm pitch WLP package (2.065mm x 2.065mm).

Simplified Block Diagram



Features

- 2.0V to 5.5V Operation Range
  - 2.5V to 5.5V with Full Functionality
  - 2.0V to 2.5V with Data Retention
- Step-Up DC-DC Converter
  - 1.6A Guaranteed Output Current for $V_{IN} \geq 3.0V$ and $V_{OUT} \leq 4.2V$
  - Adaptive Output Voltage Regulation Ensuring Highest System Efficiency Up to 90%
  - Down to 3.125% Duty Cycle
  - On-Chip Power MOSFET and Synchronous Rectifier
  - 1MHz/2MHz/4MHz PWM Switching Frequency
  - Small 1µH Inductor
- High-Side Flash/Torch/Indicator LED Current Regulator
  - I²C Programmable Flash Output Current (100mA to 1600mA in 100mA Steps)
  - I²C Programmable Torch Output Current (30mA to 100mA in 10mA Steps)
  - I²C Programmable Indicator Output Current (1mA to 16mA in 1mA Steps)
  - Adaptive Regulation Voltage (150mV typ) for Flash Mode
  - Low-Dropout Voltage (100mV max) for Torch Mode
- I²C Programmable Flash Safety Timer
- Open/Short LED Detection
- Tx Mask Reducing Output Current During Tx Event
- Overvoltage Protection
- Thermal Shutdown Protection
- 1µA Shutdown Current
- 16-Bump, 0.5mm Pitch, 2.065mm x 2.065mm WLP

Applications

- Cell Phones and Smartphones

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX77342.related.

19-6754; Rev 0; 9/13

maxim integrated™

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

IN to AGND.....-0.3V to +6.0V
OUT, IN_FLED to PGND.....-0.3V to +6.0V
EN, SDA, SCL, FLASH_STB, TORCH_EN, TX_MASK, IND to AGND ..... -0.3V to +(V_{IN} + 0.3V)
LX, FLED to PGND .....-0.3V to +(V_{OUT} + 0.3V)
AGND to PGND.....-0.3V to +0.3V
ILX Current (RMS per bump).....1.7A

Continuous Power Dissipation (T_A = +70°C)
16-Bump WLP (derate 20.4mW/°C above +70°C)....1632mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Bump Temperature (soldering) (Note 1).....+260°C

Note 1: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....49°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 3.6V, V_{PGND} = V_{AGND} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
IN Operating Voltage Range	V_{IN}			2.5		5.5	V
		Limited operation, current regulators are suspended but digital content preserved		2.0		2.5	
IN Undervoltage Lockout (UVLO) Threshold	V_{IN_UVLO}	V_{IN} falling where current regulators are disabled, 100mV typ hysteresis (V_{UVLO})		2.3	2.4	2.5	V
		V_{IN} falling power-on reset, 100mV hysteresis (V_{POR})		0.9	1.5	2.0	
IN Shutdown Supply Current	I_{SD}	EN = SCL = SDA = TORCH_EN = LOW	T_A = +25°C		0.4	1	µA
IN Standby Supply Current	I_{STDBY}	EN = HIGH, SCL = SDA = static, TORCH_EN = LOW	T_A = +25°C		1.3	5	µA
Internal Bias Startup Time	t_{BIAS_RDY}	From entering standby mode until any action can be performed			32	70	µs
LOGIC INTERFACE							
EN, TORCH_EN, TX_MASK, SDA, SCL Logic Input High Voltage	V_{IH}	V_{IN} = 2.5V to 4.5V		1.26		V_{IN}	V
FLASH_STB Logic Input High Voltage	V_{IH}	V_{IN} = 2.5V to 4.5V	VSEL_STB = 0	0.84		V_{IN}	
			VSEL_STB = 1	1.26		V_{IN}	

Electrical Characteristics (continued)

(V_{IN} = 3.6V, V_{GND} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EN, TORCH_EN, TX_MASK, SDA, SCL Logic Input Low Voltage	V_{IL}	V_{IN} = 2.5V to 4.5V				0.4	V
FLASH_STB, TORCH_EN, TX_MASK Pulldown Resistor to PGND	R_{PD}	V_{IH} = 1.5V		150	300	450	kΩ
Logic Input Current		V_{IL} = 0V or V_{IH} = 3.6V	T_A = +25°C	-1	0.01	+1	µA
FLASH_STB Detection Delay	$t_{FLASH\_STB\_DELAY}$	Time it takes to detect a FLASH_STB rising or falling edge	VSEL_STB = 0		6		ns
			VSEL_STB = 1		7		µs
I²C INTERFACE (Note 4)							
SDA Output Low Voltage		I_{SDA} = 3mA			0.03	0.4	V
I²C Clock Frequency						400	kHz
Bus-Free Time Between START and STOP	t_{BUF}			1.3			µs
Hold Time Repeated START Condition	t_{HD_STA}			0.6	0.1		µs
SCL Low Period	t_{LOW}			1.3	0.2		µs
SCL High Period	t_{HIGH}			0.6	0.2		µs
Setup Time Repeated START Condition	t_{SU_STA}			0.6	0.1		µs
SDA Hold Time	t_{HD_DAT}			0	-0.01		µs
SDA Setup Time	t_{SU_DAT}			100	50		ns
Setup Time for STOP Condition	t_{HD_STO}			0.6	0.1		µs
STEP-UP DC-DC CONVERTER							
Operating Supply Current		In PWM mode, I_{OUT} = 0mA, switching PWM mode (Note 4)			6		mA
OUT Voltage Range	V_{OUT}	Adaptive controlled		V_{IN}		5.15	V
Digital Overvoltage Threshold	V_{OVP_D}	Digital setting of 8-bit DAC (0XFF max)			5.15		V
OVP_D Debounce Timer	t_{OVP_D}	Time where adaptive regulation threshold is set at OVP_D threshold until current regulator and DC-DC regulator are disabled, I_{OUT} = 0mA		0.912	1.024	1.126	ms
Analog Overvoltage Threshold	V_{OVP_A}			5.35	5.425	5.50	V
Output Adaptive Regulation Step Size	V_{ADP_SS}	Smallest step size when output voltage is in adaptive regulation			10		mV
Adaptive Output Voltage Regulation Threshold	V_{ADP_REG}	I_{OUT} = 0mA		135	150	165	mV

Electrical Characteristics (continued)

(V_{IN} = 3.6V, V_{GND} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation		V_{IN} = 3.2V, V_{OUT} = 3.8V			200		mV/A
Active Discharge Resistor	$R_{OUT\_R\_DISC}$	V_{OUT} = 3.6V		25	50	75	Ω
Adaptive Sample Rate	f_{ADPT_SR}	Sampling frequency of adaptive regulation (Note 4)	During normal mode		62.5		kHz
			During soft-start		125		
Soft-Start Peak Current Limit	I_{LIM_SS}	Peak current limit during soft-start		290	415	500	mA
Low-Side Current Limit		V_{IN} = 2.7V, V_{FLED} = 4.2V (this is the static limit, dynamic value is slightly higher)	DCDC_ILIM = 00		1.25		A
			DCDC_ILIM = 01		1.95		
			DCDC_ILIM = 10		2.30		
			DCDC_ILIM = 11		2.80		
High-Side Zero-Crossing Threshold	I_{ZX}			35	42	50	mA
LX Low-Side On-Resistance		LX to PGND, I_{LX} = 200mA		30	50	80	mΩ
LX High-Side On-Resistance		LX to OUT, I_{LX} = -200mA		40	65	100	mΩ
LX Leakage		V_{LX} = 5.5V	T_A = +25°C		0.1	5	µA
			T_A = +85°C		1		
Operating Frequency	f_{SW}	V_{IN} = 2.5V to 4.4V, T_A = -40°C to +85°C		3.6	4.0	4.4	MHz
Maximum Duty Cycle	D_{MAX}				83		%
Minimum Duty Cycle	D_{MIN}	D_{MIN_4M} for frequency from 4MHz to 2MHz			12.5		%
		D_{MIN_2M} for frequency from 2MHz to 4MHz			6.25		
		D_{MIN_1M} for 1MHz frequency			3.125		
Maximum Duty Cycle for Shift Up in Frequency		D_{MAX_2M} for frequency from 2MHz to 4MHz			25		%
		D_{MAX_1M} for frequency from 1MHz to 2MHz			12.5		
Missing C_{OUT} Detection Threshold	V_{COUT_TH}	Maximum voltage threshold that V_{OUT} is allowed to discharge in time duration t_{COUT_DIS} before a COUT_DET fault is latched, only active for DIS_COUTDET = 0			150		mV
Missing C_{OUT} Detection Time	t_{COUT_DIS}	Time where OUT is discharged using I_{COUT_DIS} to determine if C_{OUT} is missing, only active for DIS_COUTDET = 0			12		µs
Missing C_{OUT} Detection Discharge Current	I_{COUT_DIS}	Discharge current from OUT to AGND during t_{COUT_DIS}, only active for DIS_COUTDET = 0			700		µA
Soft-Start Duration	t_{DCDC_SS}	V_{IN} = 2.5V to 4.4V, from enable triggered until soft-start completed		217	256	294	µs

Electrical Characteristics (continued)

(V_{IN} = 3.6V, V_{GND} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LED CURRENT SOURCE DRIVERS							
Current Regulator Supply Current from OUT		FLED supply current in flash mode			210		µA
Current Regulator Supply Current from IN		FLED supply current in torch/assist mode			110		µA
		IND supply current in indicator mode			40		
Flash Current	I_{FLASH}	In 100mA steps, I_FLASH[3:0]		100		1600	mA
TX_MASK Current Reduction Range		In 200mA steps, I_FLASH_TX[1:0]		200		800	mA
Low Voltage Current Reduction Range		In 200mA steps, I_LOW_V[1:0]		200		800	mA
Torch Current	I_{TORCH}	In 10mA steps, I_TORCH[2:0]		30		100	mA
Indicator Current	I_{IND}	Indicator mode output current range in 1mA steps, I_IND[3:0]		1		16	mA
TX_MASK Trigger Time	$t_{TX\_MASK\_DELAY}$	Time from when TX_MASK triggered until output current is lowered, rising edge only			20	200	µs
Minimum Output Current During TX_MASK/Low Voltage Event					100		mA
Assist and Torch Light High Current Time	$t_{TORCH2FINAL}$	Time duration that output current is set for 100mA (max) before ramping to final value		57	64	71	µs
Output Accuracy for Flash		1200mA to 1600mA	T_A = -5°C to +85°C	-5		+5	%
			T_A = -40°C to -5°C	-8		+8	
		100mA to 1200mA		-8		+8	
Output Accuracy for Assist/Torch		60mA to 100mA	T_A = -5°C to +85°C	-5		+5	%
			T_A = -40°C to -5°C	-8		+8	
		40mA to 60mA		-8		+8	
Output Accuracy for Indicator Mode		1mA to 16mA	T_A = -5°C to +85°C	-5		+5	%
			T_A = -40°C to -5°C	-8		+8	
FLED Current Regulator Dropout	$V_{FLED\_DROPOUT}$	500mA, 800mA, and 1600mA setting at -10%, powered from IN_FLED setting at -10% powered from IN_FLED			65	100	mV
		100mA setting at -10%, powered from IN			65	100	
IND Current Regulator Dropout	$I_{IND\_DROPOUT}$	I_{IND} = 24.5mA				100	mV
LED Leakage in Shutdown		V_{IN} = V_{IN_FLED} = 5.5V, V_{FLED} = 0V	T_A = +25°C		0.01	5	µA
			T_A = +85°C		0.1		
Flash Ramp Rate	t_{FLASH_RAMP}	FLED current ramp rise time, time it takes for current regulator to ramp from 0mA to full-scale current		445	496	550	µs

Electrical Characteristics (continued)

(V_{IN} = 3.6V, V_{GND} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Regulator Ramp Rate	t_{IRAMP}	Time between LSB step of torch, assist, or flash current during ramping up/down; in flash mode LSB consists of two 50mA steps	28.8	32	35.2	µs
Total Startup Time		t_{BIAS_RDY} + $t_{FLASH\_STB\_DELAY}$ + t_{BG_RDY} + t_{DCDC_SS} + t_{RAMP}, timing from flash strobe enabling flash mode until output current is at the 1600mA setting	670		1000	µs
Active Pulldown	$R_{IND\_LED\_PD}$	Indicator LED output active when current regulator is not active	50	100	150	Ω
Shorted LED Detection Threshold	V_{LED_SHORT}				1.0	V
Assist and Torch Light Open LED Detection Threshold		V_{IN} - V_{FLED}	0	20	40	mV
Indicator Light Open LED Detection Threshold		V_{IN} - V_{IND}	0	20	40	mV
FLED Output Current Ripple		At switching frequency		18		mA_{P-P}
		At adaptive sample rate		46		
Open and Short Debounce Timer		From LED short detected until LED current regulator is disabled	0.912	1.024	1.126	ms
TIMERS						
Flash Duration Timer Range	t_{FLASH}	In 1.024ms steps	1.024		262.144	ms
Flash Duration Timer Accuracy			-10	0	+10	%
TORCH_EN Debounce Timer	$t_{TORCH\_EN\_DB}$		5.5		9.0	ms
PROTECTION						
Thermal Shutdown	T_{SD}	T_J rising where the I^2C ENABLE register is reset		+160		°C
Thermal-Shutdown Hysteresis				20		°C
LOW-VOLTAGE DETECTION						
Low Battery Detect Threshold Range		In 100mV steps, sampled before current regulator is enabled, LOW_VOLTAGE_TH[2:0]	3.0		3.7	V
Low Battery Voltage Threshold Accuracy				±2.5		%
Minimum Output Current During LOW_VOLTAGE Event				100		mA

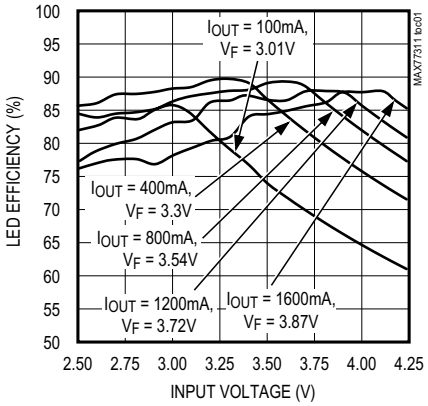
Note 3: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 4: Design guidance only, not tested during final test.

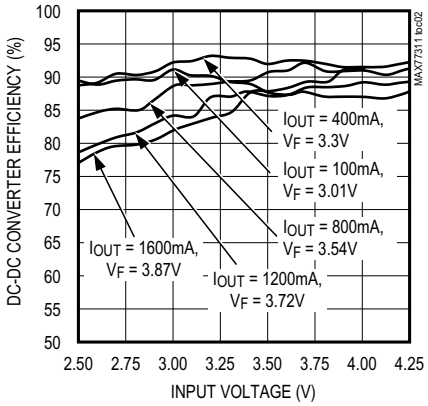
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

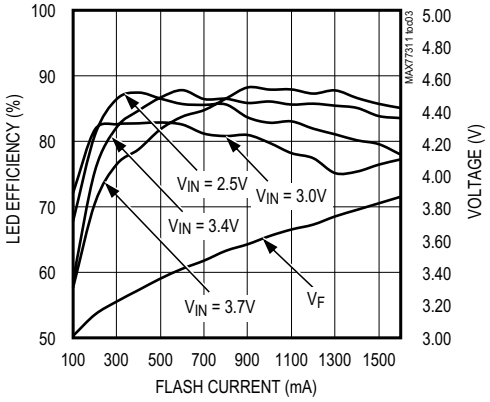
LED EFFICIENCY vs. INPUT VOLTAGE



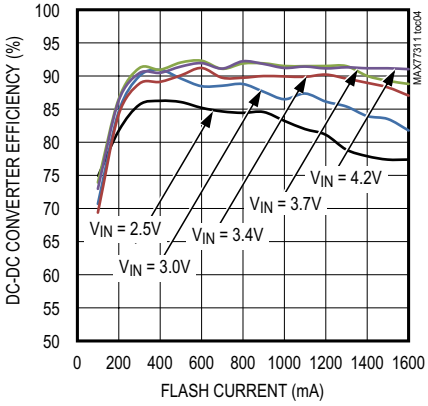
DC-DC CONVERTER EFFICIENCY vs. INPUT VOLTAGE



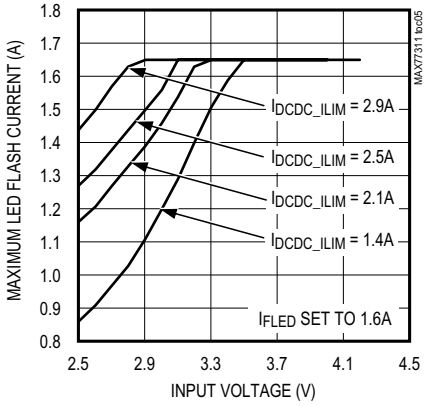
LED EFFICIENCY vs. FLASH CURRENT



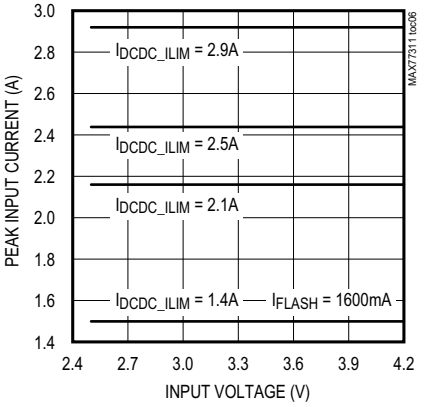
DC-DC CONVERTER EFFICIENCY vs. FLASH CURRENT



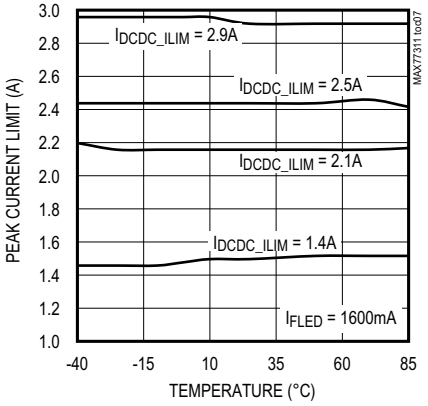
MAXIMUM LED FLASH CURRENT vs. INPUT VOLTAGE



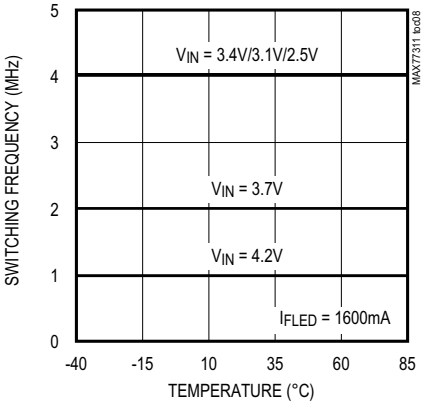
MEASURED PEAK INPUT CURRENT vs. INPUT VOLTAGE



PEAK CURRENT LIMIT vs. TEMPERATURE



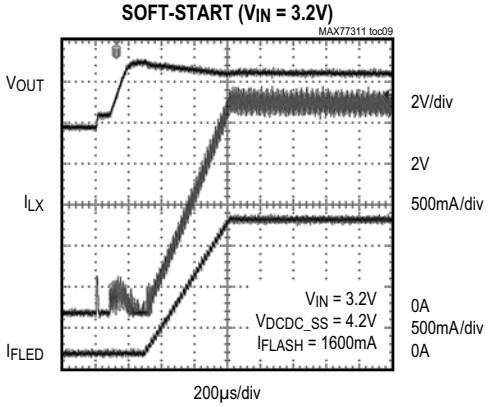
SWITCHING FREQUENCY vs. TEMPERATURE



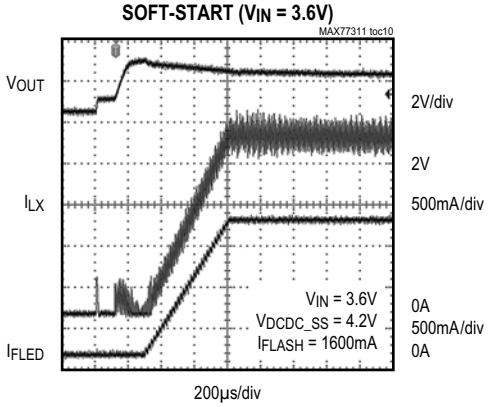
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

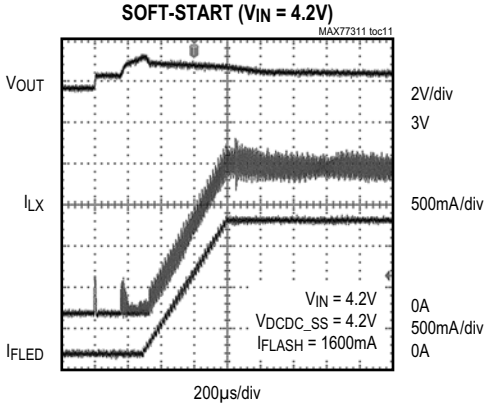
SOFT-START (V_{IN} = 3.2V)



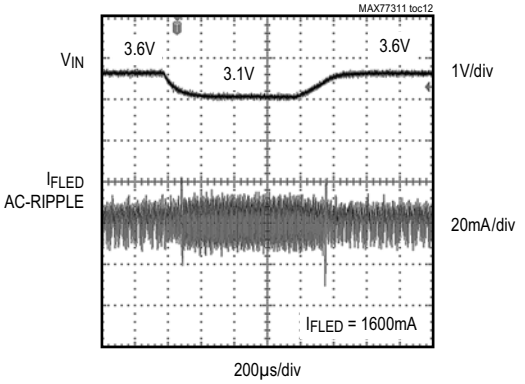
SOFT-START (V_{IN} = 3.6V)



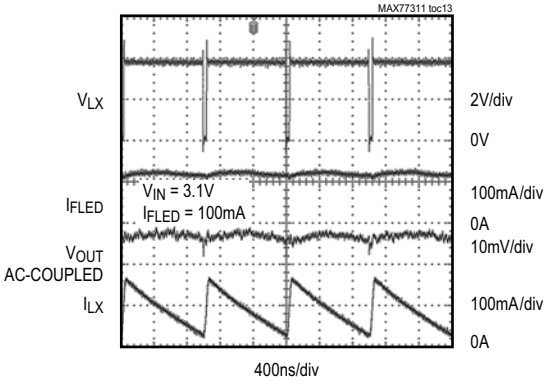
SOFT-START (V_{IN} = 4.2V)



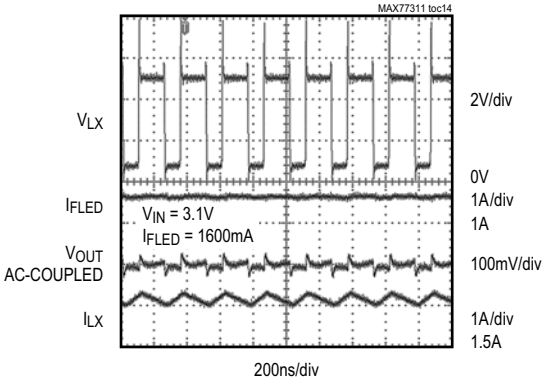
LINE TRANSIENT RESPONSE



LIGHT-LOAD SWITCHING WAVEFORM



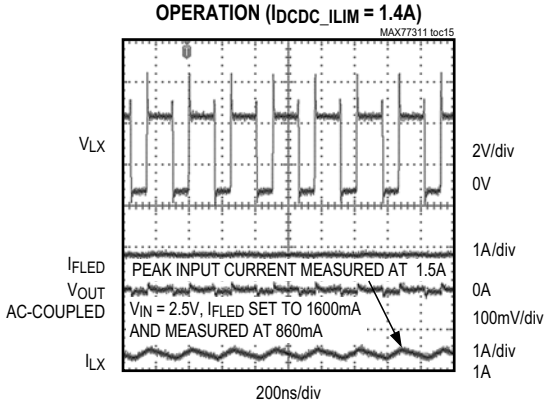
HEAVY-LOAD SWITCHING WAVEFORM



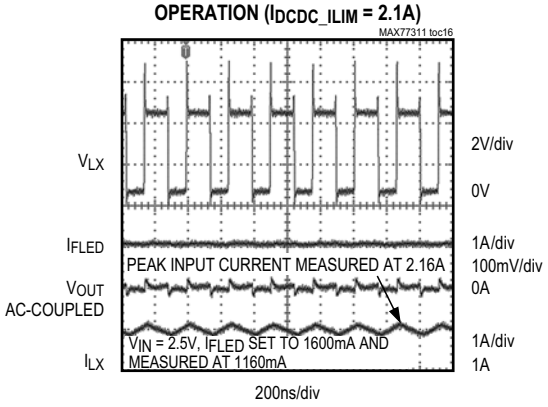
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

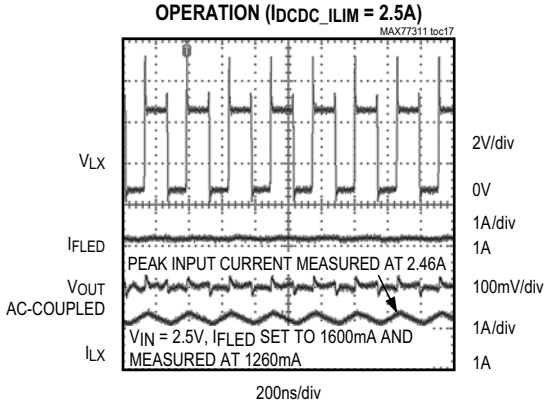
PEAK INPUT CURRENT LIMIT OPERATION (I_{DCDC_ILIM} = 1.4A)



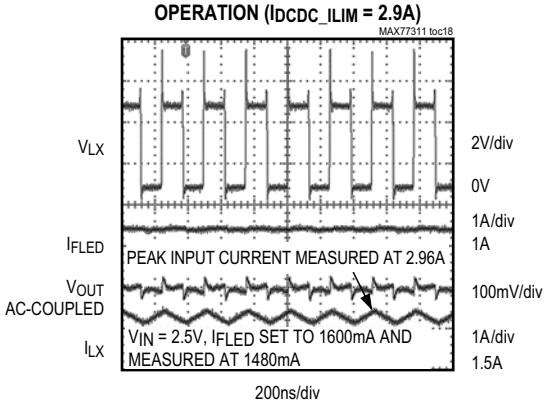
PEAK INPUT CURRENT LIMIT OPERATION (I_{DCDC_ILIM} = 2.1A)



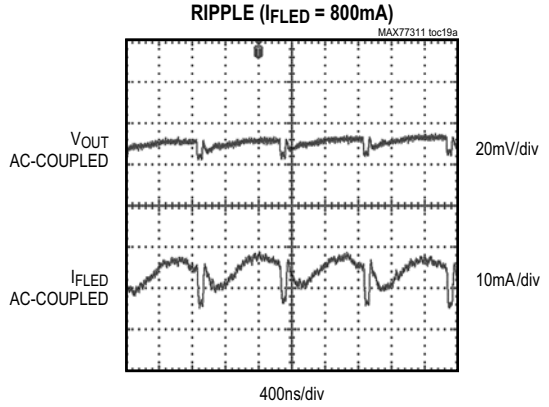
PEAK INPUT CURRENT LIMIT OPERATION (I_{DCDC_ILIM} = 2.5A)



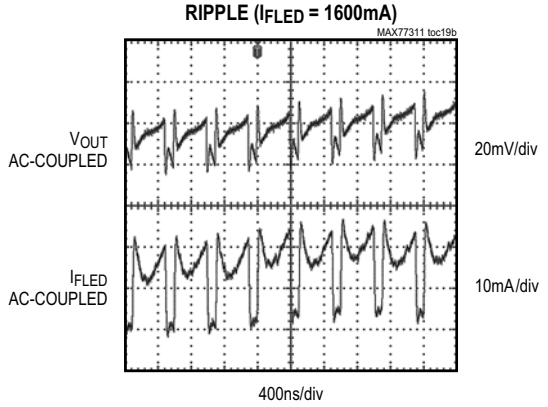
PEAK INPUT CURRENT LIMIT OPERATION (I_{DCDC_ILIM} = 2.9A)



I_{FLED} MEDIUM CURRENT RIPPLE (I_{FLED} = 800mA)



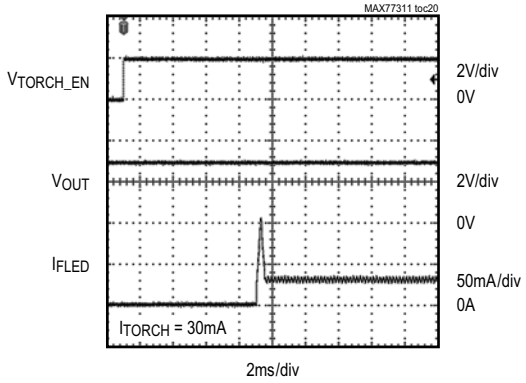
I_{FLED} HEAVY CURRENT RIPPLE (I_{FLED} = 1600mA)



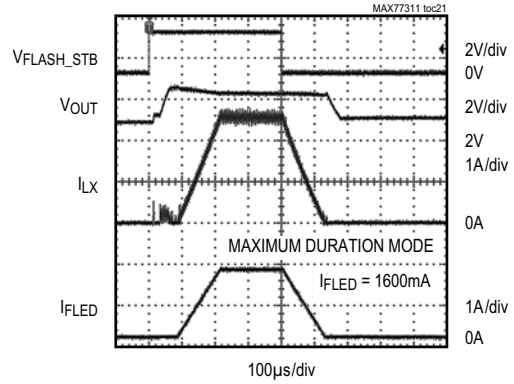
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

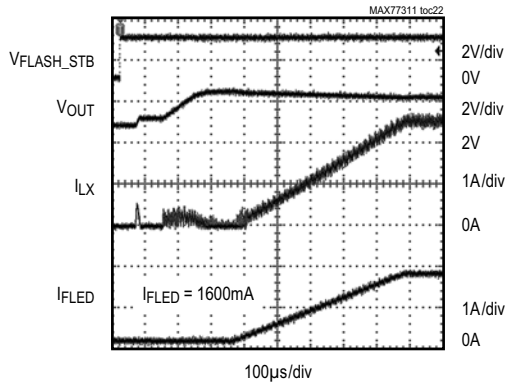
TORCH MODE ENABLE



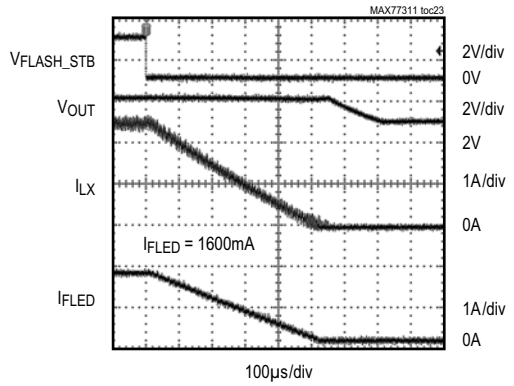
FLASH EVENT



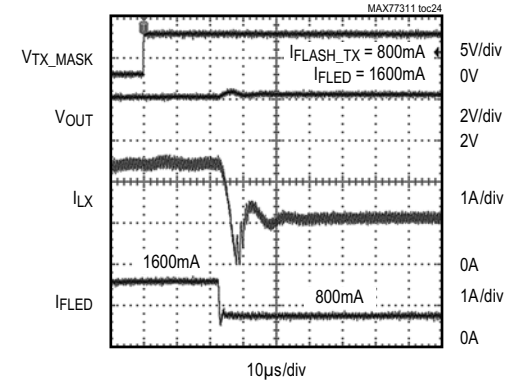
FLASH RAMP UP



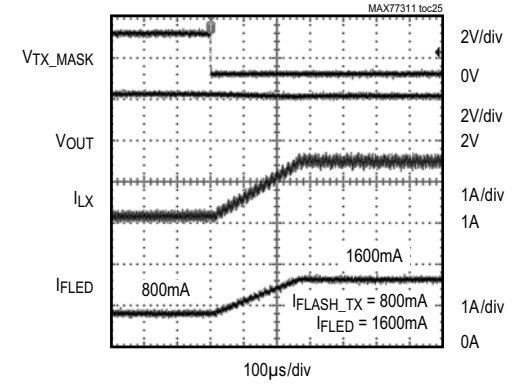
FLASH RAMP DOWN



TX EVENT ENTRY



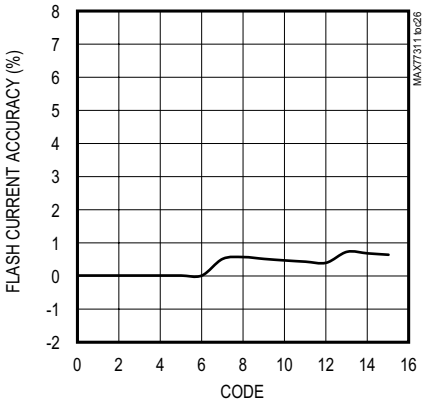
TX EVENT EXIT



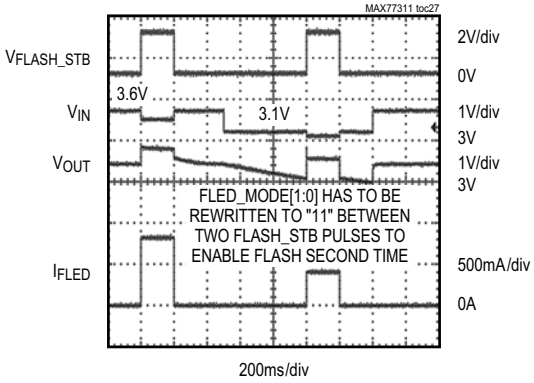
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

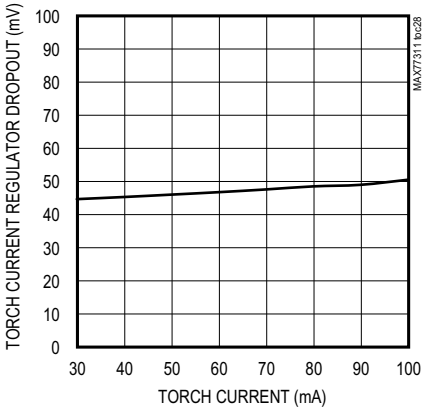
FLASH CURRENT ACCURACY vs. CODE



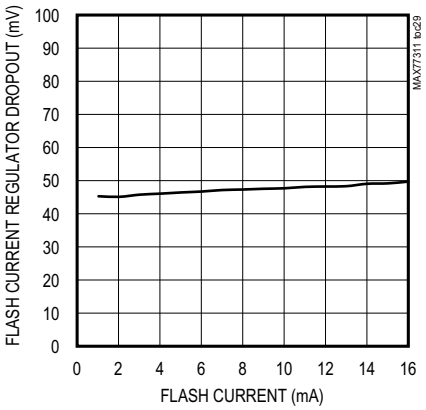
LOW VOLTAGE FUNCTION



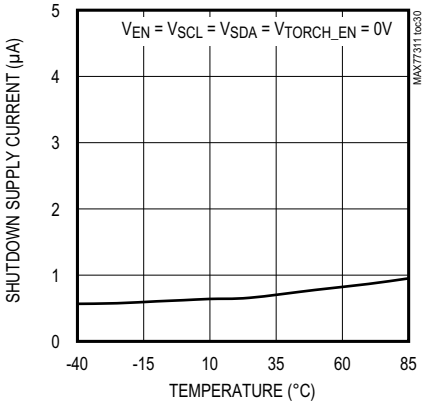
TORCH CURRENT REGULATOR DROPOUT vs. TORCH CURRENT



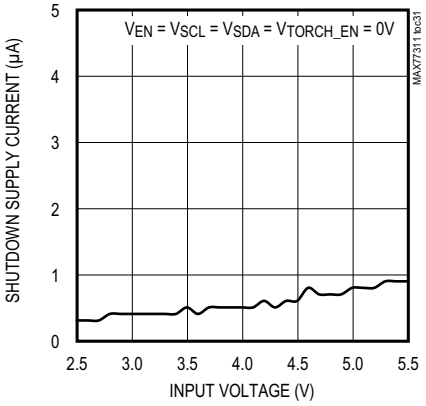
SINGLE-WIRE CURRENT REGULATOR DROPOUT vs. INDICATOR CURRENT



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



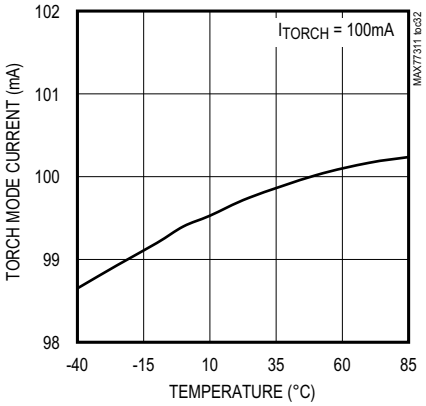
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



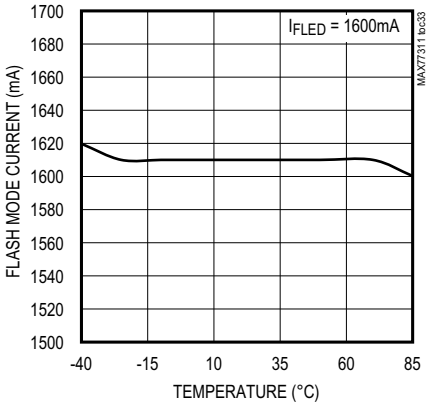
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

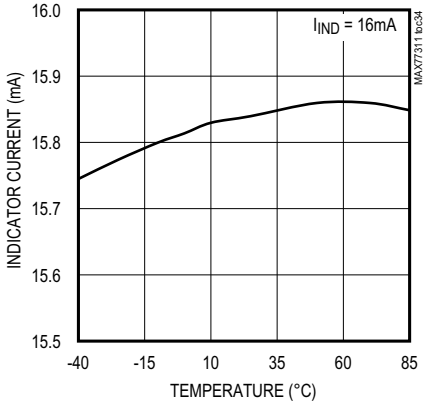
TORCH MODE CURRENT vs. TEMPERATURE



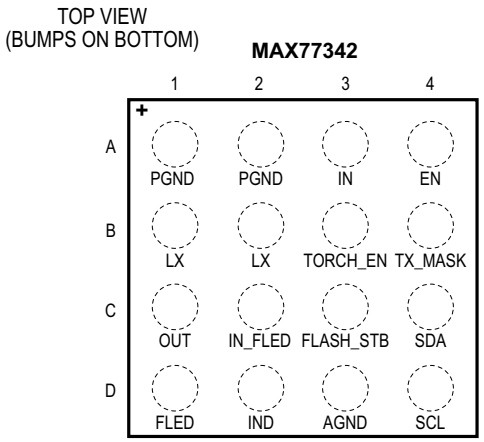
FLASH MODE CURRENT vs. TEMPERATURE



INDICATOR CURRENT vs. TEMPERATURE



Bump Configuration



16 WLP
(2.065mm x 2.065mm)

Bump Description

BUMP	NAME	FUNCTION
A1, A2	PGND	Power Ground for the DC-DC Converter. Connect PGND (A1 and A2 externally connected together) as close as possible to the IC. Make a star connection between the C_{IN} and C_{OUT} capacitor to ensure a short ground loop. Connect PGND to the common ground plane of the application.
A3	IN	Input Supply. Connect the IN bypass capacitor close to IN and the common ground plane. This input is used for low noise supply for internal bias, as well as torch, assist, indicator current regulators, and single-wire interface.
A4	EN	Enable Input. Logic-enable input used to transition from shutdown to standby mode. Pull EN logic-high to enter standby mode. This input is high impedance.
B1, B2	LX	Inductor Connection. Connect LX to the switched side of the inductor. LX is internally connected to the drain of the internal low-side MOSFET. LX is connected to OUT through the body diode of the high-side switch during shutdown. (Bumps B1 and B2 must be externally connected together.)
B3	TORCH_EN	Torch Mode Enable. Logic input that can be programmed to enable torch mode. TORCH_EN logic input has an internal 300kΩ pulldown resistor.
B4	TX_MASK	Tx Mask Input. This input can be programmed to set the reduction of flash current during a Tx event. Connect TX_MASK to the PA enable signal to limit the current drawn from the flash module during Tx of the system. The TX_MASK logic input has an internal 300kΩ pulldown resistor.
C1	OUT	DC-DC Step-Up Converter Output Voltage. Bypass OUT with two 10µF ceramic capacitors. OUT is not to be used to power other applications since the DC-DC step-up converter can only operate in adaptive mode. Bumps C1 and C2 must be externally connected together.
C2	IN_FLED	Flash Current Regulator Input Supply. It powers the flash current regulator. Bumps C1 and C2 must be externally connected together.

Bump Description (continued)

BUMP	NAME	FUNCTION
C3	FLASH_STB	Flash Event Trigger. Logic input that can be programmed to trigger the flash event. The FLASH_STB logic input has an internal 300kΩ pulldown resistor.
C4	SDA	I²C Data Input. Data is read on the rising edge of SCL and data is clocked out on the falling edge of SCL.
D1	FLED	Flash LED. High-side current regulator output. Current flowing out of FLED is set by I²C register settings. Connect FLED to the anode of a flash LED or LED module.
D2	IND	IND is used to drive a separate indicator LED. IND is pulled to AGND with an internal 100Ω resistor when the single-wire driver is disabled.
D3	AGND	Analog Ground. Connect AGND to the common ground plane of the application.
D4	SCL	I²C Clock Input. Data is read on the rising edge of SCL.

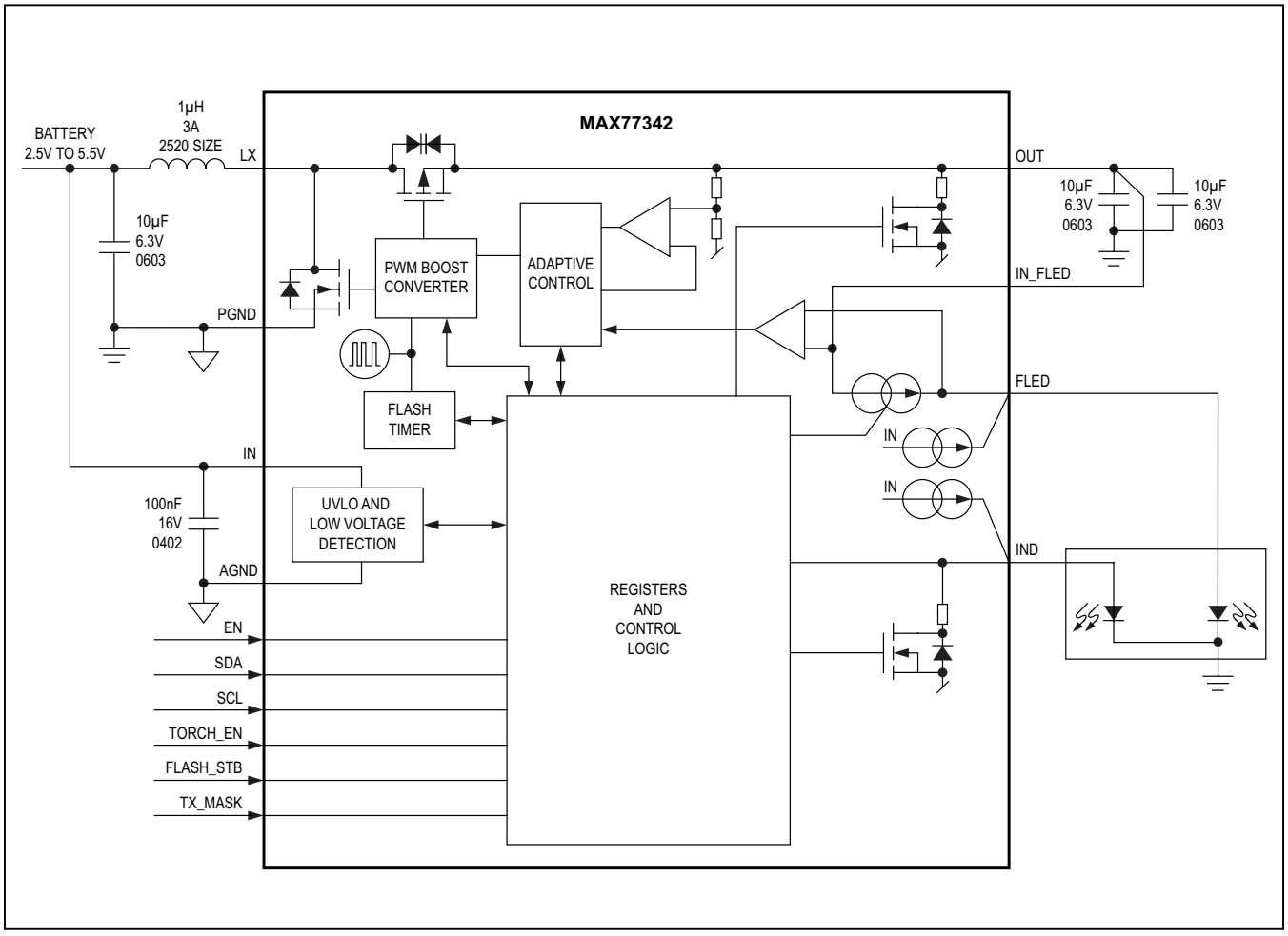


Figure 1. Typical Application Circuit and Simplified Diagram

Detailed Description

The MAX77342 flash driver IC integrates an adaptive 1.6A PWM step-up DC-DC converter, and three high-side current regulators: one for LED camera flash powered by the adaptive DC-DC step-up converter, one for torch/assist light applications powered directly from IN, and one for indicator mode powered directly from IN. An I^2C interface controls output current settings for indicator, torch, assist, and flash mode, enabling torch, assists, and flash mode as well as flash timer duration settings.

Step-Up Converter

The IC includes a PWM step-up converter with frequency scaling, optimizing efficiency for low duty cycle operation. The output voltage of the DC-DC step-up converter is adaptive controlled, based on the forward voltage of the installed LED. It is therefore not recommended to use the DC-DC step-up converter output to power other applications.

During soft-start, the converter is allowed to operate in discontinuous mode. Once the current regulator ramp-up is initiated, the converter is forced into PWM mode. In cases where V_{IN} is close to the required V_{OUT} or even higher, the converter is required to operate at as low of a duty cycle as possible, while still operating in PWM mode. Therefore, the device scales the frequency of the converter depending on the required duty cycle to ensure the output is kept within regulation. See Figure 2.

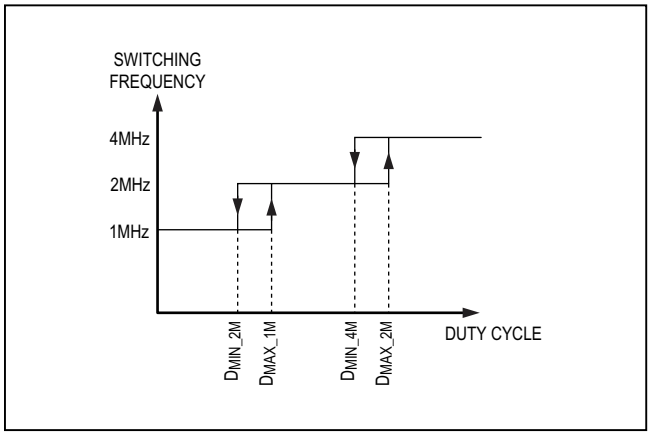


Figure 2. Switching Frequency Scaling

During output voltage ramping, the inductor peak current is limited through the low-side nMOS power switch to load the battery as little as possible during the charging of the output capacitor. In the same time, the output voltage ramping is also controlled to avoid high output dV/dt.

When the DC-DC converter is disabled, the OUT node is actively discharged until it reaches V_{IN} - 150mV (typ). This ensures that the output voltage is always at V_{IN} level when the DC-DC converter is enabled. This is done to prevent the output from discharge through the high-side switch, resulting in current being reversed back to the input capacitor.

DC-DC Converter On/Off Control

The DC-DC converter is automatically enabled when the current regulator is enabled in flash mode only, and automatically turns off again once the current regulator is disabled. The operation mode of the DC-DC converter is determined by the voltage headroom across the current regulator. The OUT voltage is regulated V_{ADP_REG} above FLED voltage. If the adaptive control loop detects that the converter is operating in minimum duty cycle mode, the adaptive regulation prevents the internal regulation loop to decrease the output voltage, since the converter, in this case, is no longer operating in closed loop. In this mode of operation the output is regulated to $V_{IN} \times D_{MIN\_1M}$.

Soft-Start

When the input supply is initially applied to the device, the output capacitor is charged to the input supply minus a diode drop. During this charging period, there is no limit of the input current. The output capacitor is charged through the internal body diode of the high-side switch. This initial charge is done with the high-side switch configured as a current source. In the second phase of soft-start, the converter is starting to switch at 1MHz with the high-side switch disabled. This is done to prevent large dI/dt current to be drawn from the input. As the output rises, the converter changes the switching frequency to first 2MHz and then 4MHz. Once operating at 4MHz, the high-side switch is enabled. The output ramps from V_{IN} to DCDC_SS level. Once the converter has completed the soft-start, it is forced into PWM mode and the current regulator is now allowed to ramp.

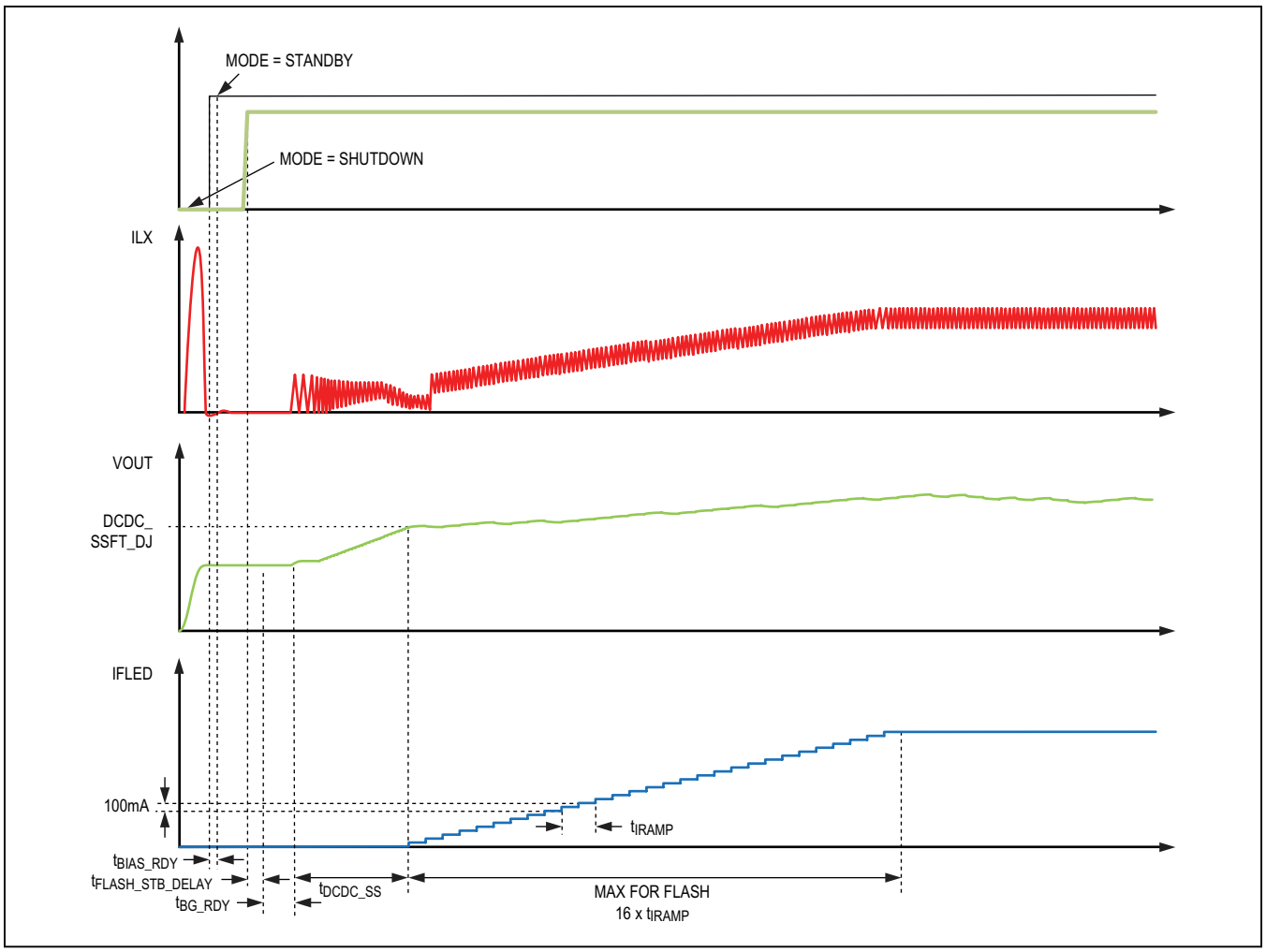


Figure 3. DC-DC Converter Soft-Start

Output Capacitor Fault

If the output capacitor is missing, the output ripple of the DC-DC converter increases significantly. This condition trips an OVP_A fault condition. Since it cannot be determined if the OVP was due to a missing capacitor or other reasons, an additional test can be performed to determine if the capacitor is missing or not.

To activate this test, clear DIS_COUTDET function in register 0x23h.

When the C_{OUT} detection is enabled, upon enabling a flash event, the DC-DC converter first precharges the output to IN, then monitors the V_{OUT} against the V_{IN} to see if the output drops within a specified time interval. If the output drops below V_{COUT_TH} 150mV (typ) of the IN, it indicates that no output capacitor is present on the output. Since the voltage difference between IN and OUT is only V_{COUT_TH} (150mV), this test is sensitive to large ripple on the input, which can easily trip the missing C_{OUT} detection. It is therefore recommended to only activate the C_{OUT} detection when no other significant load is present at the battery. If missing C_{OUT} is detected, a fault condition is latched into the fault register. To resume operation after the fault, the fault must be cleared by reading.

Adaptive Output Voltage Regulation

The adaptive regulation scheme for the device is achieved using a digital regulation control loop. The output voltage is controlled using an internal 8-bit DAC with a 2.6V to 5.3V range and a step size of V_{ADP_SS} (10mV). The effective output voltage range is limited by minimum duty cycle for the lower limit and the upper limit is limited by the OVP_D (5.15V) threshold or the peak current limit of the converter.

When the converter is initially enabled, the converter first performs a soft-start cycle. During this time the output of the converter is charged up to the DCDC_SS threshold. This is done before the current regulator is enabled to ensure there is sufficient headroom to operate the current regulator.

Once the soft-start is completed, the current regulator is enabled. The device samples the voltage headroom across the current regulator to determine if the output voltage should be regulated to a higher threshold.

The adaptive regulation has two different behaviors depending on if the current regulator is ramping up the current or if the current has reached the final steady-state level.

During current ramping up, reducing the output voltage is not allowed by the adaptive regulation. This is done to ensure that sufficient headroom is always available for the current regulator. The voltage across the current regulator is sampled every f_{ADPT_SR} (125kHz) and the output is then adjusted V_{ADP_SS} (10mV) up or kept at present level if sufficient headroom is detected.

During the final steady-state current level, the voltage across the current regulator is sampled at a lower frequency, every f_{ADPT_SR} (62.5kHz) and the output is then adjusted V_{ADP_SS} (10mV) up or down depending on the current regulator headroom.

If the input current limiter is tripped, the device adaptive control blocks the output voltage from increasing. This is an indication that insufficient energy is available and the output is not within regulation. Therefore, increasing the output voltage in this case does not result in an actual increase of output voltage, since the input current is limiting the output voltage.

If the adaptive regulation is trying to regulate the output voltage to a higher threshold than the OVP_D threshold, the adaptive control loop limits the output voltage to the OVP_D threshold. If the output condition is trying to regulate the output voltage above the OVP_D threshold for a duration longer than t_{OVP_D} 1.024ms (typ), this generates a fault condition meaning that the FLED is open and disables the DC-DC converter and the FLED driver.

Once the initial ramp up of the current regulator is completed, the sample rate of the adaptive regulation threshold f_{ADP_SR} is changed from 125kHz to 62.5kHz. This is done to ensure slow changes on the output, hence reducing EMI issues. In addition, the output voltage is now allowed to either ramp up or down one LSB depending on the voltage headroom measured across the current regulator. The only exception for this is during the following conditions:

1) Input current limit active. In this case the output is only allowed to decrease if sufficient headroom is detected for the current regulator.
2) Output exceeding overvoltage threshold, OVP_D. In this case the output is only allowed to decrease if sufficient headroom is detected for the current regulator.

Using the I^2C register, it is possible to read out the actual adaptive output voltage regulation threshold. This value is stored in the DCDC_OUT register, making it possible for the application to determine what the adaptive output voltage is within the expected range for the current operation. This result can be used to determine the condition of the external LED as well as for fault indication.

During a flash event, the adaptive maximum voltage is stored in the DCDC_OUT_MAX I^2C register. This information can be used to determine the actual forward voltage of the LED as well as the peak voltage condition during the flash event.

See Figure 4 for a state diagram of the adaptive regulation function.

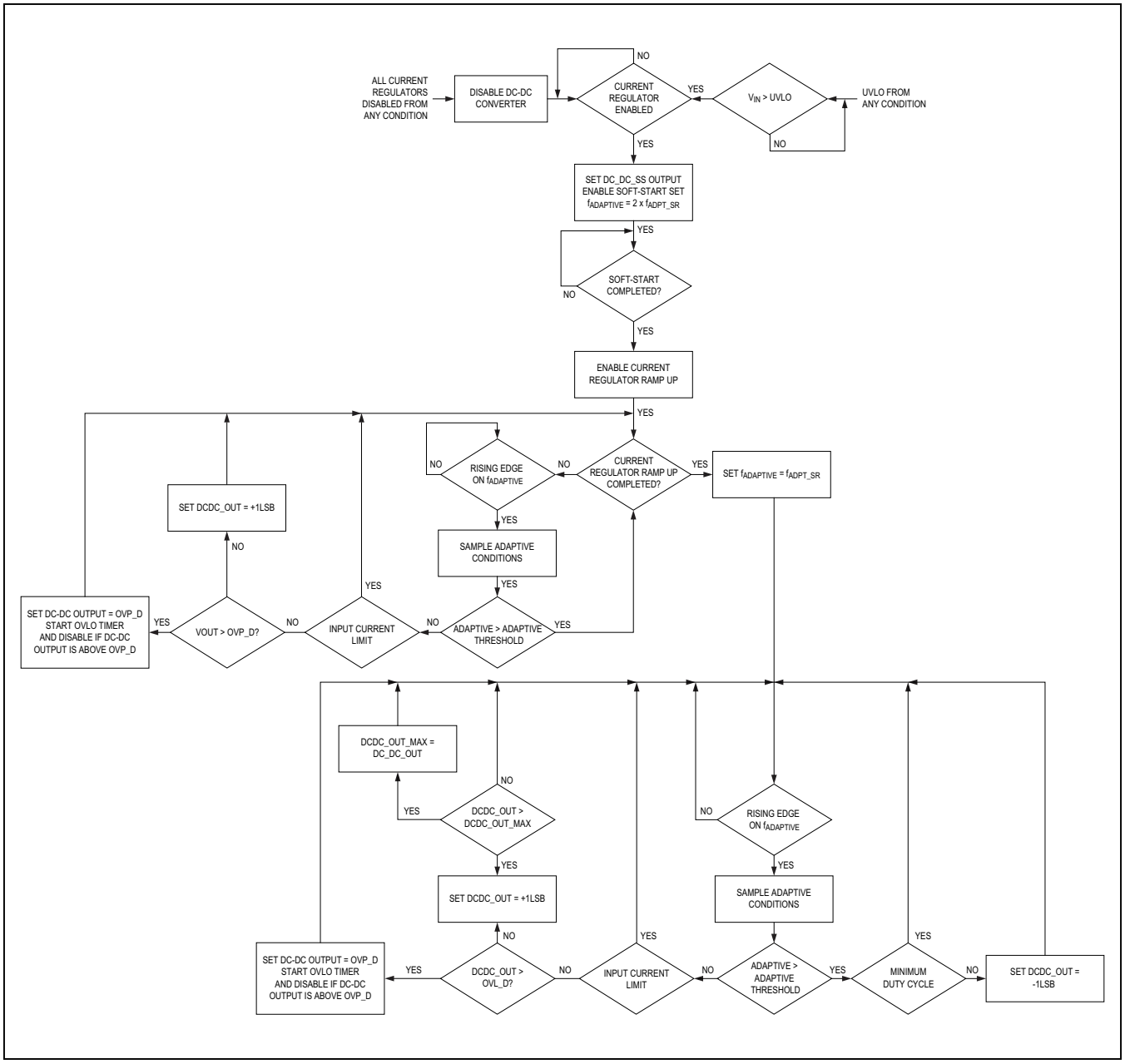


Figure 4. Adaptive Output Voltage Regulation State Diagram

Overvoltage Protection

The device includes two overvoltage protection circuits. The first protection mechanism is part of the adaptive regulation control, and limits the converter output voltage to the OVP_D threshold for a duration of t_{OVP_D} (1.024ms) before the current regulator and the DC-DC converter are disabled.

The second protection mechanism is set to trigger on a higher threshold, but has a much faster reaction time. If the output voltage rises above the OVP_A threshold, the converter and current regulators are disabled within a reduced time delay.

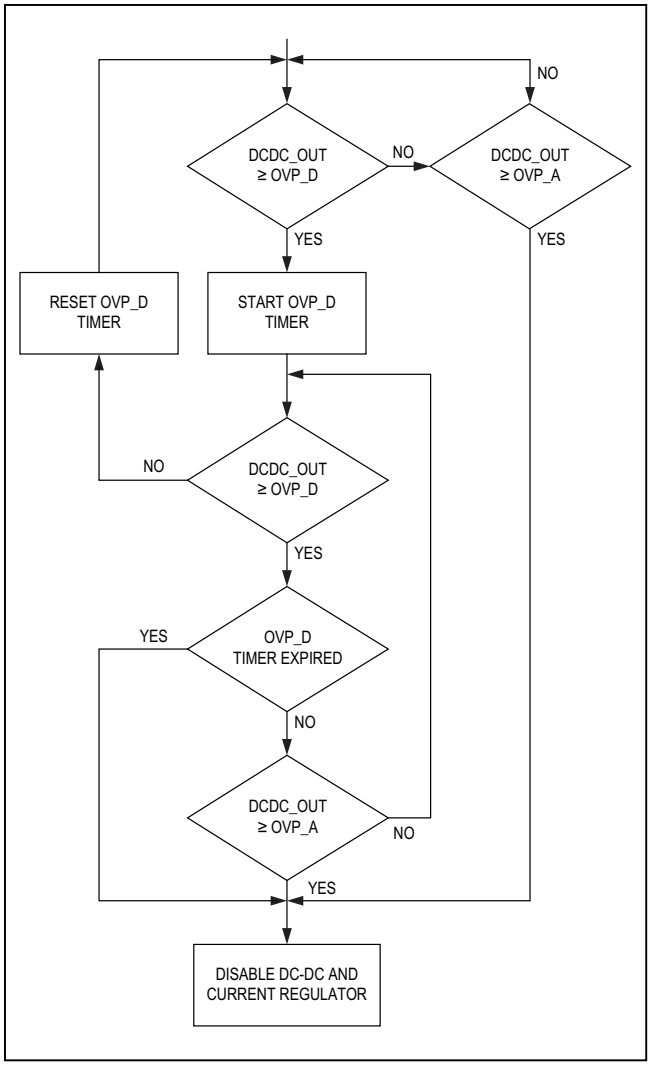


Figure 5. Overvoltage State Diagram

Low-Side Current Limit

The device provides a programmable current limit for the low-side switch. This current limit functions as an input current limit, and is critical for the application, since this function determines the maximum current that can be drawn from the input supply. This low-side current limit is also important for the choice of inductor, since it determines the minimum saturation current, to avoid the inductor hitting saturation.

If the input current limit is reached during operation, the low-side switch terminates the cycle and turns on the high-side switch. This results in a drop of the output voltage. The device operates in continuous input current limit condition, but due to a drop in output voltage, the current regulator parameters cannot be guaranteed in this mode of operation. For a duty cycle lower than the minimum duty cycle the converter cannot limit the current. This is due to the fact that the current in the inductor does not discharge sufficiently during the OFF-time to ensure that the LX peak current does not hit the peak current limit within the time for the minimum duty cycle. In application though, this is only an issue if the flash current is set to 80% min of the peak current limit.

LED Current Regulator

The MAX77342 has three internal high-side current regulators. They are connected to two outputs, FLED and IND.

The FLED output is used for flash, torch, and assist light mode using the following current regulators.

- Flash mode current regulator
- Assist/torch mode current regulator

The IND output is used for indicator and consists of a single current regulator that is always powered directly from IN.

Each of the current settings is flexibly controlled by the I^2C interface.

Indicator Mode

Indicator mode operates separate from the torch, assist, and flash modes, since it has a dedicated output.

The current regulator for IND is directly powered from the IN, and always regulates to 2.9V (min) or operates in dropout for V_{IN} voltages less than 3.0V ($V_{IND\_DROPOUT\_REG}$) when it is used. This is done to ensure that a minimum 2.9V is always available for the IND interface.

Torch Mode

Torch mode can be activated from either standby mode or shutdown mode. The only way to enable the torch mode in shutdown mode is by using the TORCH_EN logic input. In standby mode, the torch mode can be enabled by two conditions:

1) TORCH_EN when TORCH_EN_MASK is set, FLED_EN is set, and FLED_MODE = 00
2) FLED_EN when TORCH_EN_MASK is cleared and FLED_MODE = 00

The TORCH_EN logic input has a debouncer at the input to ensure that the logic input can be used by non GPIO control. When TORCH_EN is initially pulled high, it must be high for $t_{TORCH\_EN\_DB}$ before torch mode is activated. Once in torch mode, TORCH_EN must be low for $t_{TORCH\_EN\_DB}$ for the device to go back to standby or shutdown mode.

When torch mode is enabled, the output current is first ramped with a rate of 10mA/32µs, from 30mA to 100mA. This is done to control the ramp rate of the current into the LED. Open/short detection is performed once the output current reaches full scale. In case a fault is detected, the current regulator is disabled and the device enters standby or shutdown state depending on the logic EN input. After $t_{TORCH2FINAL}$ the current is ramped down from 100mA to the final value with a rate of 10mA/32µs.

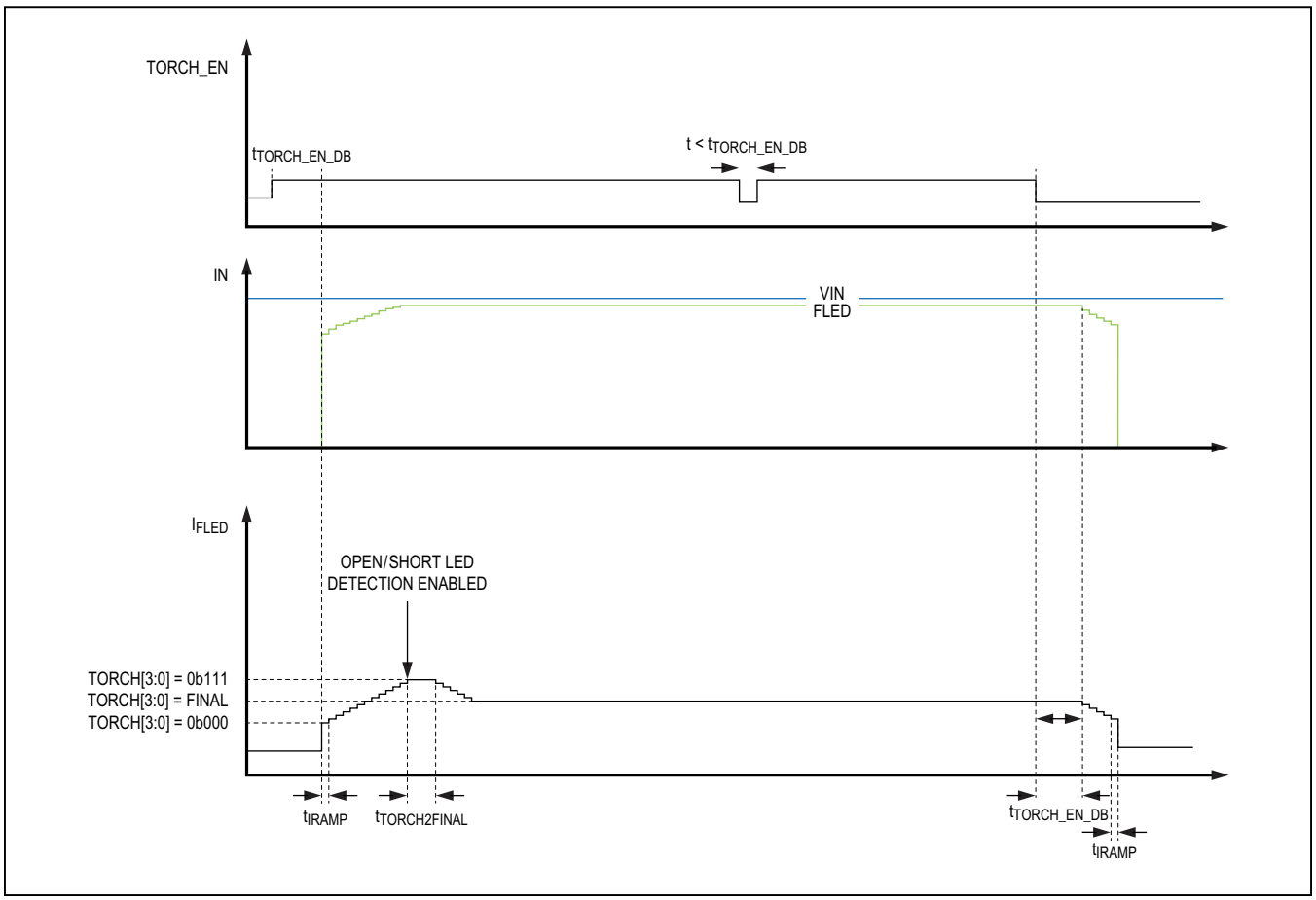


Figure 6. LED Ramping During Torch Mode

The current regulator for assist and torch operation is powered directly from IN. This provides the best efficiency for the system, but limits the operation range of the current regulator. For LED with higher V_F than V_{IN} - $V_{DROPOUT}$ (100mV at 10% drop for assist and torch mode), the current regulator enters dropout operation and during this mode of operation, the output current is limited by the external LED V_F vs. I_F curve.

Assist Light

Assist light can only be activated from standby mode. The assist light can be activated using either the I^2C interface or the logic input FLASH_STB. The assist mode can be enabled by two conditions:

1) FLASH_STB when FLASH_STB_MASK is set, FLED_EN is set, and FLED_MODE = 10
2) FLED_EN when FLASH_STB_MASK is cleared and FLED_MODE = 10

When enabling the assist light using the FLASH_STB, there is no debounce on the logic input.

When assist light mode is enabled, the output current is first ramped with a rate of 10mA/32µs, from 30mA to 100mA. This is done to control the ramp rate of the current into the LED. Open/short detection is performed once the output current reaches full scale. In case a fault is detected, the current regulator is disabled and the device enters standby. After $t_{TORCH2FINAL}$ the current is ramped down from 100mA to the final value with a rate of 10mA/32µs.

The current regulator for assist and torch light operation is powered directly from IN. This provides the best efficiency for the system, but limits the operation range of the current regulator. For LED with higher V_F than V_{IN} - $V_{DROPOUT}$ (100mV at 10% drop for assist and torch mode), the current regulator enters dropout operation and during this mode of operation output current is limited by the external LED V_F vs. I_F curve.

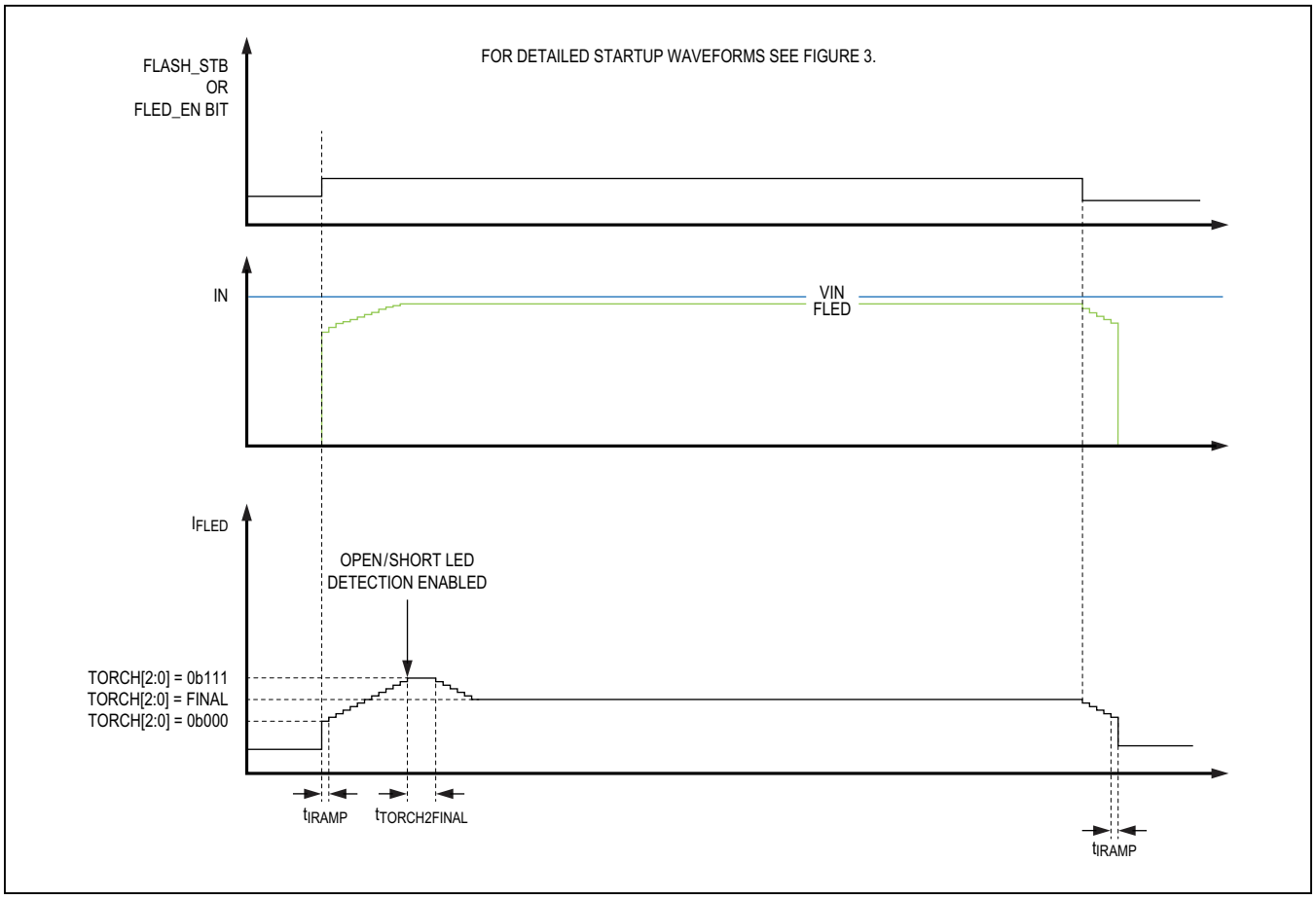


Figure 7. LED Ramping During Assist Light Mode

Flash Mode

In flash mode, the current regulator can be enabled using the I2C interface or by using logic FLASH_STB logic input if the I2C FLASH_STB_MASK bit is set.

When the flash mode is enabled, the IC first performs a soft-start of the DC-DC converter to bring the output voltage to a level where the LED starts to conduct current. Once this is completed, the output current of the FLED is ramped at a rate of 50mA/16.5kHz or 100mA/32.125kHz to control the ramp rate of the current into the LED. The ramp rate is divided into 50mA sections to allow for smoother transition on output.

At the 100mA setting the open/short detection is enabled. In case a fault is detected, the current regulator is disabled and the IC enters standby or shutdown state depending on the EN input. Once the open/short detection is performed and passed, the IC continues to ramp the output current to the final value.

Enable of Current Regulator

FLED Current Regulator

The flash current regulator can be enabled using the I2C interface for assist or torch mode or by a dedicated logic input, FLASH_STB. The torch light mode can be enabled using the I2C interface or by the logic TORCH_EN input.

The current regulators can be enabled from two different modes of operation.

- Shutdown mode (torch mode only)
- Standby mode (torch/assist or flash)

In shutdown mode, the only mode that can be activated is torch mode. Torch mode can only be activated using the TORCH_EN, and only when the TORCH_EN_MASK bit is set.

In standby mode, the FLED current regulator can be enabled in the following configurations:

- **Torch mode (FLED_MODE = “00”).** Enabled using the TORCH_EN logic input when the following conditions are met: EN is logic-high and the TORCH_EN_MASK bit is set. In this mode the output current is set to I_TORCH.
- **Assist light (FLED_MODE = “10”).** The assist light can be enabled using the FLASH_STB logic input or by using the I2C interface. Enable assist light with the FLASH_STB logic input when the following conditions are met: EN is logic-high, the FLED_EN bit is set, and the FLASH_STB_MASK bit is set. Alternatively, the assist light can be enabled using the I2C interface. This is done by setting the FLED_EN bit when the following conditions are met: EN is logic-high and the

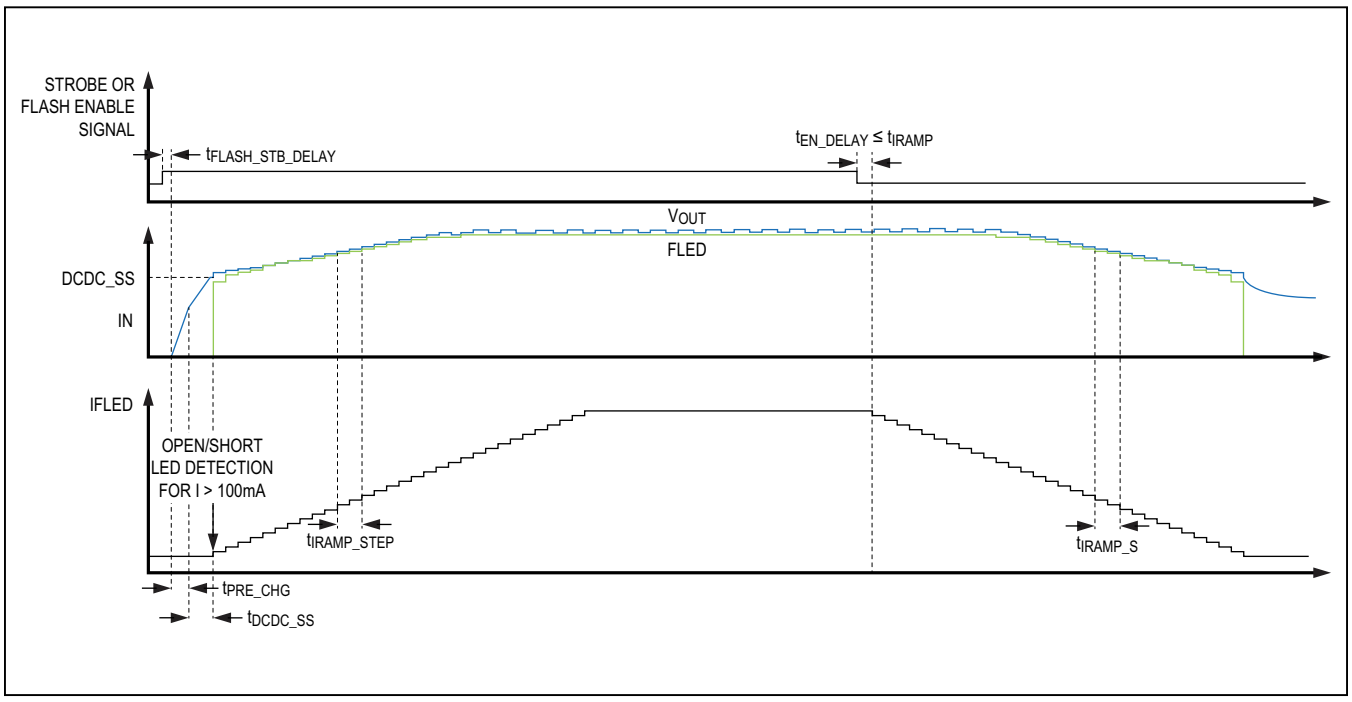


Figure 8. LED Ramping During FLASH Mode

FLASH_STB_MASK bit is cleared. In this mode the output current is set to I_TORCH.

- **Flash mode (FLED_MODE = 11).** Flash mode can be enabled using the FLASH_STB logic input or by using the I2C interface. Enable flash mode with FLASH_STB logic input when the following conditions are met: EN is logic-high, the FLED_EN bit is set, and the FLASH_STB_MASK bit is set. Alternatively, flash mode can be enabled using the I2C interface. This is done by setting the FLED_EN bit when the following conditions are met: EN is logic-high and the FLASH_STB_MASK bit is cleared. The duration of the flash mode by using FLASH_STB is determined by the FLASH_TMR_CNTL bit and can be set to either maximum duration (level sensitive) or one-shot (edge sensitive) mode. If flash mode is enabled using the I2C interface, the FLASH_TMR_CNTL bit is ignored, and the duration of the flash is determined by the FLASH_TMR setting. In this mode the output current is set to I_FLASH.
- **IND interface (FLED_MODE = 01, IND_SEL = 1)**

Indicator mode can be enabled using the FLASH_STB logic input or by using the I2C interface. Enable indicator mode with FLASH_STB logic input when the following conditions are met: EN is logic-high, FLED_EN bit is set, and FLASH_STB_MASK bit is set. Alternatively, the indicator mode can be enabled using the I2C interface. This is done by setting the FLED_EN bit when the following conditions are met: EN is logic-high and the FLASH_STB_MASK bit is cleared.

Ramping UP/DOWN Current Regulator for FLED Current Regulator Only

The current regulator has a ramp function that is engaged every time the current regulator is enabled/disabled. This is done to control the EMI of the current regulator output.

The ramping of the current regulator is done by ramping one LSB step of the current regulator per internal clock. Providing a “stair case” ramp of the output current. See Figure 8.

For flash mode, the output current increases in 50mA steps per 2 x t_{RAMP_STEP} from 50mA until the final value. The ramp time is defined by t_{RAMP} and is dependent on the number in LSB that is ramped.

For assist and torch modes, the output current increases in 10mA steps per t_{RAMP_STEP} from 30mA until the final value. The ramp time is defined by t_{RAMP} and is dependent on the number in LSB that is ramped.

The actual time used for ramping up and down is determined by the following equations:

For flash mode:

$$t_{RAMP\_FLASH} = t_{RAMP\_STEP} \times \Delta I_{FLASH}$$

where ΔI_{FLASH} is the delta change in output current divided by 100mA.

For torch mode:

$$t_{RAMP\_TORCH} = t_{RAMP\_STEP} \times \Delta I_{TORCH}$$

where ΔI_{TORCH} is the delta change in output current divided by 10mA. If ramping from off condition, the minimum current level should be calculated from 30mA and not 0mA, since the first step is 30mA instead of 10mA.

The ramp is activated for the following condition:

1) During initial enable of the current regulator
2) User change in output current
3) After TX_MASK event, when the output current is increased

The ramp is not active for the following conditions:

1) When output current is reduced as a result of a TX_MASK
2) During a fault condition

Flash Safety Timer

The flash safety timer is activated any time flash mode is enabled.

The flash safety timer, programmable from 1.024ms to 262.144ms through the I2C, limits the duration of the flash mode in case the flash is not disabled with FLASH_STB or I2C within the programmed flash safety timer duration. The flash mode is terminated when the timer expires.

The flash timer can operate in two different modes, one-shot time mode or maximum duration timer mode.

One-shot mode is sensitive to the edge of the FLASH_STB pin and maximum duration mode is sensitive to the level of the FLASH_STB pin.

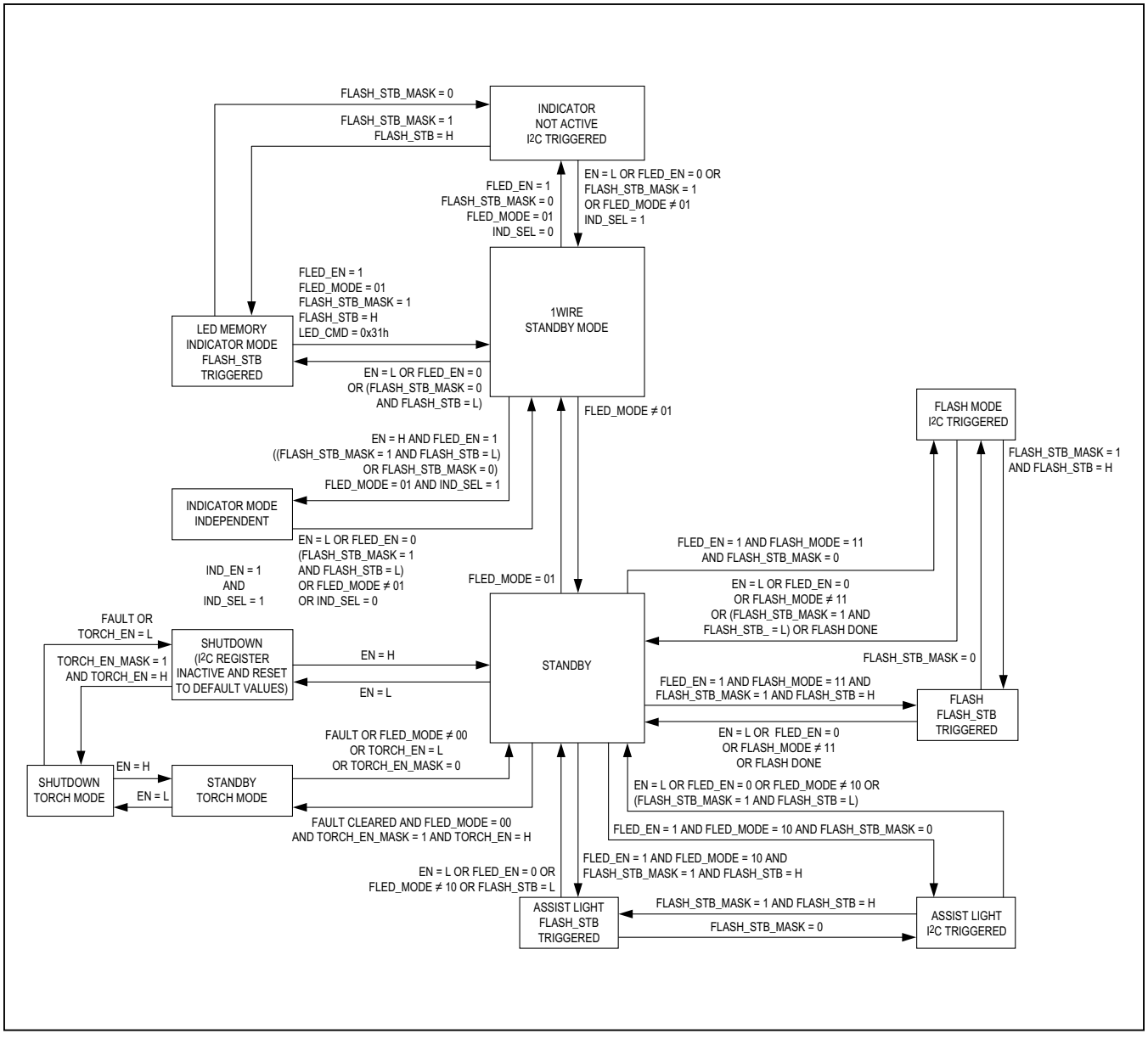


Figure 9. State Flowchart

Maximum flash timer mode can only be used for enabling flash mode using the FLASH_STB logic input. In this mode the flash is enabled for as long as the FLASH_STB logic input is logic-high and the flash timer has not expired. If the flash timer expires before the FLASH_STB is pulled low, the current regulator is disabled again and a fault condition is latched into the status register.

One-shot flash timer mode can be used with either FLASH_STB or I2C trigger flash. For I2C triggered flash, the one-shot mode is always used regardless of the FLASH_TMR setting. For one-shot mode, the flash is enabled on the rising edge of FLASH_STB or by writing to the I2C register. The duration of the flash is determined by the FLASH_TMR settings, and is terminated upon the timer expiring. For one-shot mode there is no fault condition for the flash timer.

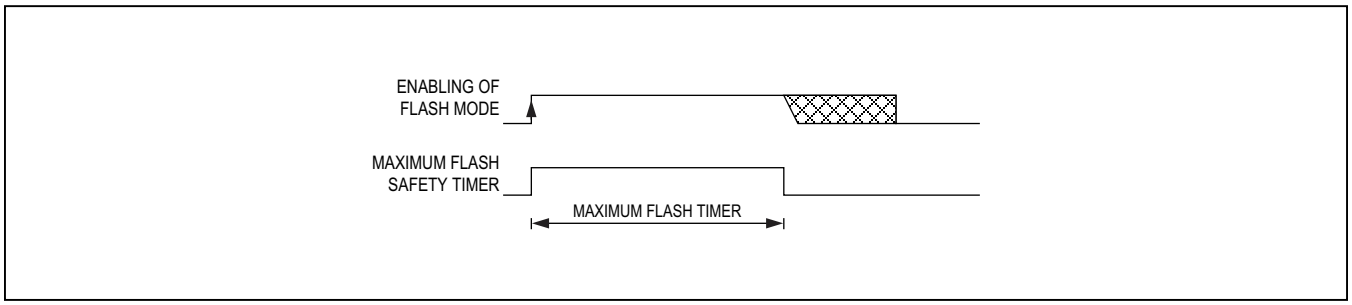


Figure 10. Maximum Flash Timer Mode

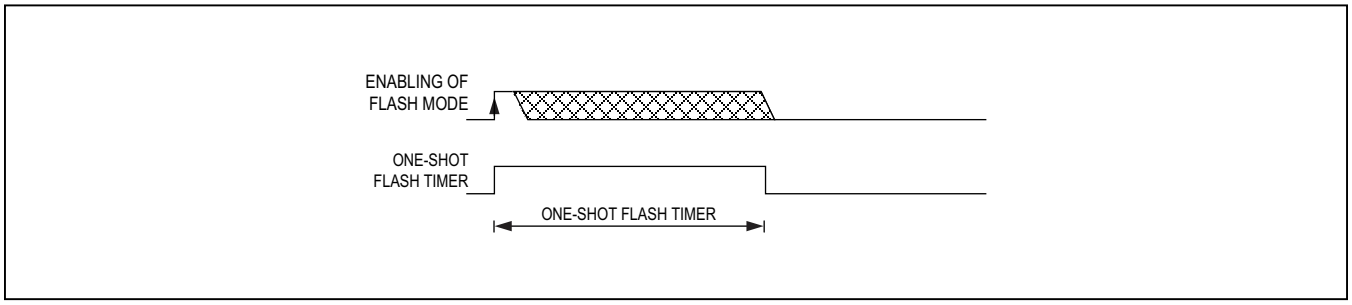


Figure 11. One-Shot Flash Timer Mode

Low Input Voltage Function

The IC monitors the input voltage before initial enable of flash mode and changes the behavior of the LED driver accordingly.

For the input, there is a monitor function that can be enabled using the LOW_VOLTAGE_EN I²C bit. When the low voltage function is enabled, it monitors the input voltage before the flash is initiated to determine the flash output current. The low voltage function is only active in flash mode.

If the input voltage drops below the user-defined threshold, LOW_VOLTAGE_TH, the flash output current is reduced by LOW_VOLTAGE_CUR. This prevents the LED driver from overloading the battery, thus preventing a system failure. See Figure 12.

TX_MASK

The IC has a logic input that can be used to provide the flash driver with the information that an RF Tx burst is in progress. During the Tx burst, the output current needs to be reduced with a predetermined current defined by the I_FLASH_TX I²C setting.

When the TX_MASK is triggered, the current is immediately reduced by the I_FLASH_TX value within 20µs (typ). The output current level then stays at this level as long as the TX_MASK condition is present. If the TX_MASK goes low while in flash mode, the output current is ramped up to normal value, using the normal ramp function.

The TX_MASK event latches a status flag in the status register, making it possible to read back if a Tx event had occurred during the flash event. See Figure 13.

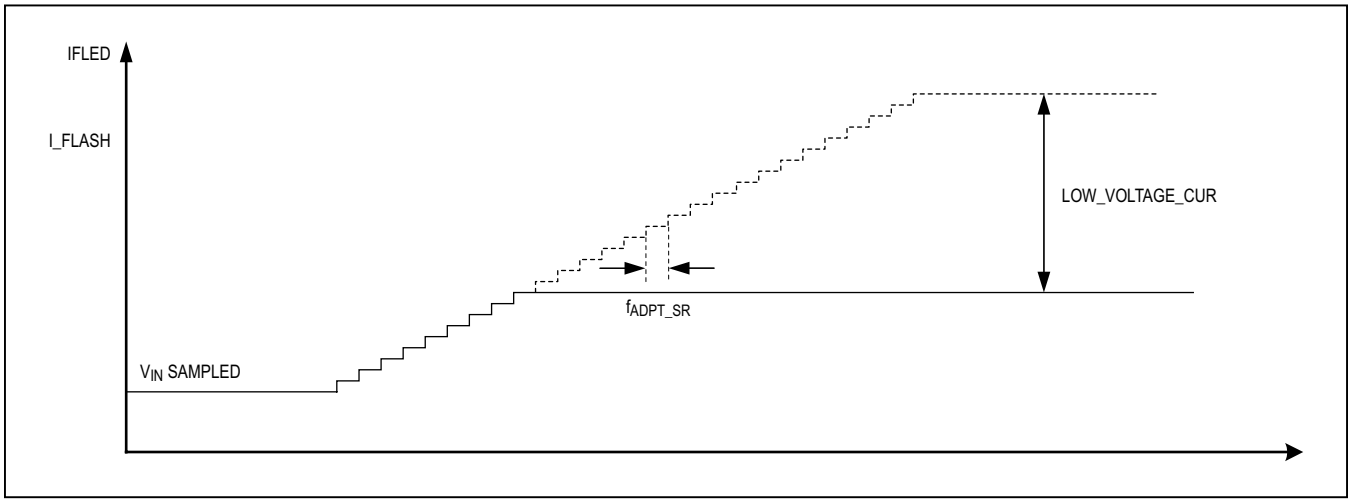


Figure 12. Low Voltage Condition

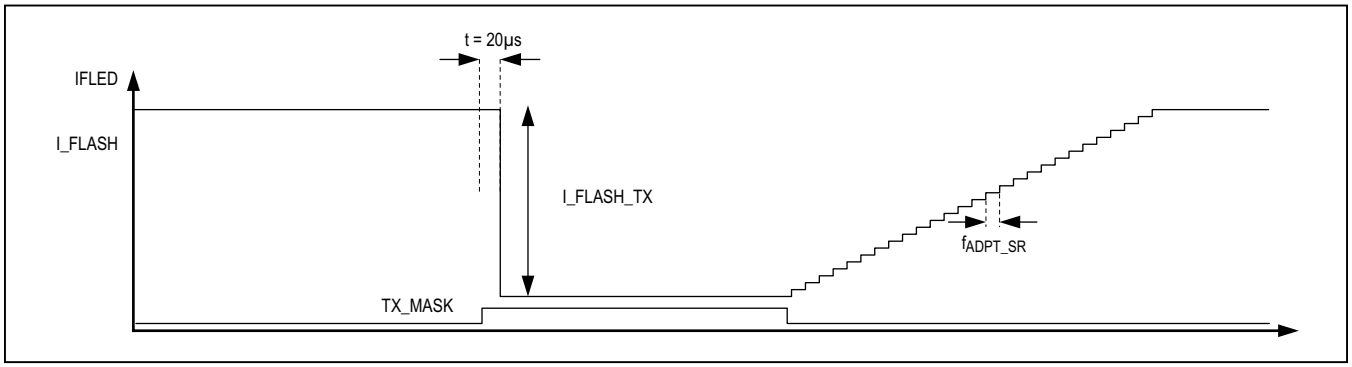


Figure 13. Flash Current During TX_MASK

Undervoltage Lockout

The device has UVLO detection that allows operation in different modes depending on the input voltage.

- V_{IN} < 1.5V (typ): the device is powered down and I²C registers are reset.
- 1.5V (typ) < V_{IN} < 2.4V (typ): I²C registers are kept intact, but remaining blocks are powered off and a fault status is latched into the status register. This is the UVLO function.
- 2.4V (typ) < V_{IN}: fully operational

Shutdown and Standby

The device is in shutdown when EN is logic-low. In power-on reset condition (V_{IN} < 1.5V typ), the I²C registers are reset to default value. In shutdown, supply current is reduced to 0.4µA (typ).

When V_{IN} is above its V_{POR} threshold and EN is pulled logic-high, the IC enters standby and is ready to accept I²C commands.

Short Detection

The device includes a comparator to detect if the FLED/IND output is shorted to ground. If the voltage level on the output of the current regulators is less than 1.0V (max), this is an indication that the FLED output is shorted to ground.

The device interprets this as a shorted output and therefore disables the current regulator, forcing the part to enter standby mode.

In the event of a shorted FLED output this event is logged into the I²C status register, where it can be read by the processor.

The short detection is enabled for assist light and torch light as soon as the output current reaches maximum current, and continues monitoring the output for short during the entire duration. For short fault in assist, torch, or flash mode, a fault is latched into the FLED_FLT bit of the I²C register.

For indicator mode, the short detection is enabled once the current regulator is enabled. If a fault is detected, a status is latched into the IND_FLT bit of the I²C register.

To resume operation after the fault, the fault must be cleared by reading the status register.

Open Detection

For assist and torch light mode, the current regulator is operating directly from the IN. Since the worst-case forward voltage for the assist/torch light LED is larger than the minimum operating input voltage, performing open LED detection is difficult to achieve without risking flash open detection, since it is required to have assist/torch light operating in dropout condition. Therefore the open detection is archived by measuring the voltage from IN to FLED. If the voltage is less than 40mV (max), the device determines that an open condition exists at the output and a fault is latched into the FLED_FLT bit of the status register.

For flash mode, an open LED forces the adaptive regulation at OVP_D and therefore a fault condition is latched.

For single-wire operation, an open detection is required since this is used to inform the single-wire interface of open/short detection. If the output voltage rises above V_{IND_OPEN}, this is an indication that the single-wire interface is not responding or the indicator LED is not correctly connected. In this case a fault is latched into the I²C bit, IND_FLT.

To resume operation after the fault, the fault must be cleared by reading.

Thermal Shutdown

Thermal shutdown limits total power dissipation in the IC. When the junction temperature exceeds 160°C (typ), the device turns off, allowing the IC to cool. In the event of an overtemperature condition occurring, the event is logged into the I²C status register, where it can be read by the processor. Once thermal shutdown occurs, the FLED_EN and IND_EN I²C bits are reset, and the IC is suspended. During a thermal shutdown condition, the only active part of the IC is the I²C interface, UVLO, and thermal monitor. All other blocks are powered down. To resume full operation after the fault, the temperature must drop by 20°C. Thermal fault must be cleared by reading before normal operation can be resumed.

I²C Serial Interface

An I²C-compatible, 2-wire serial interface controls the step-up converter output voltage, flash, torch current settings, flash duration, and other parameters. The serial bus consists of a bidirectional serial-data line (SDA) and a serial-clock input (SCL). The IC is a slave-only device, relying upon a master to generate a clock signal. The master initiates data transfer to and from the IC and generates SCL to synchronize the data transfer. See Figure 14.

I²C is an open-drain bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. They both have Schmitt triggers and filter circuits to suppress noise spikes on the bus to assure proper device operation. A bus master initiates communication with the IC as a slave device by issuing a START condition followed by the IC address. The IC address byte consists of 7 address bits and a read/write bit (R/W). After receiving the proper address, the IC issues an acknowledge bit by pulling SDA low during the ninth clock cycle.

I²C Slave Address

The IC acts as a slave transmitter/receiver. Its slave address is 0x60 for write operations and 0x61 for read operations.

I²C Bit Transfer

Each data bit, from the most significant bit to the least significant bit, is transferred one by one during each clock cycle. During data transfer, the SDA signal is allowed to change only during the low period of the SCL clock and it must remain stable during the high period of the SCL clock. See Figure 15.

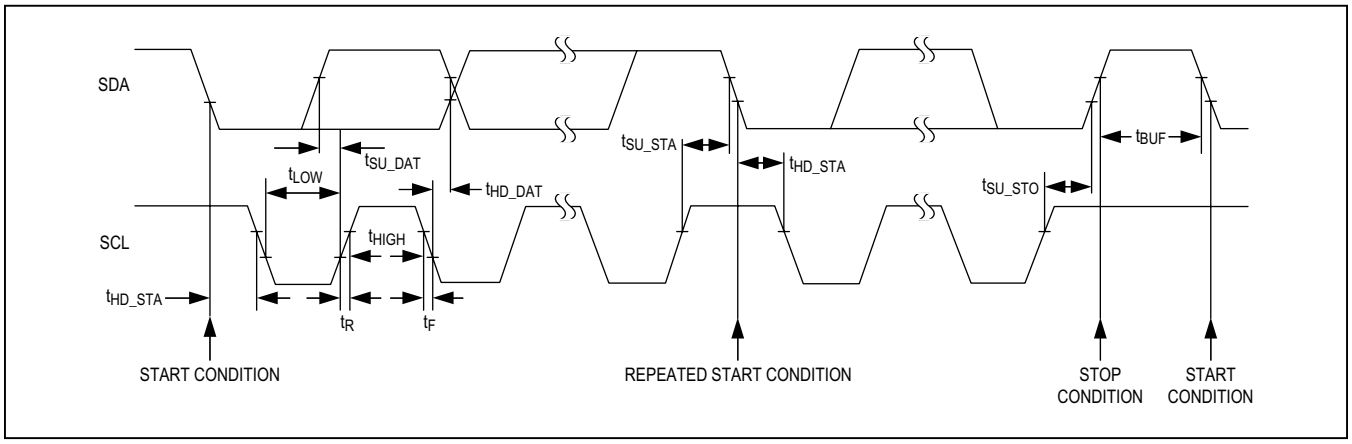


Figure 14. 2-Wire Serial Interface Timing Detail

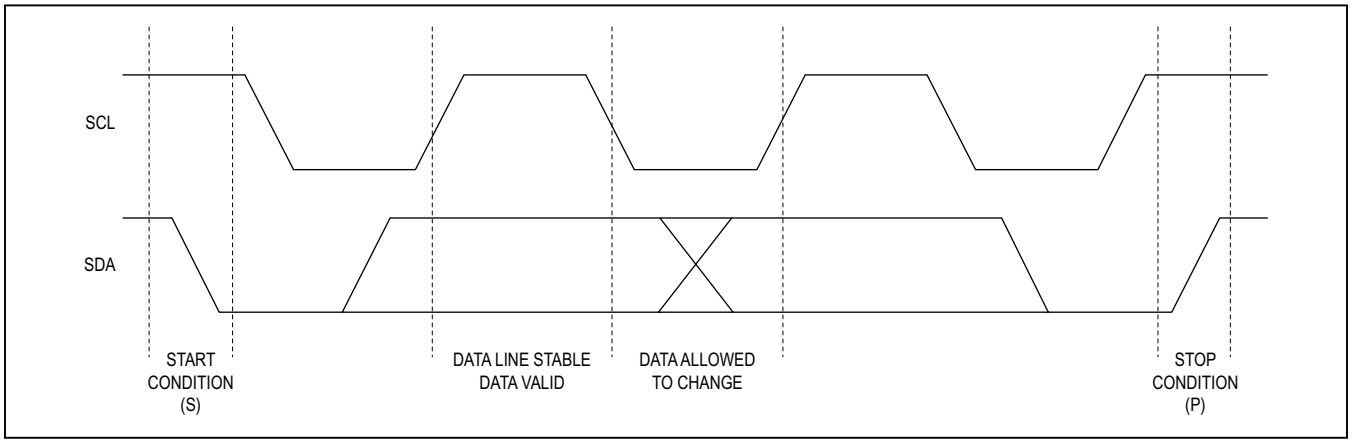


Figure 15. Bit Transfer

START and STOP Conditions

Both SCL and SDA remain high when the bus is not busy. The master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the IC, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission, Figure 16. Both START and STOP conditions are generated by the bus master.

Acknowledge

The acknowledge bit is used by the recipient to handshake the receipt of each byte of data (Figure 17). After data transfer, the master generates the acknowledge clock pulse and the recipient pulls down the SDA line during this acknowledge clock pulse so the SDA line stays low during the high duration of the clock pulse. When the master transmits the data to the IC, it releases the SDA line and the IC takes control of the SDA line and generates the acknowledge bit. When SDA remains high during this 9th clock pulse, this is defined as the not acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

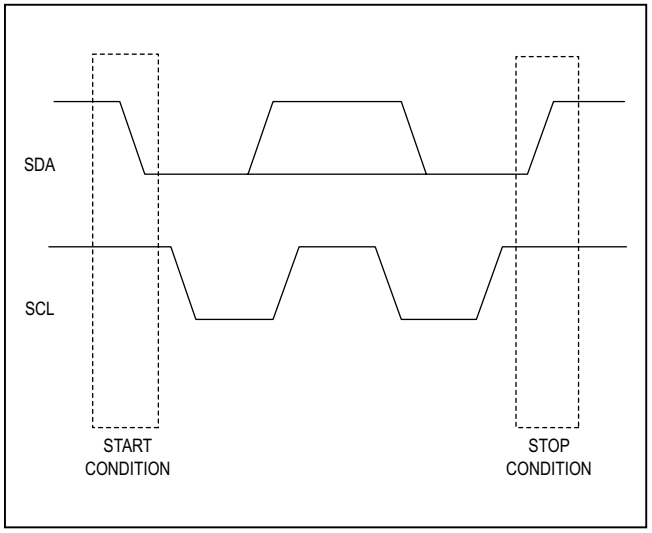


Figure 16. Start and Stop Conditions

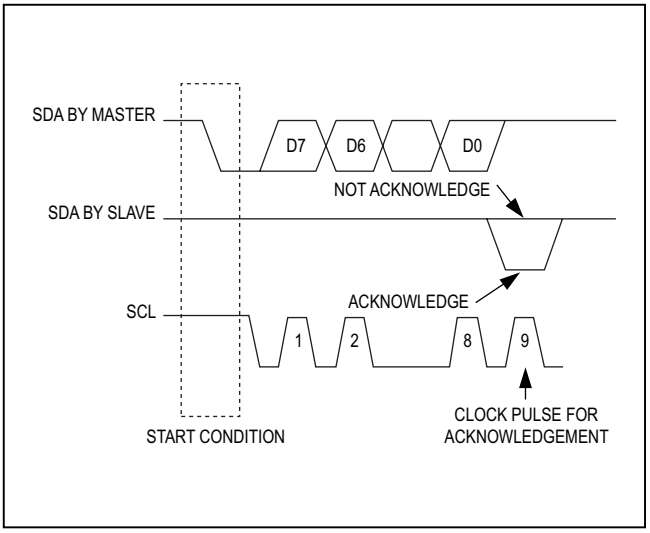


Figure 17. Acknowledge

Write Operations

The IC recognizes the write byte protocol as defined in the SMBus specification and shown in section A of Figure 18. The write byte protocol allows the I2C master device to send 1 byte of data to the slave device. The write byte protocol requires a register pointer address for the subsequent write. The IC acknowledges any register pointer even though only a subset of those registers actually exists in the device.

The write byte protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) The master sends a STOP condition.

In addition to the write-byte protocol, the IC can write to multiple registers as shown in section B of Figure 18. This protocol allows the I2C master device to address the slave only once and then send data to a sequential block of registers starting at the specified register pointer.

Use the following procedure to write to a sequential block of registers:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends the 8-bit register pointer of the first register to write.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) Steps 6 to 8 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
10) The master sends a STOP condition.

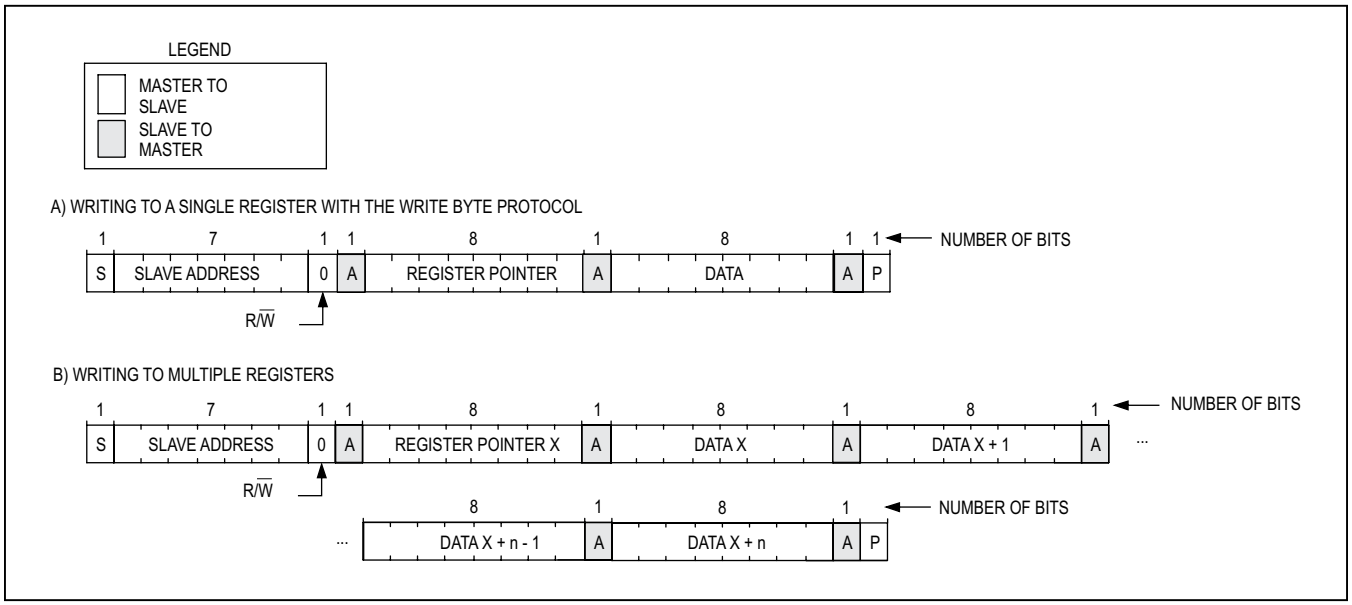


Figure 18. Write to the IC

Read Operations

The method for reading a single register (byte) is shown in section A of Figure 19. To read a single register:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated START condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave asserts an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master asserts an acknowledge by pulling SDA low.
11) The master sends a STOP condition.

In addition, the IC can read a block of multiple sequential registers as shown in section B of Figure 19. Use the following procedure to read a sequential block of registers:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer of the first register in the block.
5) The slave acknowledges the register pointer.
6) The master sends a repeated START condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave asserts an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master asserts an acknowledge by pulling SDA low.
11) Steps 9 and 10 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
12) The master sends a STOP condition.

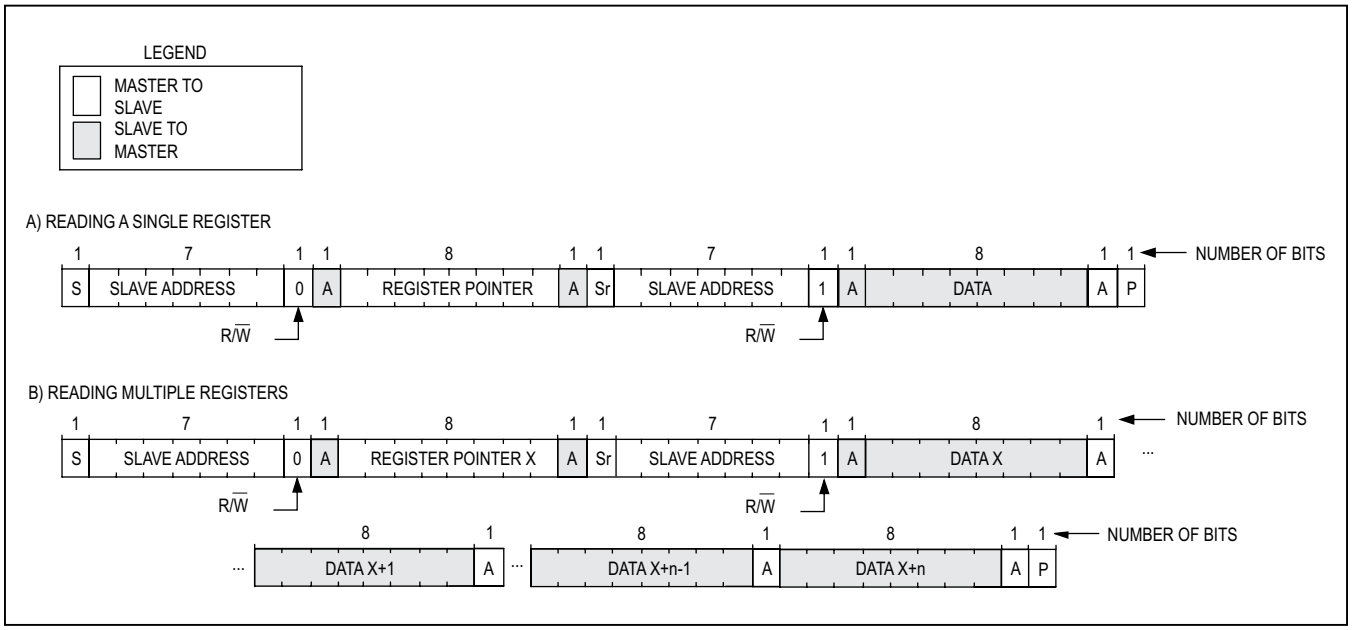


Figure 19. Read from the IC

I²C Register MAP

ADDRESS	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	CHIP_ID1	MAN_ID [3:0]				DIE_ID[3:0]			
0x01	CHIP_ID2	RESERVED	RESERVED	RESERVED	RESERVED	DIE_REV[0:3]			
0x02	ISET	RESERVED	I_TORCH[2:0]			I_FLASH[3:0]			
0x03	TX_MASK	FLASH_ STB_MASK	FLASH_ TMR_CNTL	RESERVED	DCDC_ILIM[1:0]		TORCH_ EN_MASK	IND_SEL	VSEL_STB
0x04	LOW_VOLTAGE	RESERVED	LOW_ VOLTAGE_EN	LOW_VOLTAGE_TH[2:0]			LOW_VOLTAGE_CUR[1:0]		POR
0x05	FLASH_TMR_CNTL	FLASH_TMR[0:7]							
0x06	FLED_EN	TX_MASK_EN	I_FLASH_TX[0:1]		RESERVED	RESERVED	FLED_EN	FLED_MODE[0:1]	
0x07	STATUS	OVLO	FLED_FLT	THRM	FLASH_TMR	TX_MASK	IND_FLT	LOW_ VOLTAGE _DET	UVLO
0x08	1W_STAT	RESERVED	ILIM	RESERVED	COUT_DET	—	—	—	—
0x09	RESERVED	RESERVED							
0x0A	LED_MEM_START	LED_START[7:0]							
0x0B	LED_MEM_STOP	LED_STOP[7:0]							
0x0C	IND_CTL	RESERVED	RESERVED	IND_MODE[0:1]		IND_CUR[0:3]			
0x0D	LED_MEM_CMD	LED_CMD[7:0]							
0x20	DCDC_SS	DCDC_SS[7:0]							
0x21	DCDC_OUT	DCDC_OUT[7:0]							
0x22	DCDC_MAX	DCDC_MAX[7:0]							
0x23	COUT_DET	RESERVED	RESERVED	RESERVED	RESERVED	DIS_ COUTDET	RESERVED	RESERVED	RESERVED

Table 1. CHIP_ID1

This register contains manufacturer ID and die type.

REGISTER NAME	CHIP_ID1
ADDRESS	0x00h
RESET VALUE	0x65h
TYPE	Read only
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	MAN_ID[3:0]	Manufacturer ID 0110 Maxim Integrated Products	0110
B6			
B5			
B4			
B3	DIE_ID[3:0]	Die ID 0101 (MAX77311)	0101
B2			
B1			
B0 LSB			

Table 2. CHIP_ID2

This register contains version control.

REGISTER NAME	CHIP_ID2
ADDRESS	0x01h
RESET VALUE	Depends on revision of IC
TYPE	Read only
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	—	Reserved for future use	0
B6	—	Reserved for future use	0
B5	—	Reserved for future use	0
B4	—	Reserved for future use	0
B3	DIE_REV[3:0]	Die REV 0000 Revision 1 0001 Revision 2 … … 1110 Revision 15 1111 Revision 16	—
B2			
B1			
B0 LSB			

Table 3. ISET

This register contains control for the output current in assist and flash modes.

REGISTER NAME	ISET
ADDRESS	0x2h
RESET VALUE	0x3Fh
TYPE	Read/Write
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	—	Reserved for future use	0
B6	I_TORCH[2:0]	Setting of torch and assist current 000: 30mA 001: 40mA 011: 60mA (default) 110: 90mA 111: 100mA	011
B5			
B4			
B3	I_FLASH[3:0]	Setting of flash current 0000: 100mA 0001: 200mA 1110: 1500mA 1111: 1600mA	1111
B2			
B1			
B0 LSB			

Table 4. TX_MASK

This register contains control for TX_MASK.

REGISTER NAME	TX_MASK
ADDRESS	0x3h
RESET VALUE	0xCDh
TYPE	Read/Write
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	FLASH_STB_MASK	Enable of FLASH_STB logic input 0: FLASH_STB logic input disabled 1: FLASH_STB logic input enabled	1
B6	FLASH_TMR_CNTL	Flash timer control 0: One-shot mode 1: Maximum duration mode	1
B5	—	Reserved for future use	0
B4	DCDC_ILIM[1:0]	Selects current limit for low-side switch 00: 1.4A 01: 2.1A 10: 2.5A 11: 2.9A	01
B3			
B2	TORCH_EN_MASK	Enable of TORCH_EN logic input 0: TORCH_EN logic input disabled 1: TORCH_EN logic input enabled	1
B1	IND_SEL	Select operation of single-wire current regulator 0: Do not use 1: Set to indicator function	0
B0 LSB	VSEL_STB	Voltage selection for FLASH_STB input 0: 1.2V IO 1: 1.8V IO	1

Table 5. LOW_VOLTAGE

This register contains control information for the low input voltage function.

REGISTER NAME	LOW_VOLTAGE
ADDRESS	0x04h
RESET VALUE	0x54h
TYPE	Read/Write
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	—	Reserved for future use	0
B6	LOW_VOLTAGE_EN	ON/OFF control for the low-voltage function 0: Disabled 1: Enabled	1
B5	LOW_VOLTAGE_TH[2:0]	Selects low-voltage detection threshold 000: 3.0V 001: 3.1V 110: 3.6V 111: 3.7V	010
B4			
B3			
B2	LOW_VOLTAGE_CUR[1:0]	Reduction of flash current during low-voltage event 00: 200mA 01: 400mA 10: 600mA 11: 800mA	10
B1			
B0 LSB	POR	This bit is used to reset all I^2C registers to default value 0: No action 1: Reset I^2C registers	0

Table 6. FLASH_TMR_CNTL

This register contains control information for the flash timer.

REGISTER NAME	FLASH_TMR_CNTL
ADDRESS	0x05h
RESET VALUE	0x1Fh
TYPE	Read/Write
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	FLASH_TMR[7:0]	Selecting for flash timer Flash timer = (FLASH_TMR[7:0] + 1) x 1.024ms	00011111
B6			
B5			
B4			
B3			
B2			
B1			
B0 LSB			

Table 7. FLED_EN

This register contains control information for the TX_MASK and mode of operation.

REGISTER NAME	FLED_EN
ADDRESS	0x06h
RESET VALUE	0xB0h
TYPE	Read/Write
SPECIAL FEATURES	B2 is reset upon a flash/torch event

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th><th>DEFAULT VALUE</th></tr>
<tr><td>B7 MSB</td><td>TX_MASK_EN</td><td>TX_MASK enable
0: TX_MASK input disabled
1: TX_MASK input enabled</td><td>1</td></tr>
<tr><td>B6
B5</td><td>I_FLASH_TX[1:0]</td><td>Reduction of flash current during a Tx event
00: 200mA
01: 400mA
10: 600mA
11: 800mA</td><td>01</td></tr>
<tr><td>B4</td><td>—</td><td>Reserved for future use</td><td>1</td></tr>
<tr><td>B3</td><td>—</td><td>Reserved for future use</td><td>0</td></tr>
<tr><td>B2</td><td>FLED_EN</td><td>Enable of FLED
0: FLED current regulator always disable regardless of other settings
1: FLED current regulator is controlled the following way
<table>
<tr><th>FLED_MODE</th><th>TORCH_EN_MASK = 0</th><th>TORCH_EN_MASK = 1</th></tr>
<tr><td>00</td><td>Enabled</td><td>Enabled using TORCH_EN</td></tr>
<tr><td></td><td>FLASH_STB_MASK = 0</td><td>FLASH_STB_MASK = 1</td></tr>
<tr><td>01</td><td>Enabled</td><td>Enabled using FLASH_STB</td></tr>
<tr><td>10</td><td>Enabled</td><td>Enabled using FLASH_STB</td></tr>
<tr><td>11</td><td>Enabled</td><td>Enabled using FLASH_STB</td></tr>
</table></td><td>0</td></tr>
<tr><td>B1
B0 LSB</td><td>FLED_MODE[1:0]</td><td>Mode of operation for FLED
00: TORCH mode
01: Indicator mode
10: Assist light mode
11: Flash light mode</td><td>00</td></tr>
</table>

Table 8. STATUS

This register contains the status of the MAX77342.

REGISTER NAME	STATUS
ADDRESS	0x07h
RESET VALUE	0x00h
TYPE	Read
SPECIAL FEATURES	Reset upon read operation and power-on reset

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	OVLO	Indication that IC has been in an OVLO condition 0: OVLO has not occurred 1: OVLO has occurred Needs to be read before a new event can be executed	0
B6	FLED_FLT	FLED current regulator output status 0: No fault detected 1: Open or shorted LED detected for assist, torch, or flash modes Needs to be read before a new event can be executed	0
B5	THERM	Temperature fault indication 0: No temperature fault has occurred 1: Temperature fault has occurred Needs to be read before a new event can be executed	0
B4	FLASH_TMR	Indication of flash timer (only valid when operating in maximum timer mode) 0: Flash timer did not expire during last flash sequence 1: Flash timer expired during last flash sequence Reset upon read or trigger of flash event	0
B3	TX_MASK	Indication of TX_MASK 0: TX_MASK has not occurred during last flash event 1: TX_MASK has occurred during last flash event Reset upon read or trigger of flash event	0
B2	IND_FLT	IND current regulator output status 0: No fault detected 1: Fault detected (OPEN/SHORT) Needs to be read before a new event can be executed	0
B1	LOW_VOLTAGE_DET	Indication of status of low input voltage detection 0: Low voltage condition has not occurred during the last flash event 1: Low voltage condition has occurred before the last flash event Reset upon read or trigger of flash event	0
B0 LSB	UVLO	Indication that the device has been in UVLO or EN low condition since last read operation 0: IN has been within operating range at all times 1: IN has dropped below the undervoltage lockout trip point. Reset upon read or trigger of assist, torch, or flash event	0

Table 9. 1W_STAT

This register contains the status for 1WIRE.

REGISTER NAME	1W_STAT
ADDRESS	0x08h
RESET VALUE	0x00h
TYPE	Read
SPECIAL FEATURES	Reset upon read operation and power-on reset

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	—	Reserved for future use	0
B6	ILIM	Peak input current limiter triggered 0: Input current below peak input current limit 1: Peak input current exceeding limit	0
B5	—	Reserved for future use	0
B4	COUT_DET	Status of COUT detection 0: COUT detected 1: Error in C_{OUT} detection Needs to be read before a new event can be executed	0

Table 10. 1W_IND_CNTL

This register contains the byte to be written in indicator mode for single-wire interface.

REGISTER NAME	1W_IND_CNTL
ADDRESS	0x0Ch
RESET VALUE	0x00h
TYPE	Read/write
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION		DEFAULT VALUE
B7 MSB	—	Reserved		0
B6	—	Reserved		0
B5	—	Reserved		00
B4				
B3	IND_CUR[3:0]		**Indicator current for IND_SEL = 0 (single-wire current) (mA)**	000
		0000	1	
B2		0001	2	
		…	…	
		1010	11	
B1		1011	12	
		1100	13	
		1101	14	
B0 LSB		1110	15	
		1111	16	

Table 11. DCDC_SS

This register contains control information for the DC-DC converter.

REGISTER NAME	DCDC_SS
ADDRESS	0x20h
RESET VALUE	0x64h
TYPE	Read/write
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	DCDC_SS[7:0]	Set the soft-start threshold for the DC-DC converter 00000000: 2.6V 00000001: 2.611V 01100100: 3.6V 11111111: 5.15V	01100100
B6			
B5			
B4			
B3			
B2			
B1			
B0 LSB			

Table 12. DCDC_OUT

This register contains control information about the actual regulation output voltage for the DC-DC converter during adaptive regulation.

REGISTER NAME	DCDC_OUT
ADDRESS	0x21h
RESET VALUE	0x84h
TYPE	Read only
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	DCDC_OUT[7:0]	Read-back information regarding adaptive regulation output voltage 00000000: 2.6V 00000001: 2.61V 11111110: 5.14V 11111111: 5.15V	10000100
B6			
B5			
B4			
B3			
B2			
B1			
B0 LSB			

Table 13. DCDC_OUT_MAX

This register contains control information about the actual maximum output voltage for the DC-DC converter during adaptive regulation.

REGISTER NAME	DCDC_OUT_MAX
ADDRESS	0x22h
RESET VALUE	0x00h
TYPE	Read only
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	DCDC_OUT_MAX[7:0]	Read-back information regarding maximum adaptive regulation output voltage 00000000: 2.6V 00000001: 2.61V 11111110: 5.14V 11111111: 5.15V	00000000
B6			
B5			
B4			
B3			
B2			
B1			
B0 LSB			

Table 14. COUT_DET

This register contains control information about COUT_DET.

REGISTER NAME	COUT_DET
ADDRESS	0x23h
RESET VALUE	0x08h
TYPE	Read/Write
SPECIAL FEATURES	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 MSB	—	Reserved for future use.	0
B6	—	Reserved for future use.	0
B5	—	Reserved for future use.	0
B4	—	Reserved for future use.	0
B3	DIS_COUTDET	Disable of COUT_DET function 0: Enable COUT detection function 1: Disable COUT detection function	1
B2	—	Reserved for future use.	0
B1	—	Reserved for future use.	0
B0 LSB	—	Reserved for future use.	0

Table 15. Maximum Output Current Capability of DC-DC Step-Up Converter ($L = 1\mu H$, $V_{OUT} = 4.2V$, $f_{SW} = 4MHz$)

V_{IN} (V)	I_{PEAK} (A) (DCDC_ILIM[1:0])			
	00 **1.4 (typ)**	**01** **2.1 (typ)**	**10** **2.5 (typ)**	**11** **2.9 (typ)**
2.50	0.5	0.9	1.1	1.3
2.60	0.5	0.9	1.1	1.4
2.70	0.6	1.0	1.2	1.4
2.80	0.6	1.0	1.2	1.5
2.90	0.6	1.0	1.3	1.5
3.00	0.6	1.1	1.4	1.6
3.10	0.6	1.1	1.4	1.6
3.20	0.7	1.2	1.4	1.6
3.30	0.7	1.2	1.5	1.6
3.40	0.7	1.2	1.5	1.6
3.50	0.7	1.3	1.6	1.6
3.60	0.7	1.3	1.6	1.6
3.70	0.7	1.3	1.6	1.6
3.80	0.7	1.4	1.6	1.6
3.90	0.8	1.4	1.6	1.6
4.00	0.8	1.4	1.6	1.6
4.10	0.8	1.4	1.6	1.6
4.20	0.8	1.5	1.6	1.6
4.30	0.8	1.5	1.6	1.6
4.40	0.8	1.5	1.6	1.6
4.50	0.8	1.5	1.6	1.6

Table 16. Maximum Output Current Capability of DC-DC Step-Up Converter ($L = 1\mu H$, $V_{IN} = 2.7V$, $f_{SW} = 4MHz$)

V_{OUT} (V)	I_{PEAK} (A) (DCDC_ILIM[1:0])			
	00 **1.4 (typ)**	**01** **2.1 (typ)**	**10** **2.5 (typ)**	**11** **2.9 (typ)**
3.00	1.0	1.6	1.6	1.6
3.20	0.9	1.6	1.6	1.6
3.40	0.9	1.6	1.6	1.6
3.60	0.8	1.5	1.6	1.6
3.80	0.8	1.4	1.6	1.6
4.00	0.7	1.4	1.6	1.6
4.20	0.7	1.3	1.6	1.6

Applications Information

Inductor Selection

The device is designed to use a 1µH inductor. To prevent core saturation, ensure that the inductor-saturation current rating exceeds the peak inductor current for the application. Calculate the worst-case peak inductor current with the following formula:

$$I_{PEAK} = \frac{V_{OUT} \times I_{OUT(MAX)}}{0.9 \times V_{IN(MIN)}} + \frac{V_{IN(MIN)}}{2 \times \pi \times L \times f_{SW}}$$

If the saturation current in the inductor is lower than the peak current of the application, the effective inductance starts to reduce, resulting in increased ripple current. Since the ripple current also affects the output voltage ripple, this impacts the performance of the device. The key area impacted is the output ripple current of the FLED output.

Table 17 shows a list of recommended inductors for the device; the final choice of the inductor is dependent on the operating condition of the application.

Input Capacitor Selection

The input capacitor required consists of two capacitors; one capacitor for decoupling the input to IN, the other is for decoupling the inductor to reduce input ripple.

The input capacitor is a 100nF ceramic capacitor. This capacitor is required to ensure a low-noise input to IN. This is critical for operation of functions like low voltage detection and current accuracy.

The input capacitor for the inductor is required to support the ripple current from the DC-DC converter switching. The input capacitor needs to be a 10µF or larger ceramic capacitor.

Output Capacitor Selection

The output capacitor is one of the critical items in determining the output ripple current of the FLED output. The output ripple is generated from the voltage ripple existing on the OUT, due to DC-DC step-up converter switching. The output ripple consists of two main components: the ESR of the output capacitor and the ΔV across the output capacitor caused by the charge and discharge cycle.

The choice of output capacitor is critical for the ripple current. To ensure low output ripple current two actions can be taken:

1) Select an output capacitor with a low ESR.
2) In PCB layout, careful routing between IC and output capacitor can reduce ripple current.

The recommended output capacitance is 2 x 10µF with a low ESR (2 x 10µF is recommended as opposed to 1 x 22µF so a lower ESR is achieved and to ensure low output ripple). Increasing the output capacitance reduces the output ripple current of the FLED output.

Table 17. Suggested Inductor

MANUFACTURER	SERIES	INDUCTANCE (µH)	DCR (mΩ)	I_{SAT} (A)	DIMENSIONS L_{TYP} x W_{TYP} x H_{MAX} (mm)
Samsung	CIG32K1R0SAE	1.0	60	2.7	3.2 x 2.5 x 1
Coilcraft	LPS4012-102ML	1.0	60	2.8	4 x 4 x 1.1
Taiyo Yuden	NR03SB1R0N	1.0	27	2.6	4 x 4 x 1.8
	BRL3225T1R0M	1.0	51.6	2.4	3.2 x 2.5 x 1.7
TOKO	DFE252012C	1.0	65	2.5	2.5 x 2.0 x 1.2
	DEM2818C	1.0	29	2.3	2.8 x 3 x 1.8

Table 18. Suggested Output Capacitors

MANUFACTURER	SERIES	CAPACITANCE (µF)	DIMENSIONS (L_{TYP} x W_{TYP} x H_{MAX} = Volume) (mm)
Murata	GRM188R60J126	10	1.6 x 0.8 x 0.85
	GRM155R61C104K	0.1	1.0 x 0.5 x 0.55
Taiyo Yuden	LMK105B7104K	0.1	1.0 x 0.5 x 0.55
TDK	C1005X7R1A104K	0.1	1.0 x 0.5 x 0.55

PCB Layout

Layout is critical for the performance of the device. Proper layout ensures good thermal conditions for the IC as well as minimizing EMI disturbances.

Bypass IN to ground with a ceramic capacitor. Ceramic capacitors with X5R and X7R dielectrics are recommended for their low ESR and tighter tolerances over a wide temperature range. Place the capacitor as close as possible to the IC. The recommended minimum value for the input capacitor is 100nF placed near the IC with an additional capacitor of 10µF to PGND near the inductor; however, larger value capacitors can be used to reduce input ripple at the expense of size and higher cost.

Bypass OUT to PGND with a ceramic capacitor. Ceramic capacitors with X5R and X7R dielectrics are recommended for their low ESR and tighter tolerances over a wide temperature range. Place the capacitor as close as possible to the IC. The recommended minimum value for the output capacitor is 4µF (derated; value at DC bias equal to V_{OUT}); however, larger value capacitors can be used to reduce output ripple at the expense of size and higher cost. To achieve low ripple current (15mA$_{P-P}$) use 2 x 10µF ceramic capacitors. Connect the IN_FLED as close as possible to the output capacitor, to achieve the lower output current ripple, IN_FLED and OUT must be kelvin connected to the output capacitor. Sharing trace between OUT/IN_FLED to the output capacitor increases the voltage ripple on the input of the current regulator, hence increases the output ripple current.

Keep the ground loop between the input, output, and the device as short as possible, since this ground plane is carrying the full load current. Keep the connection between the LX and inductor as short as possible. Keep the LX trace away from noise-sensitive traces.

The trace from FLED to the anode of the LED can be longer, but keeping this trace low impedance is critical for the efficiency of the applications as well as getting heat transferred away from the device.

Place as much ground as possible around the device since this enhances the thermal properties of the device. Refer to the layout in the MAX77342 EV kit data sheet.

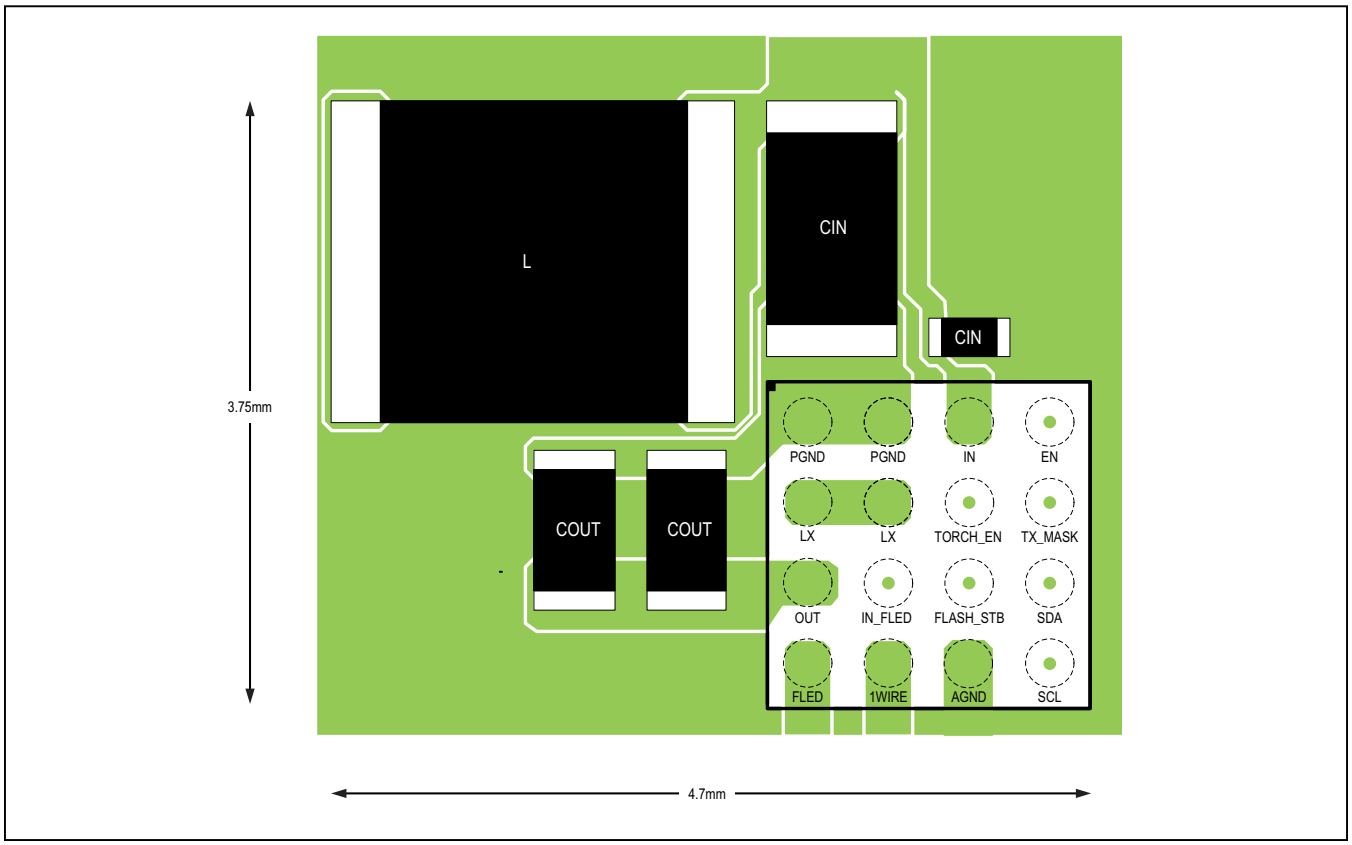


Figure 20. Recommended PCB Layout

Ordering Information

PART	TEMP RANGE	BUMP-PACKAGE
MAX77342EWE+T	-40°C to +85°C	16 WLP (2.065mm x 2.065mm)

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

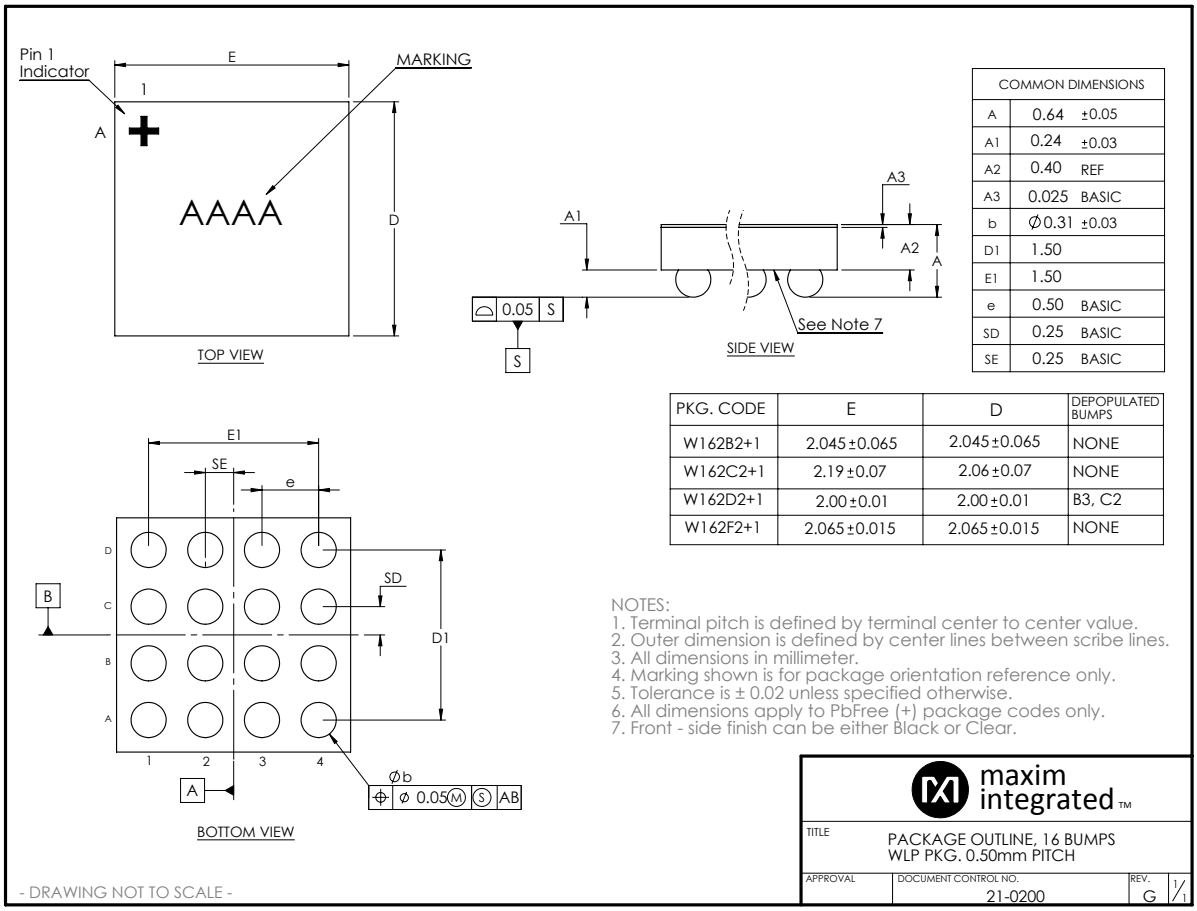
Chip Information

PROCESS: BiCMOS 180nm

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W162F2+1	21-0200	—



COMMON DIMENSIONS		
A	0.64	±0.05
A1	0.24	±0.03
A2	0.40	REF
A3	0.025	BASIC
b	Ø0.31	±0.03
D1	1.50	
E1	1.50	
e	0.50	BASIC
SD	0.25	BASIC
SE	0.25	BASIC

PKG. CODE	E	D	DEPOPULATED BUMPS
W162B2+1	2.045±0.065	2.045±0.065	NONE
W162C2+1	2.19±0.07	2.06±0.07	NONE
W162D2+1	2.00±0.01	2.00±0.01	B3, C2
W162F2+1	2.065±0.015	2.065±0.015	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

maxim integrated™

TITLE: PACKAGE OUTLINE, 16 BUMPS WLP PKG. 0.50mm PITCH

APPROVAL | DOCUMENT CONTROL NO. 21-0200 | REV. G | 1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/13	Initial release	—

