SLOS406A – FEBRUARY 2003 – REVISED MARCH 2003

3-W STEREO CLASS-D AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

FEATURES

- **3-W/Ch Into an 8-Ω Load From 12-V Supply**
- **Efficient, Class-D Operation Eliminates Heatsinks and Reduces Power Supply Requirements**
- **32-Step DC Volume Control From –40 dB to 36 dB**
- **Third Generation Modulation Techniques**
  - **Replaces Large LC Filter With Small Low-Cost Ferrite Bead Filter**
- **Thermal and Short-Circuit Protection**

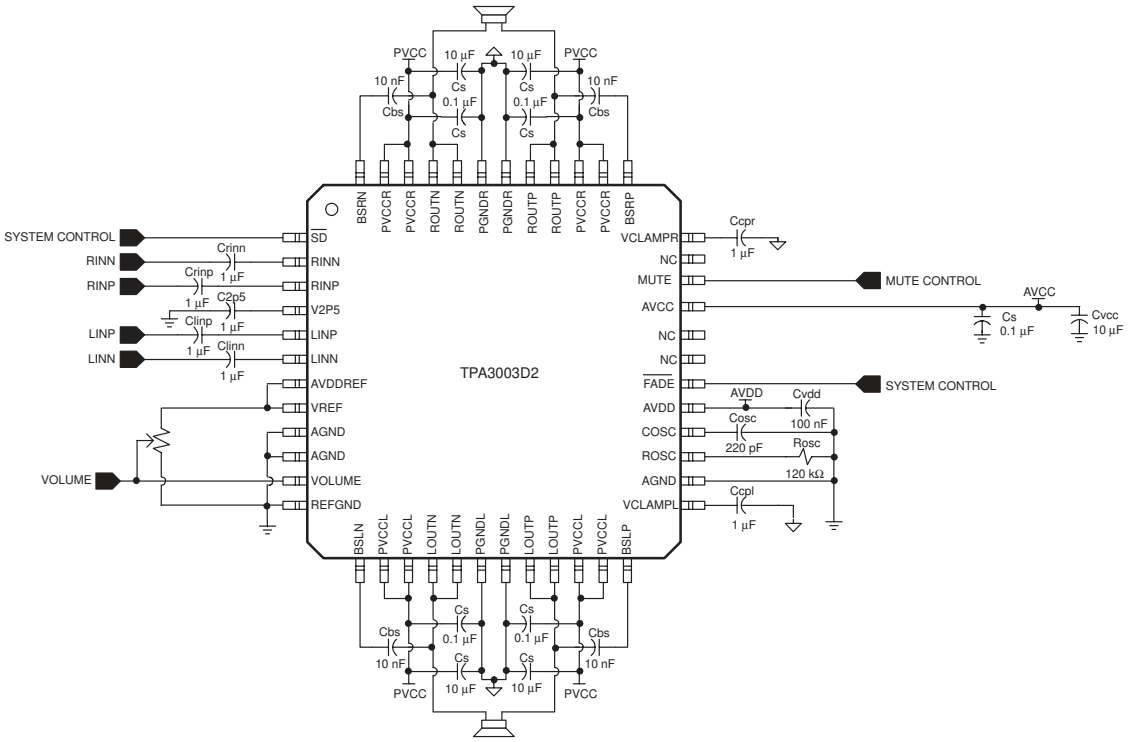
APPLICATIONS

- **LCD Monitors and TVs**
- **Powered Speakers**

DESCRIPTION

The TPA3003D2 is a 3-W (per channel) efficient, Class-D audio amplifier for driving bridged-tied stereo speakers. The TPA3003D2 can drive stereo speakers as low as 8 Ω. The high efficiency of the TPA3003D2 eliminates the need for external heatsinks when playing music.

Stereo speaker volume is controlled with a dc voltage applied to the volume control terminal offering a range of gain from –40 dB to 36 dB.



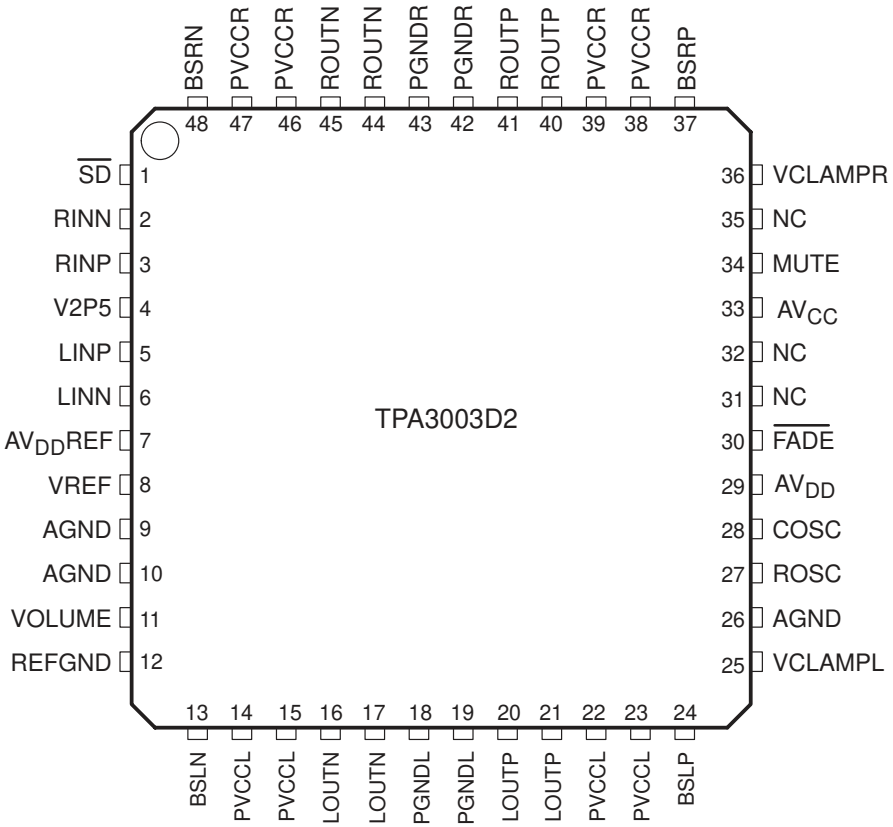
AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	48-PIN TQFP (PFB)†
–40°C to 85°C	TPA3003D2PFB

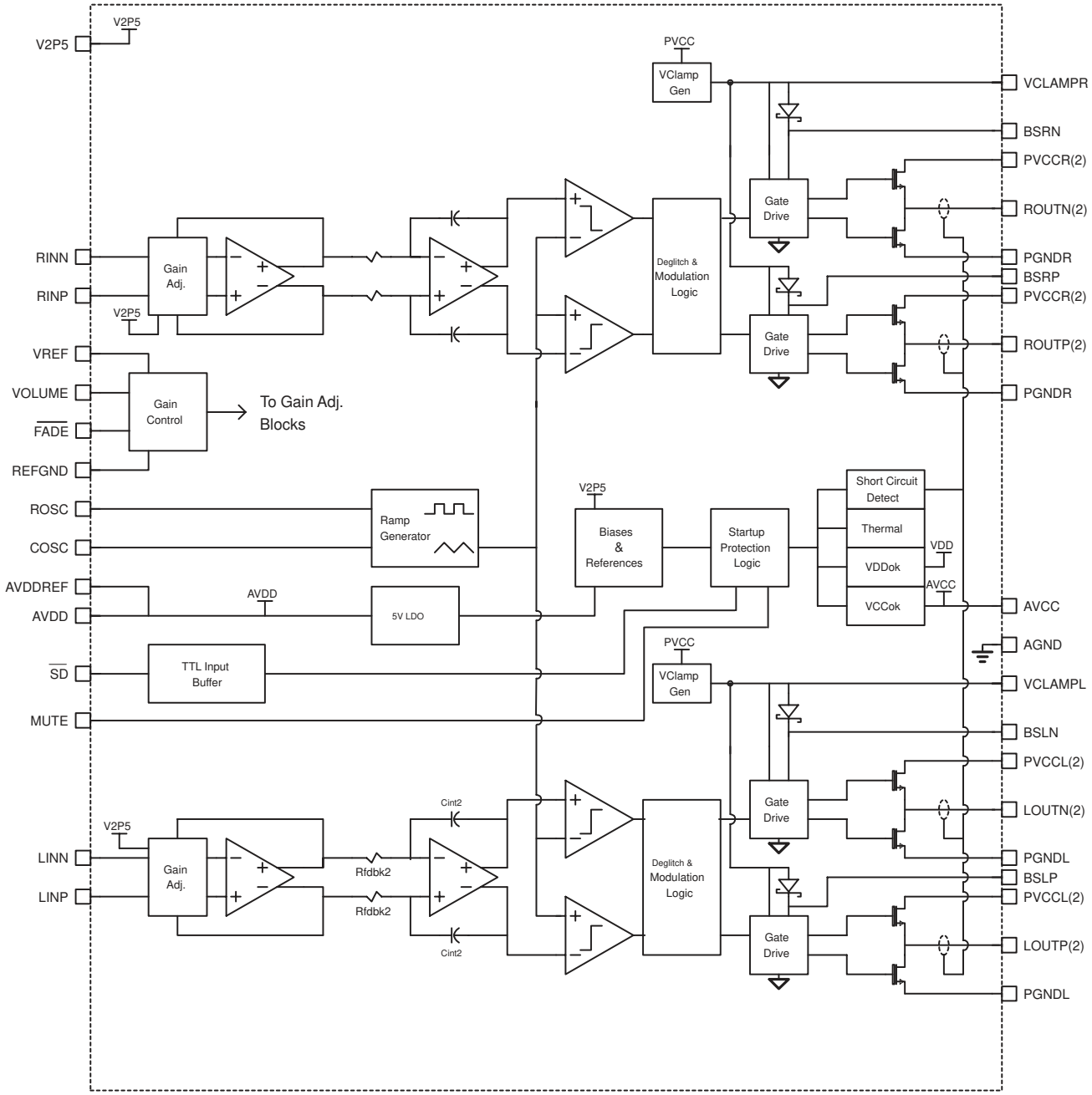
† The PFB package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA3003D2PFBR).

PHP PACKAGE

(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NO.	TERMINAL NAME	I/O	DESCRIPTION
AGND	9, 10, 26	–	Analog ground for digital/analog cells in core
AV_{CC}	33	–	High-voltage analog power supply (8.5 V to 14 V)
AV_{DD}	29	O	5-V Regulated output
AV_{DD}REF	7	O	5-V Reference output—provided for connection to adjacent VREF terminal.
BSLN	13	I/O	Bootstrap I/O for left channel, negative high-side FET
BSLP	24	I/O	Bootstrap I/O for left channel, positive high-side FET
BSRN	48	I/O	Bootstrap I/O for right channel, negative high-side FET
BSRP	37	I/O	Bootstrap I/O for right channel, positive high-side FET
COSC	28	I/O	I/O for charge/discharging currents onto capacitor for ramp generator triangle wave biased at V2P5
$\overline{\text{FADE}}$	30	I	Input for controlling volume ramp rate when cycling $\overline{\text{SD}}$ or during power-up. A logic low on this pin places the amplifier in fade mode. A logic high on this pin allows a quick transition to the desired volume setting.
LINN	6	I	Negative differential audio input for left channel
LINP	5	I	Positive differential audio input for left channel
LOUTN	16, 17	O	Class-D 1/2-H-bridge negative output for left channel
LOUTP	20, 21	O	Class-D 1/2-H-bridge positive output for left channel
MUTE	34	I	A logic high on this pin disables the outputs. A low on this pin enables the outputs.
NC	31, 32, 35	–	Not internally connected
PGNDL	18, 19	–	Power ground for left channel H-bridge
PGNDR	42, 43	–	Power ground for right channel H-bridge
PVCCL	14, 15	–	Power supply for left channel H-bridge (tied to pins 22 and 23 internally), not connected to PVCCR or AV_{CC}.
PVCCL	22, 23	–	Power supply for left channel H-bridge (tied to pins 14 and 15 internally), not connected to PVCCR or AV_{CC}.
PVCCR	38,39	–	Power supply for right channel H-bridge (tied to pins 46 and 47 internally), not connected to PVCCL or AV_{CC}.
PVCCR	46, 47	–	Power supply for right channel H-bridge (tied to pins 38 and 39 internally), not connected to PVCCL or AV_{CC}.
REFGND	12	–	Ground for gain control circuitry. Connect to AGND. If using a DAC to control the volume, connect the DAC ground to this terminal.
RINP	3	I	Positive differential audio input for right channel
RINN	2	I	Negative differential audio input for right channel
ROSC	27	I/O	Current setting resistor for ramp generator. Nominally equal to $1/8*V_{CC}$
ROUTN	44, 45	O	Class-D 1/2-H-bridge negative output for right channel
ROUTP	40, 41	O	Class-D 1/2-H-bridge positive output for right channel
$\overline{\text{SD}}$	1	I	Shutdown signal for IC (low = shutdown, high = operational). TTL logic levels with compliance to V_{CC}.
VCLAMPL	25	–	Internally generated voltage supply for left channel bootstrap capacitors.
VCLAMPR	36	–	Internally generated voltage supply for right channel bootstrap capacitors.
VOLUME	11	I	DC voltage that sets the gain of the amplifier.
VREF	8	I	Analog reference for gain control section.
V2P5	4	O	2.5-V Reference for analog cells, as well as reference for unused audio input when using single-ended inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: AV_{CC}, PV_{CC} . . . . . –0.3 V to 15 V
Input voltage range, V_I: MUTE, VREF, VOLUME, $\overline{FADE}$ . . . . . 0 V to 5.5 V
$\overline{SD}$ . . . . . –0.3 V to V_{CC} + 0.3 V
RINN, RINP, LINN, LINP . . . . . –0.3 V to 7 V
Supply current, AV_{DD} . . . . . 10 mA
AVDDREF . . . . . 10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Operating junction temperature range, T_J . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PFB	2.8 W	22.2 mW/°C	1.8 W	1.4 W

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}	8.5	14	V
Volume reference voltage	VREF	3.0	5.5	V
Volume control pins, input voltage	VOLUME		5.5	V
High-level input voltage, V_{IH}	$\overline{SD}$	2		V
	MUTE	3.5		
	$\overline{FADE}$	4		
Low-level input voltage, V_{IL}	$\overline{SD}$		0.8	V
	MUTE		2	
	$\overline{FADE}$		2	
High-level input current, I_{IH}	MUTE, V_I= 5 V, V_{CC} = 14 V		1	μA
	$\overline{SD}$, V_I= 14 V, V_{CC} = 14 V		50	
	$\overline{FADE}$, V_I= 5 V, V_{CC} = 14 V		150	
Low-level input current, I_{IL}	MUTE, $\overline{SD}$, $\overline{FADE}$, V_I= 0 V, V_{CC} = 14 V		1	μA
Oscillator frequency, f_{OSC}		225	275	kHz
Operating free-air temperature, T_A		–40	85	°C

dc characteristics, T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)	INN and INP connected together, Gain = 36 dB			10	65	mV
V2P5 (terminal 4)	2.5-V Bias voltage	No load		0.45x AV_{DD}	0.5x AV_{DD}	0.55x AV_{DD}	V
PSRR	Power supply rejection ratio	V_{CC} = 11.5 V to 12.5 V			–80		dB
I_{CC}	Supply quiescent current	MUTE = 2 V, $\overline{SD}$ = 2 V			16	28.5	mA
$I_{CC(MUTE)}$	MUTE mode quiescent current	MUTE = 3.5 V, $\overline{SD}$ = 2 V			7	9	mA
$I_{CC(max\ power)}$	Supply current at max power	R_L = 8 Ω, P_O = 3 W			0.6		A
$I_{CC(SD)}$	Supply current in shutdown mode	$\overline{SD}$ = 0.8 V			1	10	μA
$r_{ds(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 1 A, T_J = 25°C	High side		600	700	mΩ
			Low side		600	700	
			Total		1200	1400	

ac characteristics, T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
k_{SVR}	Supply ripple rejection ratio	V_{CC} = 11.5 V to 12.5 V from 10 Hz to 1 kHz, Gain = 36 dB		–67		dB
$P_{O(max)}$	Maximum continuous output power	THD+N = 1%, f = 1 kHz, R_L = 8 Ω		3		W
		THD+N = 10%, f = 1 kHz, R_L = 8 Ω		3.75		W
V_n	Output integrated noise floor	20 Hz to 22 kHz, No weighting filter, Gain = 0.5 dB		–82		dBV
	Crosstalk, Left → Right	Gain = 13.2 dB, P_O = 1 W, R_L = 8 Ω		–77		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 0.5%, f= 1 kHz, Gain = 0.5 dB		102		dB
	Thermal trip point			150		°C
	Thermal hystersis			20		°C

Table 1. DC Volume Control

VOLTAGE ON THE VOLUME PIN AS A PERCENTAGE OF VREF (INCREASING VOLUME OR FIXED GAIN)	VOLTAGE ON THE VOLUME PIN AS A PERCENTAGE OF VREF (DECREASING VOLUME)	GAIN OF AMPLIFIER
%	%	dB
0 – 4.5	0 – 2.9	–75†
4.5 – 6.7	2.9 – 5.1	–40.0
6.7 – 8.91	5.1 – 7.2	–37.5
8.9 – 11.1	7.2 – 9.4	–35.0
11.1 – 13.3	9.4 – 11.6	–32.4
13.3 – 15.5	11.6 – 13.8	–29.9
15.5 – 17.7	13.8 – 16.0	–27.4
17.7 – 19.9	16.0 – 18.2	–24.8
19.9 – 22.1	18.2 – 20.4	–22.3
22.1 – 24.3	20.4 – 22.6	–19.8
24.3 – 26.5	22.6 – 24.8	–17.2
26.5 – 28.7	24.8 – 27.0	–14.7
28.7 – 30.9	27.0 – 29.1	–12.2
30.9 – 33.1	29.1 – 31.3	–9.6
33.1 – 35.3	31.3 – 33.5	–7.1
35.3 – 37.5	33.5 – 35.7	–4.6
37.5 – 39.7	35.7 – 37.9	–2.0
39.7 – 41.9	37.9 – 40.1	0.5†
41.9 – 44.1	40.1 – 42.3	3.1
44.1 – 46.4	42.3 – 44.5	5.6
46.4 – 48.6	44.5 – 46.7	8.1
48.6 – 50.8	46.7 – 48.9	10.7
50.8 – 53.0	48.9 – 51.0	13.2
53.0 – 55.2	51.0 – 53.2	15.7
55.2 – 57.4	53.2 – 55.4	18.3
57.4 – 59.6	55.4 – 57.6	20.8
59.6 – 61.8	57.6 – 59.8	23.3
61.8 – 64.0	59.8 – 62.0	25.9
64.0 – 66.2	62.0 – 64.2	28.4
66.2 – 68.4	64.2 – 66.4	30.9
68.4 – 70.6	66.4 – 68.6	33.5
> 70.6	>68.6	36.0†

† Tested in production. Remaining steps are specified by design.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Efficiency	vs Output power	1
P_O	Output power	vs Load resistance	2
		vs Supply voltage	3
I_Q	Quiescent supply current	vs Supply voltage	4
I_{CC}	Supply current	vs Output Power	5
$I_{Q(sd)}$	Quiescent shutdown supply current	vs Supply voltage	6
	Input impedance	vs Gain	7
THD+N	Total harmonic distortion + noise	vs Frequency	8, 9
		vs Output power	10, 11
k_{SVR}	Supply ripple rejection ratio	vs Frequency	12
	Closed loop response		13, 14
	Intermodulation performance		15
	Input offset voltage	vs Common-mode input voltage	16
	Crosstalk	vs Frequency	17
	Mute attenuation	vs Frequency	18
	Shutdown attenuation		19
	Common-mode rejection ratio	vs Frequency	20

TYPICAL CHARACTERISTICS

EFFICIENCY
vs
OUTPUT POWER

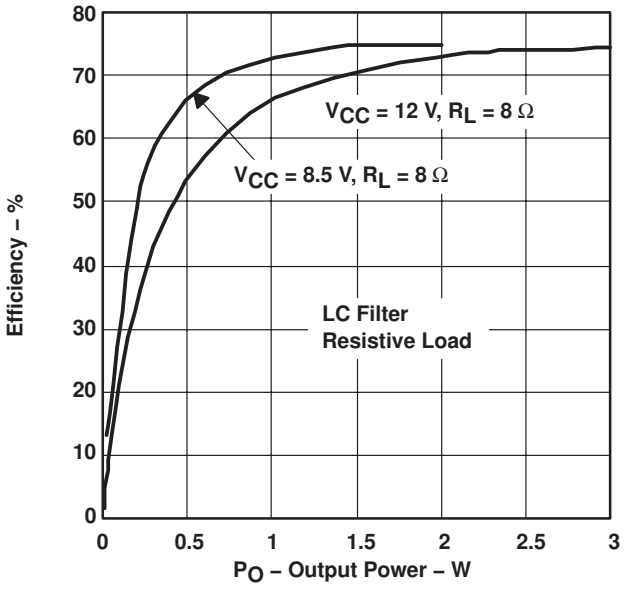


Figure 1

OUTPUT POWER
vs
LOAD RESISTANCE

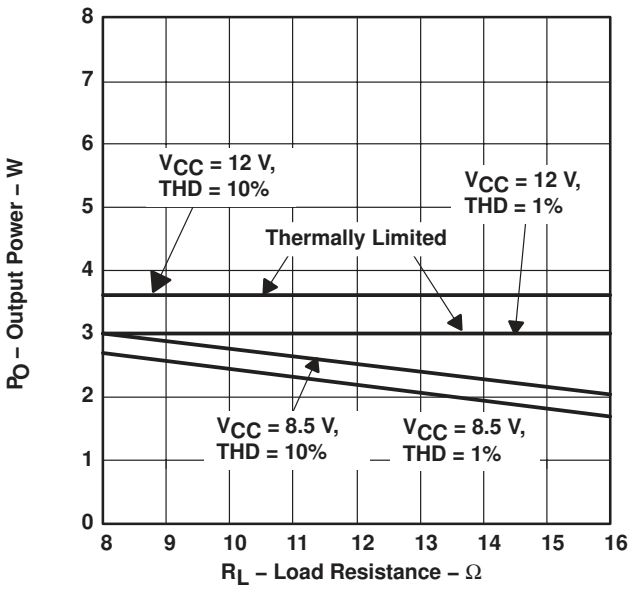


Figure 2

OUTPUT POWER
vs
SUPPLY VOLTAGE

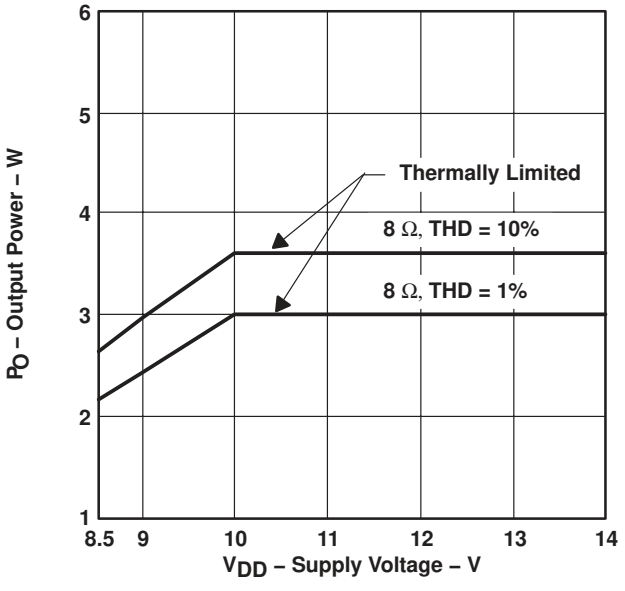


Figure 3

QUIESCENT SUPPLY CURRENT
vs
SUPPLY VOLTAGE

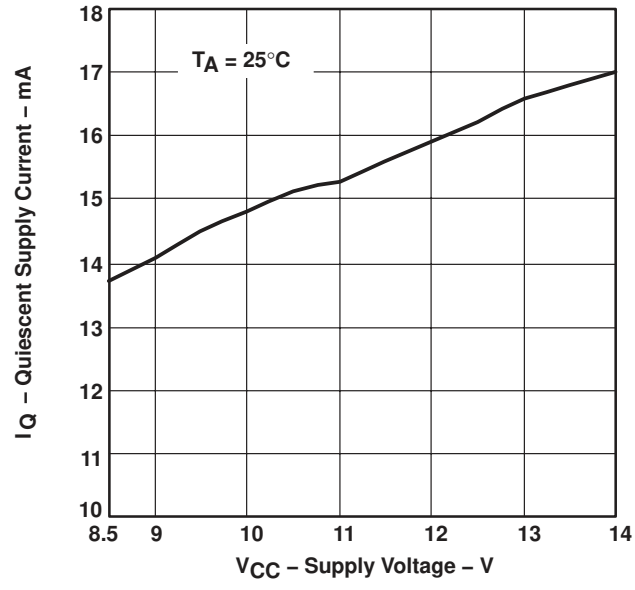


Figure 4

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs OUTPUT POWER (TOTAL)

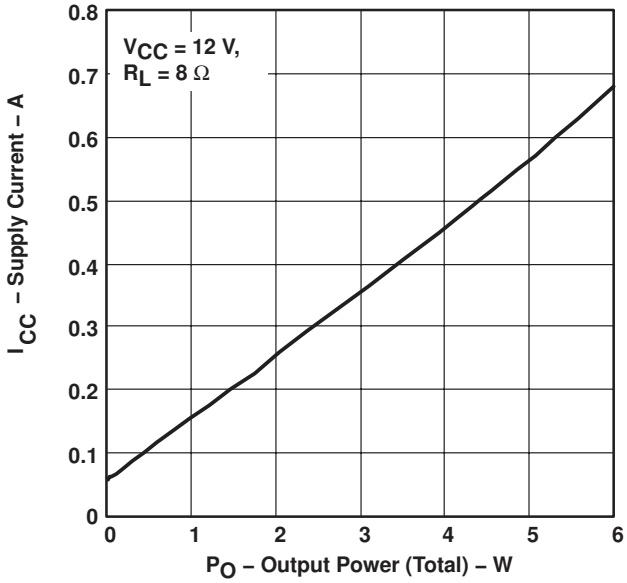


Figure 5

QUIESCENT SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE

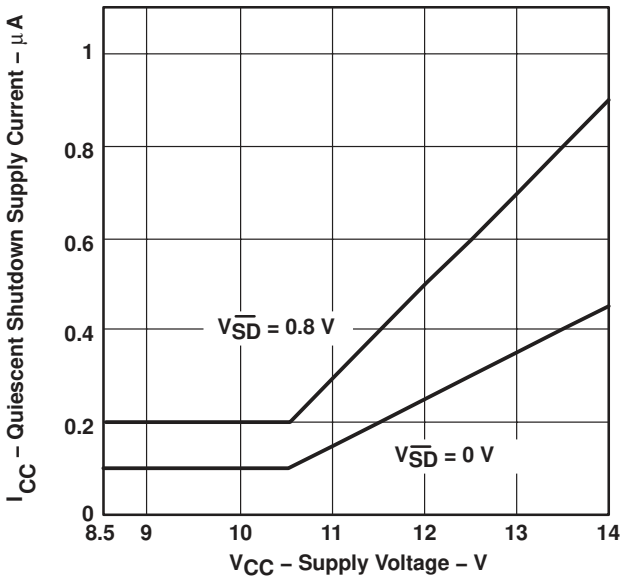


Figure 6

INPUT IMPEDANCE vs GAIN

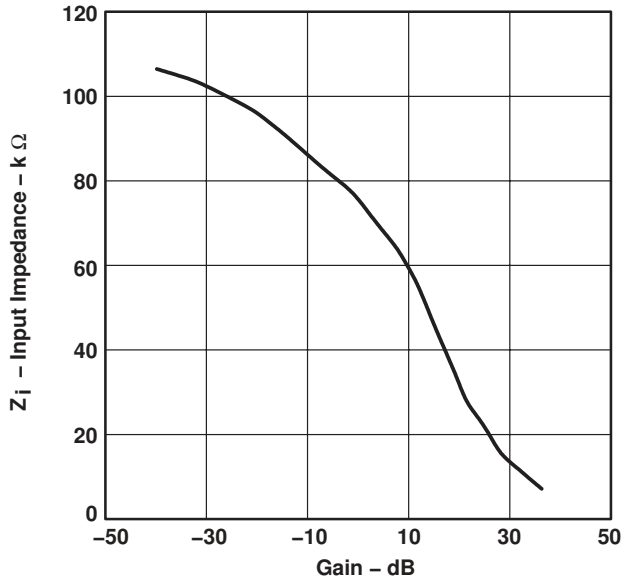


Figure 7

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

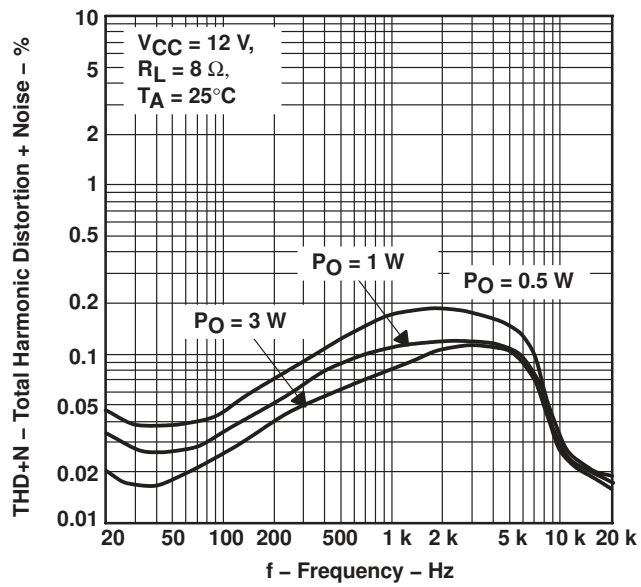


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

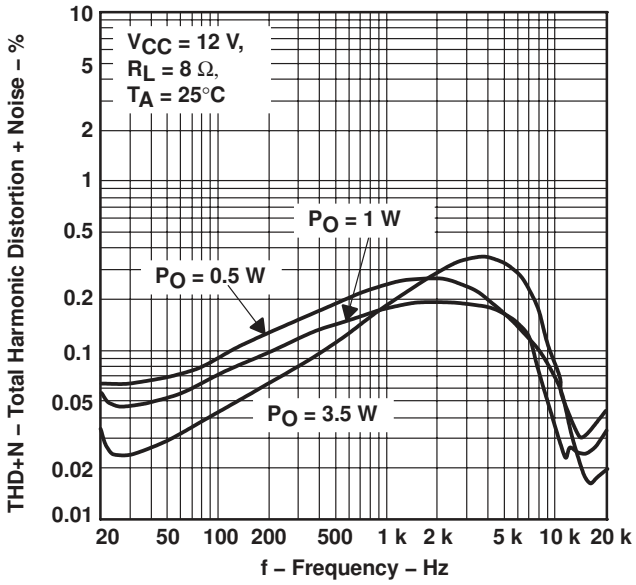


Figure 9

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

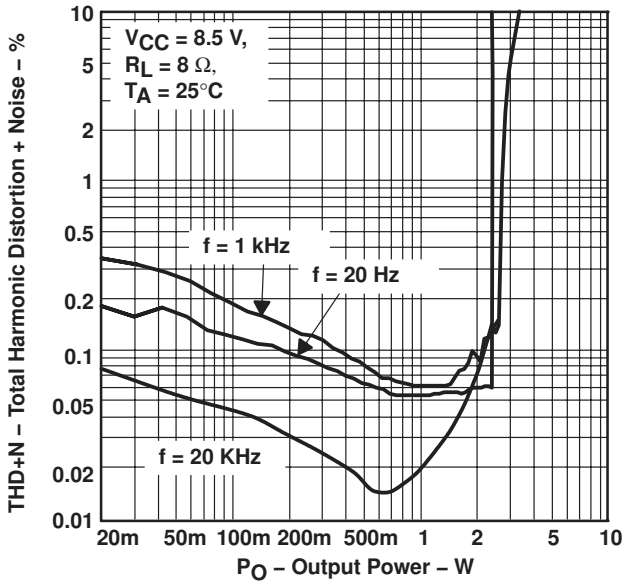


Figure 10

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

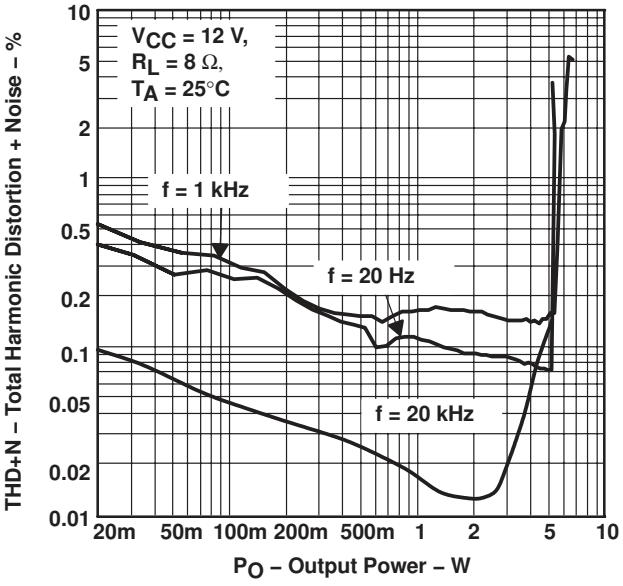


Figure 11

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

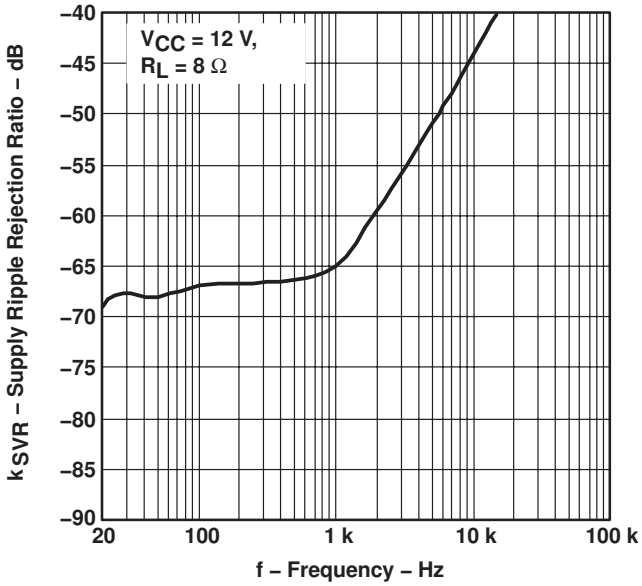


Figure 12

TYPICAL CHARACTERISTICS

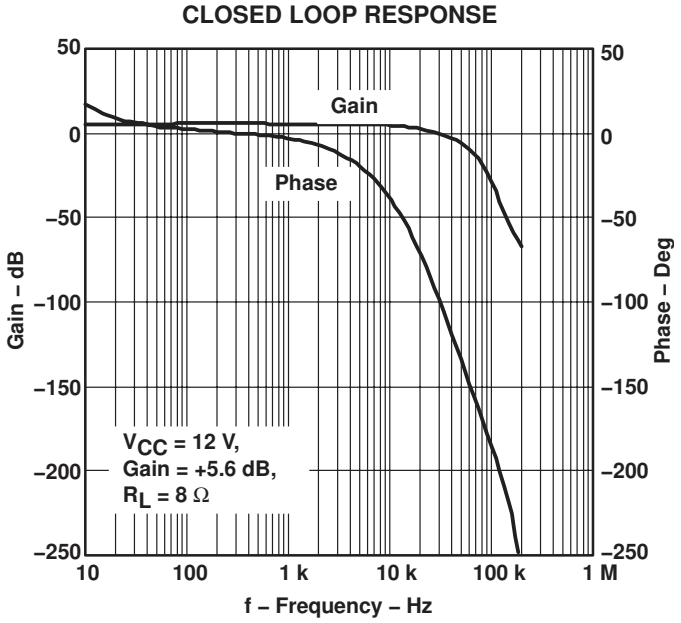


Figure 13

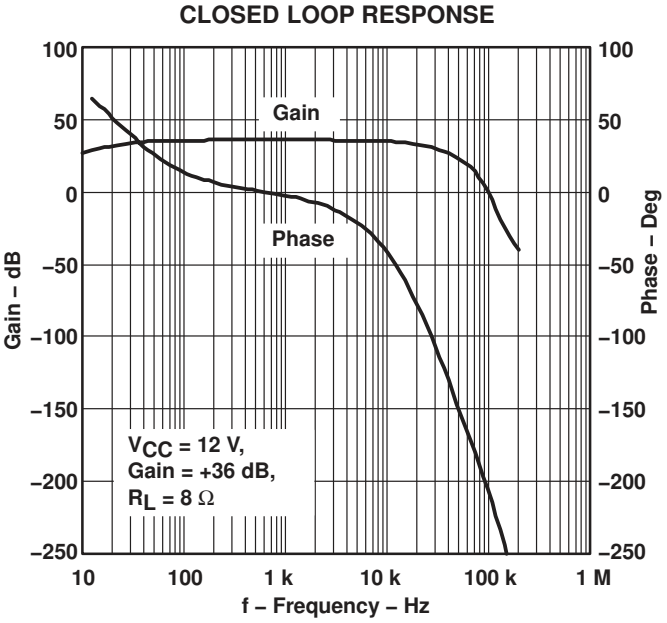


Figure 14

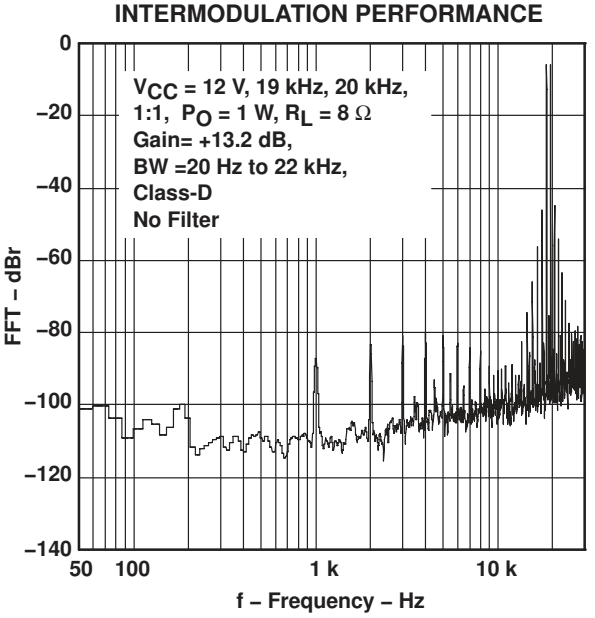


Figure 15

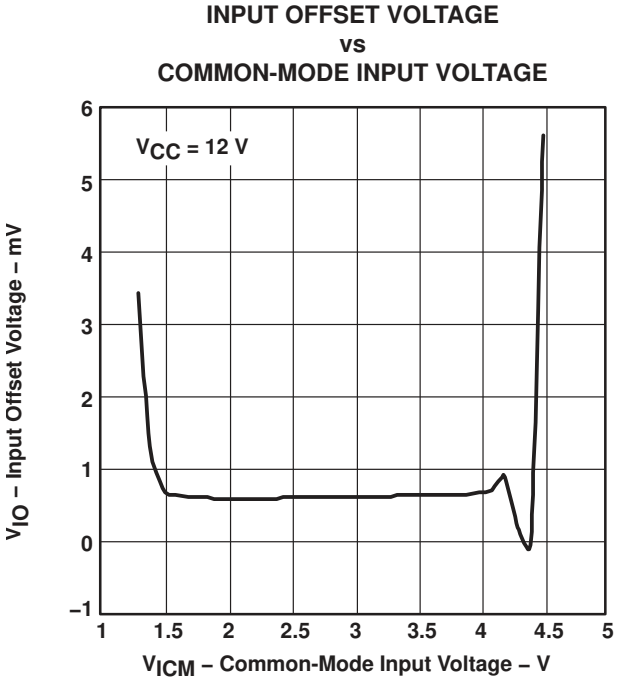


Figure 16

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

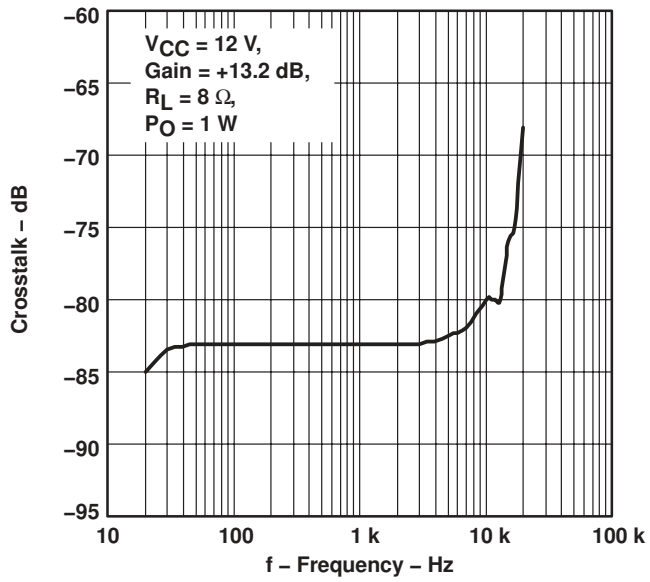


Figure 17

MUTE ATTENUATION vs FREQUENCY

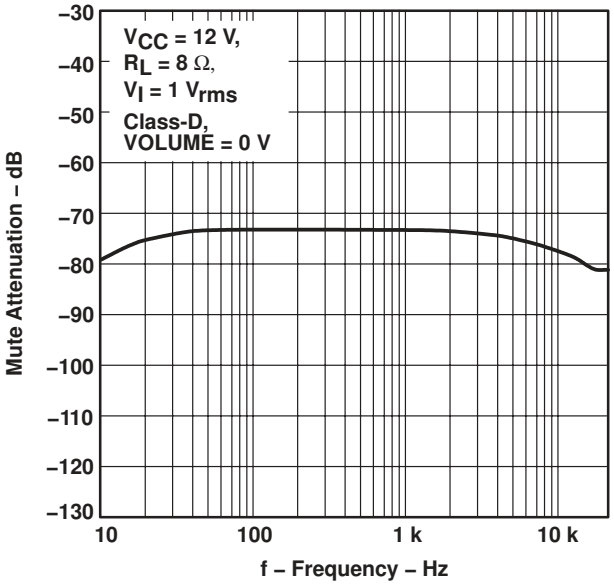


Figure 18

SHUTDOWN ATTENUATION vs FREQUENCY

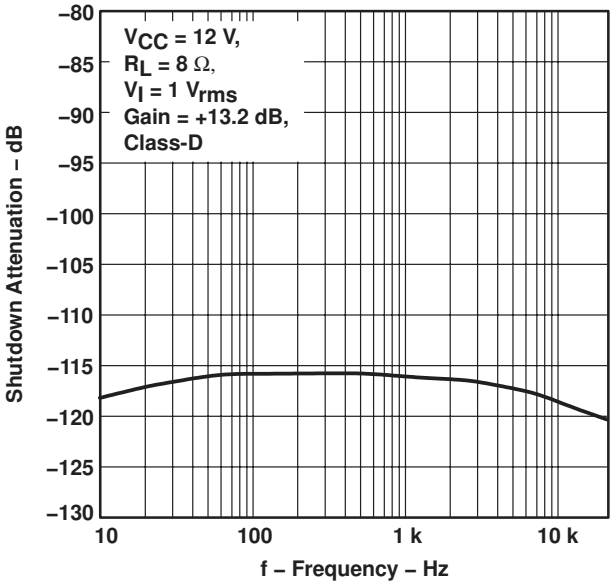


Figure 19

COMMON-MODE REJECTION RATIO vs FREQUENCY

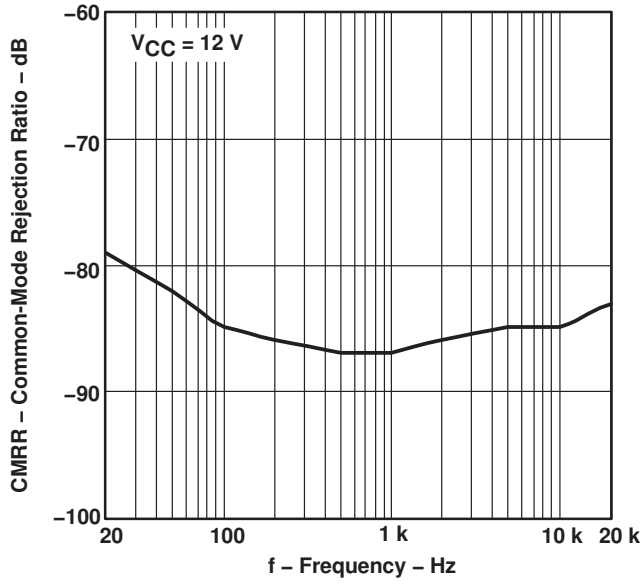


Figure 20

APPLICATION INFORMATION

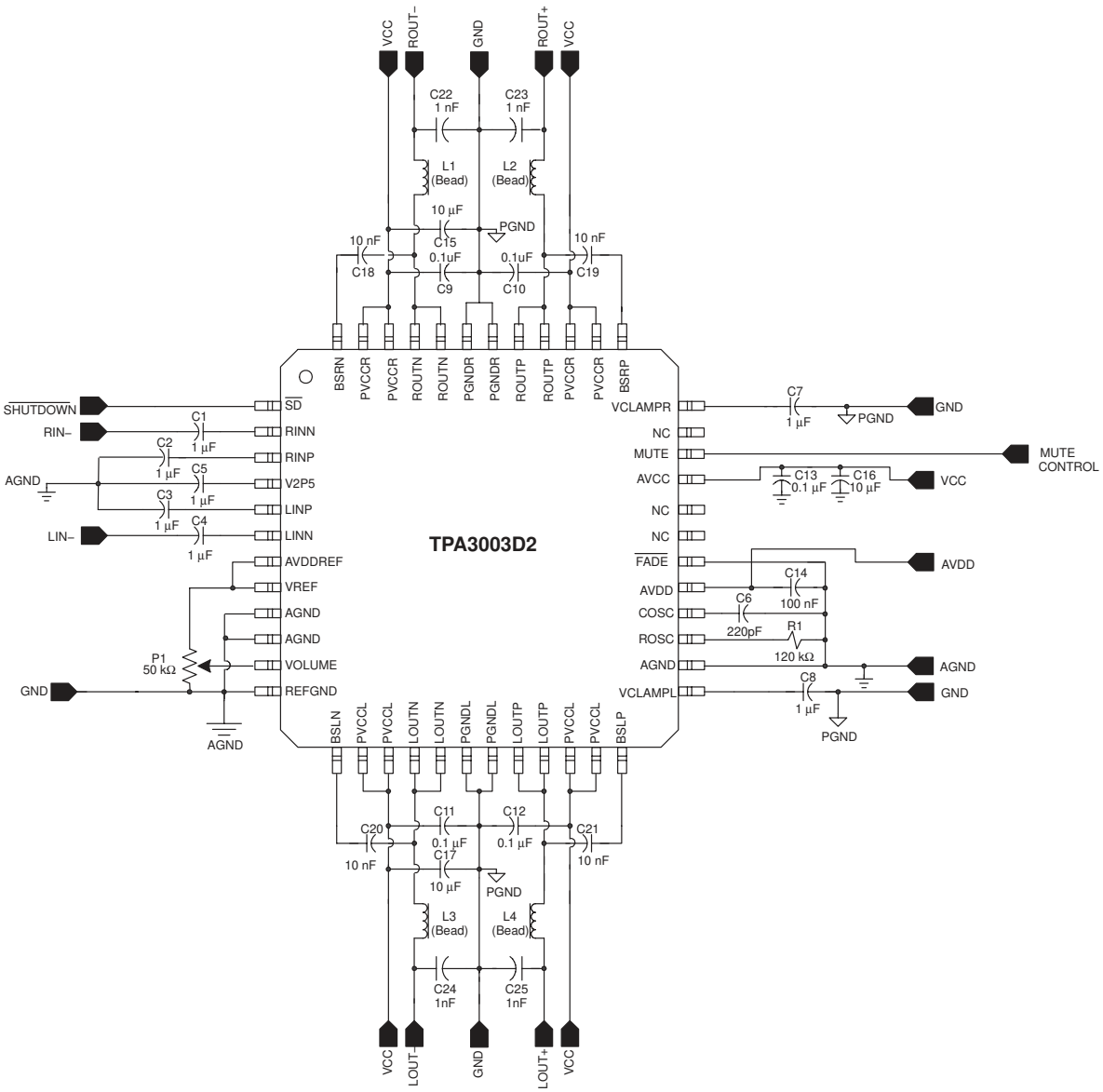


Figure 21. Stereo Configuration With Single-Ended Inputs

APPLICATION INFORMATION

class-D operation

This section focuses on the class-D operation of the TPA3003D2.

traditional class-D modulation scheme

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{CC}. Therefore, the differential prefiltered output varies between positive and negative V_{CC}, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 22. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss, thus causing a high supply current.

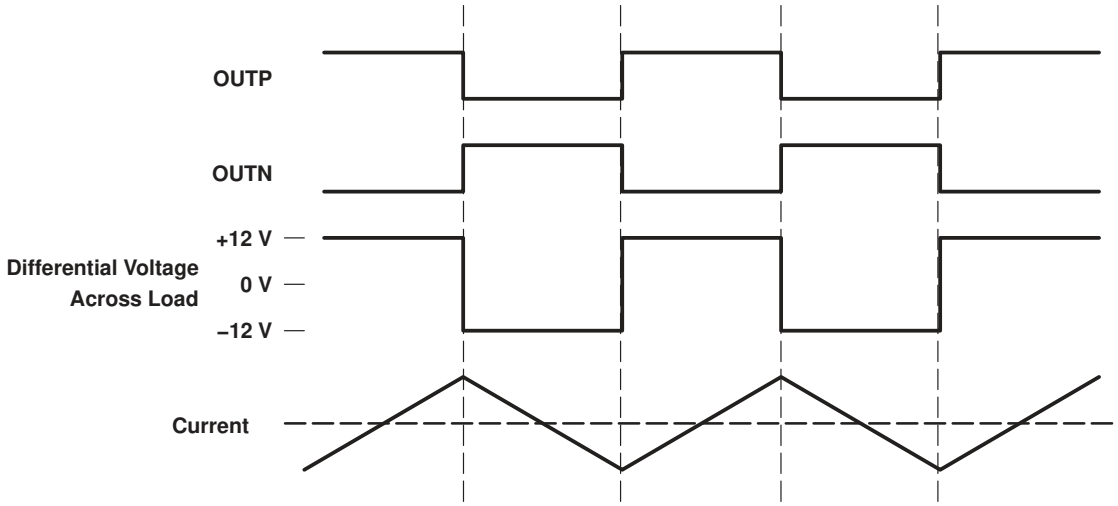


Figure 22. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA3003D2 modulation scheme

The TPA3003D2 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

APPLICATION INFORMATION

TPA3003D2 modulation scheme (continued)

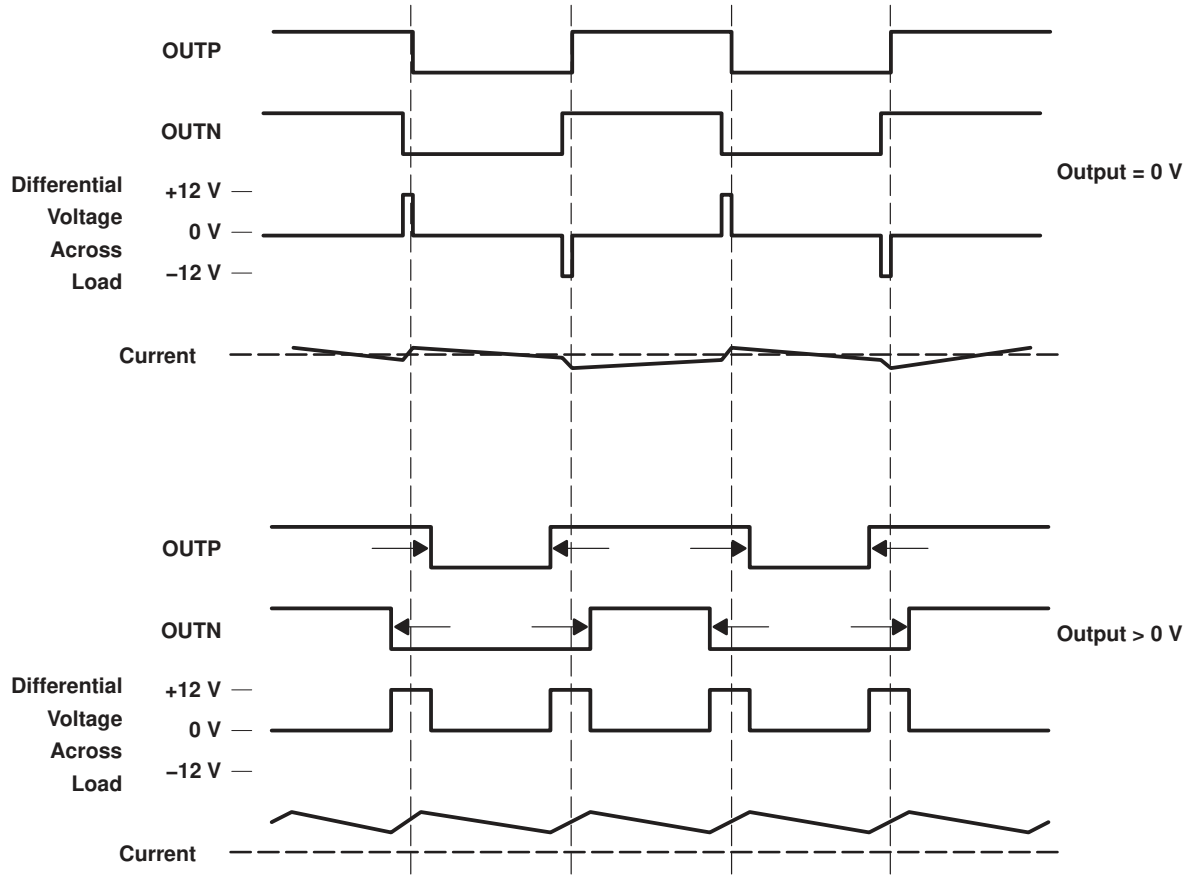


Figure 23. The TPA3003D2 Output Voltage and Current Waveforms Into an Inductive Load

efficiency: LC filter required with the traditional class-D modulation scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{CC}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3003D2 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is V_{CC} instead of $2 \times V_{CC}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker, which results in less power dissipation, therefore increasing efficiency.

APPLICATION INFORMATION

effects of applying a square wave into a speaker

Audio specialists have advised for years not to apply a square wave to speakers. If the amplitude of the waveform is high enough and the frequency of the square wave is within the bandwidth of the speaker, the square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, does not significantly move the voice coil, as the cone movement is proportional to $1/f^2$ for frequencies beyond the audio band.

Damage may occur if the voice coil cannot handle the additional heat generated from the high-frequency switching current. The amount of power dissipated in the speaker may be estimated by first considering the overall efficiency of the system. If the on-resistance ($r_{ds(on)}$) of the output transistors is considered to cause the dominant loss in the system, then the maximum theoretical efficiency for the TPA3003D2 with an 8-Ω load is as follows:

$$\text{Efficiency (theoretical, \%)} = R_L / \left(R_L + r_{ds(on)} \right) \times 100\% = 8/(8 + 1.4) \times 100\% = 85.11\% \quad (1)$$

The maximum measured output power is approximately 3 W with an 12-V power supply. The total theoretical power supplied ($P_{(total)}$) for this worst-case condition would therefore be as follows:

$$P_{(total)} = P_O/\text{Efficiency} = 3\ \text{W} / 0.8511 = 3.52\ \text{W} \quad (2)$$

The efficiency measured in the lab using an 8-Ω speaker was 75%. The power not accounted for as dissipated across the $r_{ds(on)}$ may be calculated by simply subtracting the theoretical power from the measured power:

$$\text{Other losses} = P_{(total)}\text{(measured)} - P_{(total)}\text{ (theoretical)} = 4 - 3.52 = 0.48\ \text{W} \quad (3)$$

The quiescent supply current at 12 V is measured to be 28.5 mA. It can be assumed that the quiescent current encapsulates all remaining losses in the device, i.e., biasing and switching losses. It may be assumed that any remaining power is dissipated in the speaker and is calculated as follows:

$$P_{(dis)} = 0.48\ \text{W} - (12\ \text{V} \times 28.5\ \text{mA}) = 0.14\ \text{W} \quad (4)$$

Note that these calculations are for the worst-case condition of 3 W delivered to the speaker. Since the 0.14 W is only 5% of the power delivered to the speaker, it may be concluded that the amount of power actually dissipated in the speaker is relatively insignificant. Furthermore, this power dissipated is well within the specifications of most loudspeaker drivers in a system, as the power rating is typically selected to handle the power generated from a clipping waveform.

when to use an output filter

Design the TPA3003D2 without the filter if the traces from amplifier to speaker are short (< 1 inch). Powered speakers, where the speaker is in the same enclosure as the amplifier, is a typical application for class-D without a filter.

Most applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use a LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires from the amplifier to the speaker.

APPLICATION INFORMATION

when to use an output filter (continued)

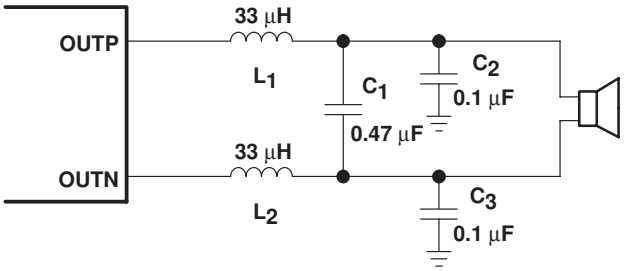


Figure 24. Typical LC Output Filter, Cutoff Frequency of 41 kHz, Speaker Impedance = 8 Ω

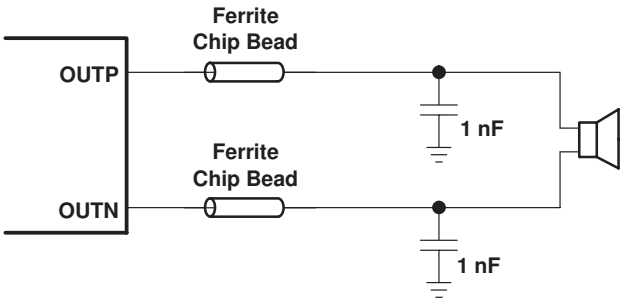


Figure 25. Typical Ferrite Chip Bead Filter (Chip bead example: Fair-Rite 2512067007Y3)

volume control operation

The VOLUME terminal controls the internal amplifier gain. This pin is controlled with a dc voltage, which should not exceed VREF. Table 1 lists the gain as determined by the voltage on the VOLUME pin in reference to the voltage on VREF.

If using a resistor divider to fix the gain of the amplifier, the VREF terminal can be directly connected to AVDDREF and a resistor divider can be connected across VREF and REFGND. (See Figure 21 in the Application Information Section). For fixed gain, calculate the resistor divider values necessary to center the voltage between the two percentage points given in the first column of Table 1. For example, if a gain of 10.7 dB is desired, the resistors in the divider network can both be 10 kΩ. With these resistor values, a voltage of 50%*VREF will be present at the VOLUME pin and result in a class-D gain of 10.7 dB.

If using a DAC to control the class-D gain, VREF and REFGND should be connected to the reference voltage for the DAC and the GND terminal of the DAC, respectively. For the DAC application, AVDDREF would be left unconnected. The reference voltage of the DAC provides the reference to the internal gain circuitry through the VREF input and any fluctuations in the DAC output voltage will not affect the TPA3003D2 gain. The percentages in the first column of Table 1 should be used for setting the voltages of the DAC when the voltage on the VOLUME terminal is increased. The percentages in the second column should be used for the DAC voltages when decreasing the voltage on the VOLUME terminal. Two lookup tables should be used in software to control the gain based on an increase or decrease in the desired system volume. This is explained further in a section below.

APPLICATION INFORMATION

volume control operation (continued)

If using an analog potentiometer to control the gain, it should be connected between VREF and REFGND. VREF can be connected to AVDDREF or an external voltage source, if desired. The first and second column in Table 1 should be used to determine the point at which the gain changes depending on the direction that the potentiometer is turned. If the voltage on the center tap of the potentiometer is increasing, the first column in Table 1 should be referenced to determine the trip points. If the voltage is decreasing, the trip points in the second column should be referenced.

The trip point, where the gain actually changes, is different depending on whether the voltage on the VOLUME terminal is increasing or decreasing as a result of hysteresis about each trip point. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. A pictorial representation of the volume control can be found in Figure 26. The graph focuses on three gain steps with the trip points defined in the first and second columns of Table 1. The dotted lines represent the hysteresis about each gain step.

The timing of the volume control circuitry is controlled by an internal 60-Hz clock. This clock determines the rate at which the gain changes when adjusting the voltage on the external volume control pins. The gain updates every 4 clock cycles (nominally 67 ms based on a 60 Hz clock) to the next step until the final desired gain is reached. For example, if the TPA3003D2 is currently in the +0.53 dB gain step and the VOLUME pin is adjusted for maximum gain at +36 dB, the time required for the gain to reach +36 dB is 14 steps x 67ms/step = 0.938 seconds. Referencing Table 1, there are 14 steps between the +0.53 dB gain step and the maximum gain step of +36 dB.

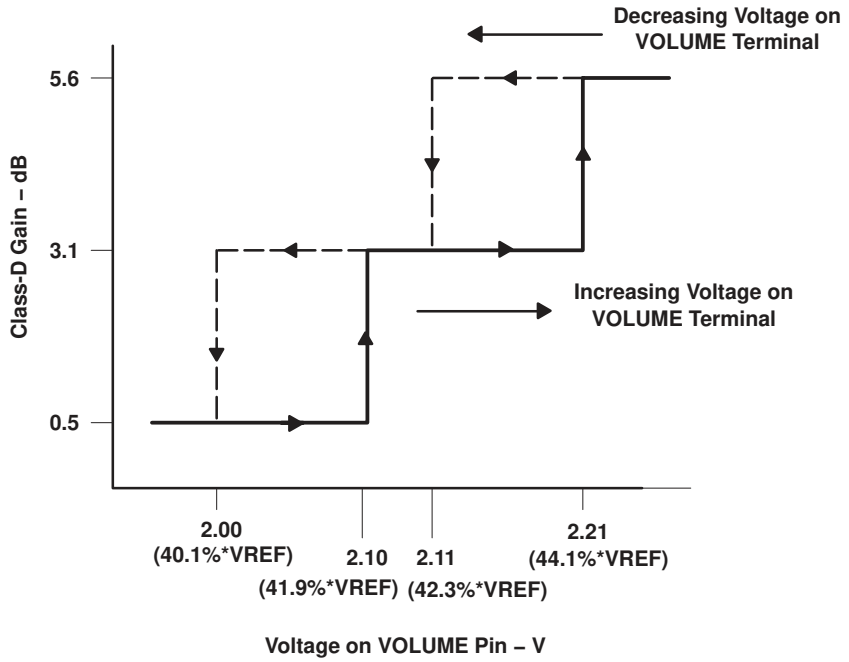


Figure 26. DC Volume Control Operation, VREF = 5 V

APPLICATION INFORMATION

$\overline{\text{FADE}}$ operation

The $\overline{\text{FADE}}$ terminal is a logic input that controls the operation of the volume control circuitry during transitions to and from the shutdown state and during power-up.

A logic low on this terminal places the amplifier in the fade mode. During power-up or recovery from the shutdown state (a logic high is applied to the $\overline{\text{SD}}$ terminal), the volume is smoothly ramped up from the mute state, –75 dB, to the desired volume setting determined by the voltage on the volume control terminal. Conversely, the volume is smoothly ramped down from the current state to the mute state when a logic low is applied to the $\overline{\text{SD}}$ terminal. The timing of the volume control circuitry is controlled by an internal 60-Hz clock. This clock determines the rate at which the gain changes when adjusting the voltage on the external volume control pins. The gain updates every 4 clock cycles (nominally 67 ms based on a 60 Hz clock) to the next step until the final desired gain is reached. For example, if the TPA3003D2 is currently in the +0.53 dB class-D gain step and the VOLUME pin is adjusted for maximum gain at +36 dB, the time required for the gain to reach 36 dB is 14 steps x 67 ms/step = 0.938 seconds. Referencing Table 1, there are 14 steps between the +0.53 dB gain step and the maximum gain step of +36 dB.

Figure 27 shows a scope capture of the differential output (measured across OUT+ and OUT–) with the amplifier in the fade mode. A 1 V_{pp} dc voltage was applied across the differential inputs and a logic low was applied to the $\overline{\text{SD}}$ terminal at the time defined in the figure. The figure depicts the outputs transitioning from one gain step to the next lower step at approximately 67 ms/step.

A logic high on this pin disables the volume fade effect during transitions to and from the shutdown state and during power-up. During power-up or recovery from the shutdown state (a logic high is applied to the $\overline{\text{SD}}$ terminal), the transition from the mute state, –75 dB, to the desired volume setting is less than 1 ms. Conversely, the volume ramps down from current state to the mute state within 1 ms when a logic low is applied to the $\overline{\text{SD}}$ terminal.

Figure 28 shows a scope capture of the differential output with the fade effect disabled. The outputs transition to the lowest gain state within 1ms of applying a logic low to the $\overline{\text{SD}}$ terminal.

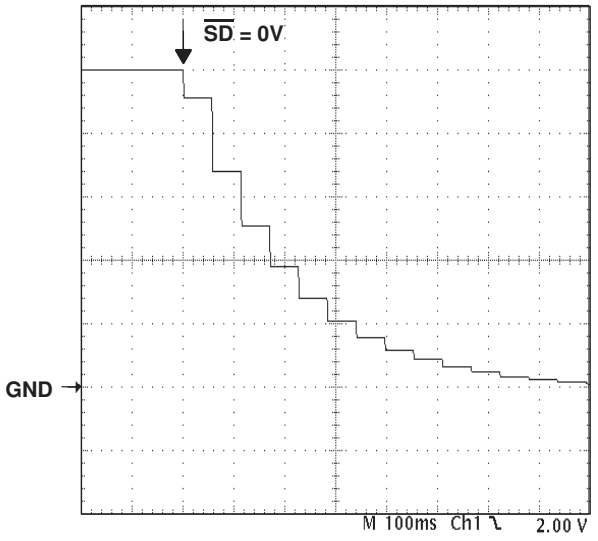


Figure 27. Differential Output With $\overline{\text{FADE}}$ (Terminal 30) Held Low

APPLICATION INFORMATION

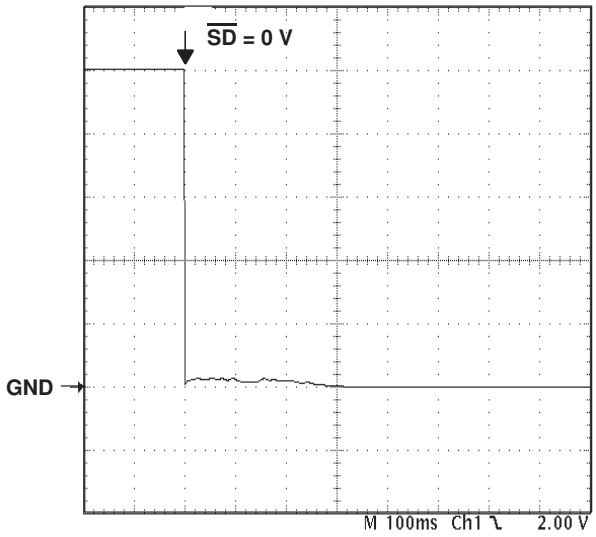


Figure 28. Differential Output With $\overline{\text{FADE}}$ Terminal Held High

MUTE operation

The MUTE pin is an input for controlling the output state of the TPA3003D2. A logic high on this pin disables the outputs. A logic low on this pin enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade. Quiescent current is listed in the dc characteristics specification table. The MUTE pin should never be left floating.

For power conservation, the $\overline{\text{SD}}$ pin should be used to reduce the quiescent current to the absolute minimum level. The volume will fade, slowly increase or decrease, when leaving or entering the shutdown state if the $\overline{\text{FADE}}$ terminal is held low. If the $\overline{\text{FADE}}$ terminal is held high, the outputs will transition very quickly. Refer to the $\overline{\text{FADE}}$ operation section.

$\overline{\text{SD}}$ operation

The TPA3003D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{\text{SD}}$ input terminal should be held high (see specification table for trip point)during normal operation when the amplifier is in use. Pulling $\overline{\text{SD}}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{\text{SD}}$ should never be left unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, the amplifier should be placed in the shutdown mode prior to removing the power supply voltage.

selection of COSC and ROSC

The switching frequency is determined using the values of the components connected to ROSC (pin 20) and COSC (pin 21) and may be calculated with the following equation:

$$f_{OSC} = 6.6 / (R_{OSC} * C_{OSC})$$

The frequency may be varied from 225 kHz to 275 kHz by adjusting the values chosen for R_{OSC} and C_{OSC}. The recommended values are C_{OSC} = 220 pF, R_{OSC}=120 kΩ for a switching frequency of 250 kHz.

APPLICATION INFORMATION

internal 2.5-V bias generator capacitor selection

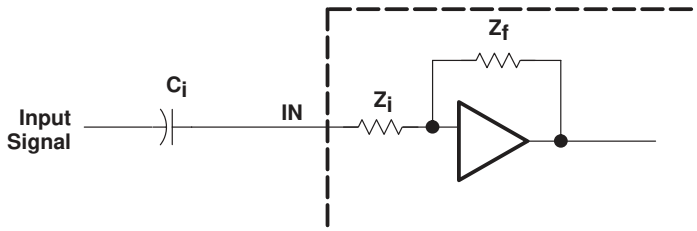
The internal 2.5-V bias generator (V2P5) provides the internal bias for the preamplifier stage. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the V2P5 terminal is critical for achieving the best device performance. During startup or recovery from the shutdown state, the V2P5 capacitor determines the rate at which the amplifier starts up. When the voltage on the V2P5 capacitor equals 0.75 x V2P5, or 75% of its final value, the device turns on and the class-D outputs start switching. The startup time is not critical for the best depop performance since any pop sound that is heard is the result of the class-D outputs switching on and not the startup time. However, at least a 0.47-µF capacitor is recommended for the V2P5 capacitor.

A secondary function of the V2P5 capacitor is to filter high frequency noise on the internal 2.5-V bias generator.

input resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency also changes by over six times.



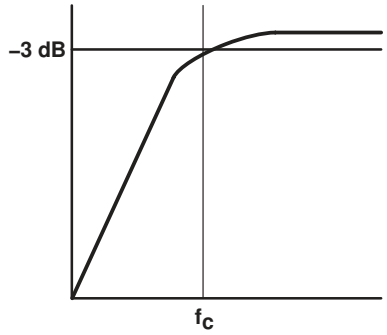
The –3-dB frequency can be calculated using equation 5.

$$f_{-3dB} = \frac{1}{2\pi Z_i C_i} \quad (5)$$

input capacitor, C_i

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level (V2P5) for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in equation 6.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (6)$$



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The value of C_i is important, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 6 is reconfigured as equation 7.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (7)$$

In this example, C_i is 0.4 μF, so one would likely choose a value in the range of 0.47 μF to 1 μF. If the gain is known and will be constant, use Z_i to calculate C_i. Calculations for C_i should be based off the impedance at the lowest gain step intended for use in the system. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2.5 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA3003D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{CC} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended. The 10-μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

BSN and BSP capacitors

The full H-bridge output stages use only NMOS transistors. They therefore require bootstrap capacitors for the high side of each output to turn on correctly. A 10-nF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 10-nF capacitor must be connected from xOUTP to xBSP, and one 10-nF capacitor must be connected from xOUTN to xBSN. (See the application circuit diagram in Figure 21.)

VCLAMP capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, two internal regulators clamp the gate voltage. Two 1-μF capacitors must be connected from VCLAMPL (pin 25) and VCLAMPR (pin 36) to ground and must be rated for at least 25 V. The voltages at the VCLAMP terminals vary with V_{CC} and may not be used for powering any other circuitry.

internal regulated 5-V supply (AV_{DD})

The AV_{DD} terminal (pin 29) is the output of an internally-generated 5-V supply, used for the oscillator, preamplifier, and volume control circuitry. It requires a 0.1-μF to 1-μF capacitor, placed very close to the pin, to ground to keep the regulator stable. The regulator may not be used to power any external circuitry.

APPLICATION INFORMATION

differential input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3003D2 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3003D2 with a single-ended source, ac ground the INP input through a capacitor equal in value to the input capacitor on INN and apply the audio source to the INN input. In a single-ended input application, the INP input should be ac-grounded at the audio source instead of at the device input for best noise performance.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

short-circuit protection

The TPA3003D2 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-V_{CC} shorts. When a short-circuit is detected on the outputs, the output drive is immediately disabled. This is a latched fault and must be reset by cycling the voltage on the $\overline{SD}$ pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

thermal protection

Thermal protection on the TPA3003D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 20°C. The device begins normal operation at this point with no external system interaction.

thermal considerations: output power and maximum ambient temperature

To calculate the maximum ambient temperature, the following equation may be used:

$$T_{Amax} = T_J - \Theta_{JA} P_{Dissipated}$$

where: $T_J = 150°C$

$\Theta_{JA} = 45°C/W$ (8)

(The derating factor for the 48-pin PFB package is given in the dissipation rating table.)

To estimate the power dissipation, the following equation may be used:

$$P_{Dissipated} = P_{O(average)} \times ((1 / Efficiency) - 1)$$

Efficiency = ~75% for an 8-Ω load (9)

APPLICATION INFORMATION

thermal considerations: output power and maximum ambient temperature (continued)

Example. What is the maximum ambient temperature for an application that requires the TPA3003D2 to drive 3 W into an 8-Ω speaker (stereo)?

$P_{Dissipated}$ = 6 W x ((1 / 0.75) – 1) = 2 W (P_O = 3 W * 2)

T_{Amax} = 150°C – (45°C/W x 2 W) = 60°C

This calculation shows that the TPA3003D2 can drive 3 W of continuous RMS power per channel into an 8-Ω speaker up to an ambient temperature of 60°C.

printed circuit board (PCB) layout

Because the TPA3003D2 is a class-D amplifier that switches at a high frequency, the layout of the printed circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors — As described on page 23, the high-frequency 0.1-uF decoupling capacitors should be placed as close to the PVCC (pin 14, 15, 22, 23, 38, 39, 46, 47) and AV_{CC} (pin 33) terminals as possible. The V2P5 (pin 4) capacitor, AV_{DD} (pin 29) capacitor, and VCLAMP (pins 25, 36) capacitor should also be placed as close to the device as possible. Large (10 uF or greater) bulk power supply decoupling capacitors should be placed near the TPA3003D2 on the PVCCL, PVCCR, and AV_{CC} terminals.
- Grounding — The AV_{CC} (pin 33) decoupling capacitor, AV_{DD} (pin 29) capacitor, V2P5 (pin 4) capacitor, COSC (pin 28) capacitor, and ROSC (pin 27) resistor should each be grounded to analog ground (AGND, pin 26. The PVCC (pin 9 and pin 16) decoupling capacitors should each be grounded to power ground (PGND, pins 18, 19, 42, 43). Basically, an AGND island should be created with a single connection to PGND.
- Output filter — The ferrite EMI filter (Figure 25, page 18) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 24, page 18 should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to PGND.

For an example layout, please refer to the TPA3003D2 Evaluation Module (TPA3003D2EVM) User Manual, TI literature number SLOU159. The EVM user manual is available on the TI web site at http://www.ti.com.

basic measurement system

This section focuses on methods that use the basic equipment listed below:

- Audio analyzer or spectrum analyzer
- Digital multimeter (DMM)
- Oscilloscope
- Twisted pair wires
- Signal generator
- Power resistor(s)
- Linear regulated power supply
- Filter components
- EVM or other complete audio circuit

APPLICATION INFORMATION

Figure 29 shows the block diagrams of basic measurement systems for class-AB and class-D amplifiers. A sine wave is normally used as the input signal since it consists of the fundamental frequency only (no other harmonics are present). An analyzer is then connected to the APA output to measure the voltage output. The analyzer must be capable of measuring the entire audio bandwidth. A regulated dc power supply is used to reduce the noise and distortion injected into the APA through the power pins. A System Two audio measurement system (AP-II) (Reference 1) by Audio Precision includes the signal generator and analyzer in one package.

The generator output and amplifier input must be ac-coupled. However, the EVMs already have the ac-coupling capacitors, (C_{IN}), so no additional coupling is required. The generator output impedance should be low to avoid attenuating the test signal, and is important since the input resistance of APAs is not very high (about 10 kΩ). Conversely the analyzer-input impedance should be high. The output impedance, R_{OUT}, of the APA is normally in the hundreds of milliohms and can be ignored for all but the power-related calculations.

Figure 29(a) shows a class-AB amplifier system, which is relatively simple because these amplifiers are linear their output signal is a linear representation of the input signal. They take analog signal input and produce analog signal output. These amplifier circuits can be directly connected to the AP-II or other analyzer input.

This is not true of the class-D amplifier system shown in Figure 29(b), which requires low pass filters in most cases in order to measure the audio output waveforms. This is because it takes an analog input signal and converts it into a pulse-width modulated (PWM) output signal that is not accurately processed by some analyzers.

APPLICATION INFORMATION

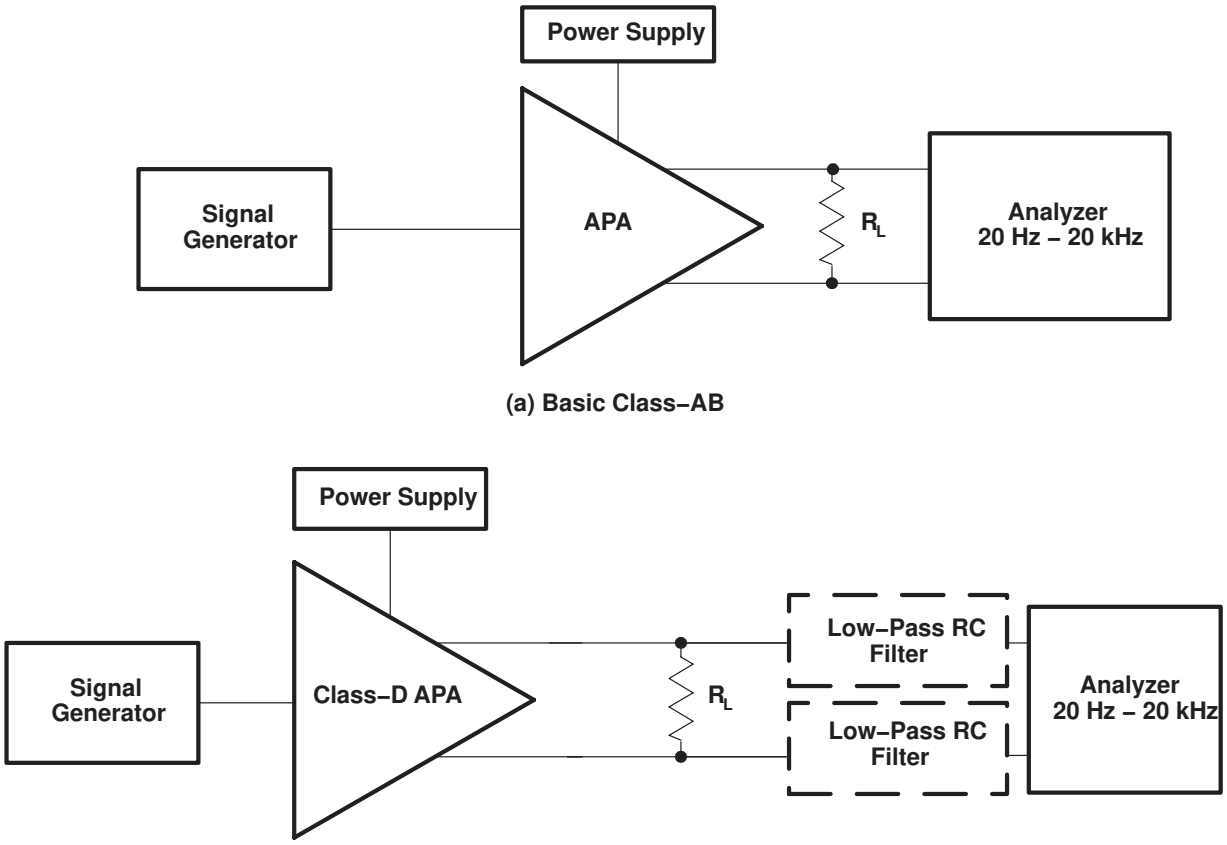


Figure 29. Audio Measurement Systems

The TPA3003D2 uses a modulation scheme that does not require an output filter for operation, but they do sometimes require an RC low-pass filter when making measurements. This is because some analyzer inputs cannot accurately process the rapidly changing square-wave output and therefore record an extremely high level of distortion. The RC low-pass measurement filter is used to remove the modulated waveforms so the analyzer can measure the output sine wave.

APPLICATION INFORMATION

differential input and BTL output

All of the class-D APAs and many class-AB APAs have differential inputs and bridge-tied load (BTL) outputs. Differential inputs have two input pins per channel and amplify the difference in voltage between the pins. Differential inputs reduce the common-mode noise and distortion of the input circuit. BTL is a term commonly used in audio to describe differential outputs. BTL outputs have two output pins providing voltages that are 180 degrees out of phase. The load is connected between these pins. This has the added benefits of quadrupling the output power to the load and eliminating a dc blocking capacitor.

A block diagram of the measurement circuit is shown in Figure 30. The differential input is a balanced input, meaning the positive (+) and negative (–) pins will have the same impedance to ground. Similarly, the BTL output equates to a balanced output.

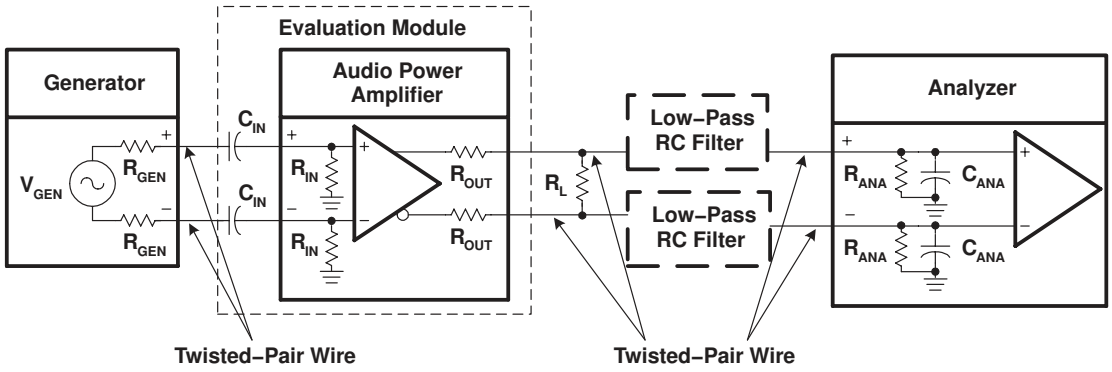


Figure 30. Differential Input—BTL Output Measurement Circuit

The generator should have balanced outputs and the signal should be balanced for best results. An unbalanced output can be used, but it may create a ground loop that will affect the measurement accuracy. The analyzer must also have balanced inputs for the system to be fully balanced, thereby cancelling out any common mode noise in the circuit and providing the most accurate measurement.

The following general rules should be followed when connecting to APAs with differential inputs and BTL outputs:

- Use a balanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 2).

Table 2 shows the recommended wire size for the power supply and load cables of the APA system. The real concern is the dc or ac power loss that occurs as the current flows through the cable. These recommendations are based on 12-inch long wire with a 20-kHz sine-wave signal at 25°C.

APPLICATION INFORMATION

Table 2. Recommended Minimum Wire Size for Power Cables

P_{OUT} (W)	R_L (Ω)	AWG SIZE	DC POWER LOSS (mW)		AC POWER LOSS (mW)	
1	8	22 to 28	2.0	8.0	2.1	8.1
< 0.75	8	22 to 28	1.5	6.1	1.6	6.2

Class-D RC low-pass filter

A RC filter is used to reduce the square-wave output when the analyzer inputs cannot process the pulse-width modulated class-D output waveform. This filter has little effect on the measurement accuracy because the cutoff frequency is set above the audio band. The high frequency of the square wave has negligible impact on measurement accuracy because it is well above the audible frequency range and the speaker cone cannot respond at such a fast rate. The RC filter is not required when an LC low-pass filter is used, such as with the class-D APAs that employ the traditional modulation scheme (TPA032D0x, TPA005Dxx).

The component values of the RC filter are selected using the equivalent output circuit as shown in Figure 31. R_L is the load impedance that the APA is driving for the test. The analyzer input impedance specifications should be available and substituted for R_{ANA} and C_{ANA}. The filter components, R_{FILT} and C_{FILT}, can then be derived for the system. The filter should be grounded to the APA near the output ground pins or at the power supply ground pin to minimize ground loops.

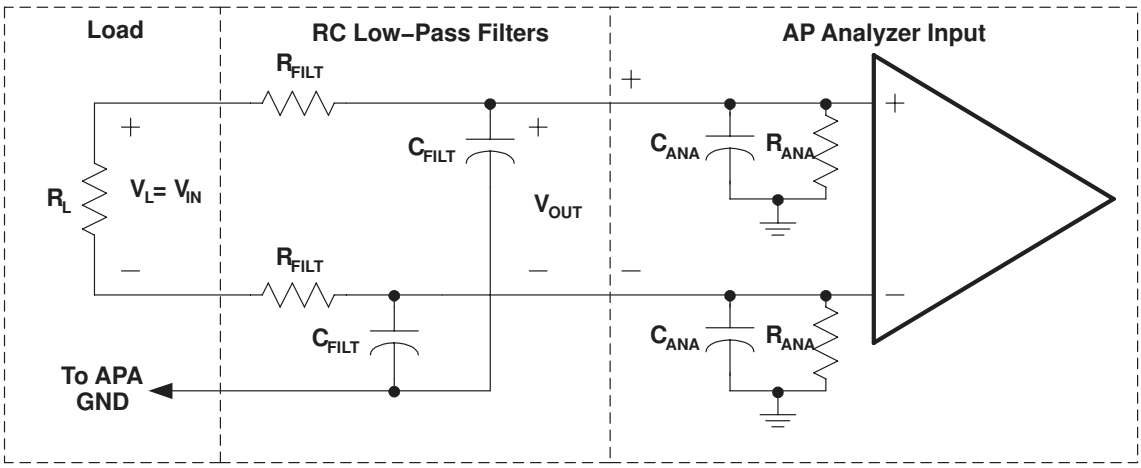


Figure 31. Measurement Low-Pass Filter Derivation Circuit—Class-D APAs

APPLICATION INFORMATION

The transfer function for this circuit is shown in equation (10) where $\omega_O = R_{EQ}C_{EQ}$, $R_{EQ} = R_{FILT} \| R_{ANA}$ and $C_{EQ} = (C_{FILT} + C_{ANA})$. The filter frequency should be set above f_{MAX}, the highest frequency of the measurement bandwidth, to avoid attenuating the audio signal. Equation (11) provides this cutoff frequency, f_C. The value of R_{FILT} must be chosen large enough to minimize current that is shunted from the load, yet small enough to minimize the attenuation of the analyzer-input voltage through the voltage divider formed by R_{FILT} and R_{ANA}. A rule of thumb is that R_{FILT} should be small (~100 Ω) for most measurements. This reduces the measurement error to less than 1% for $R_{ANA} \geq 10$ kΩ.

$$\left(\frac{V_{OUT}}{V_{IN}}\right) = \frac{\left(\frac{R_{ANA}}{R_{ANA} + R_{FILT}}\right)}{1 + j\left(\frac{\omega}{\omega_O}\right)} \tag{10}$$

$$f_C = \sqrt{2} \times f_{MAX} \tag{11}$$

An exception occurs with the efficiency measurements, where R_{FILT} must be increased by a factor of ten to reduce the current shunted through the filter. C_{FILT} must be decreased by a factor of ten to maintain the same cutoff frequency. See Table 3 for the recommended filter component values.

Once f_C is determined and R_{FILT} is selected, the filter capacitance is calculated using equation (12). When the calculated value is not available, it is better to choose a smaller capacitance value to keep f_C above the minimum desired value calculated in equation (11).

$$C_{FILT} = \frac{1}{2\pi \times f_C \times R_{FILT}} \tag{12}$$

Table 3 shows recommended values of R_{FILT} and C_{FILT} based on common component values. The value of f_C was originally calculated to be 28 kHz for an f_{MAX} of 20 kHz. C_{FILT}, however, was calculated to be 57000 pF, but the nearest values of 56000 pF and 51000 pF were not available. A 47000 pF capacitor was used instead, and f_C is 34 kHz, which is above the desired value of 28 kHz.

Table 3. Typical RC Measurement Filter Values

MEASUREMENT	R_{FILT}	C_{FILT}
Efficiency	1 000 Ω	5 600 pF
All other measurements	100 Ω	56 000 pF

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3003D2PFB	NRND	TQFP	PFB	48	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA3003D2	
TPA3003D2PFBR	NRND	TQFP	PFB	48	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA3003D2	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

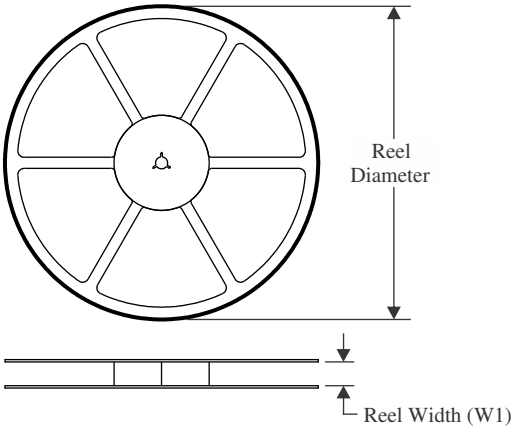
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

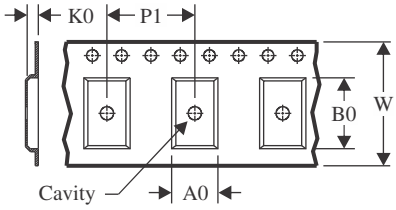
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

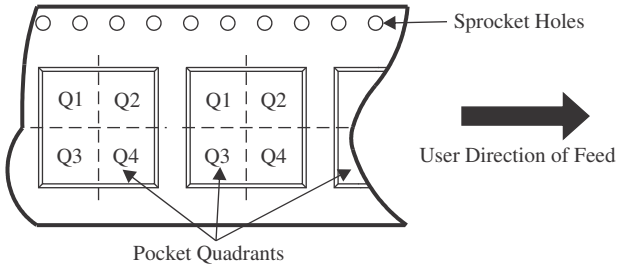


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

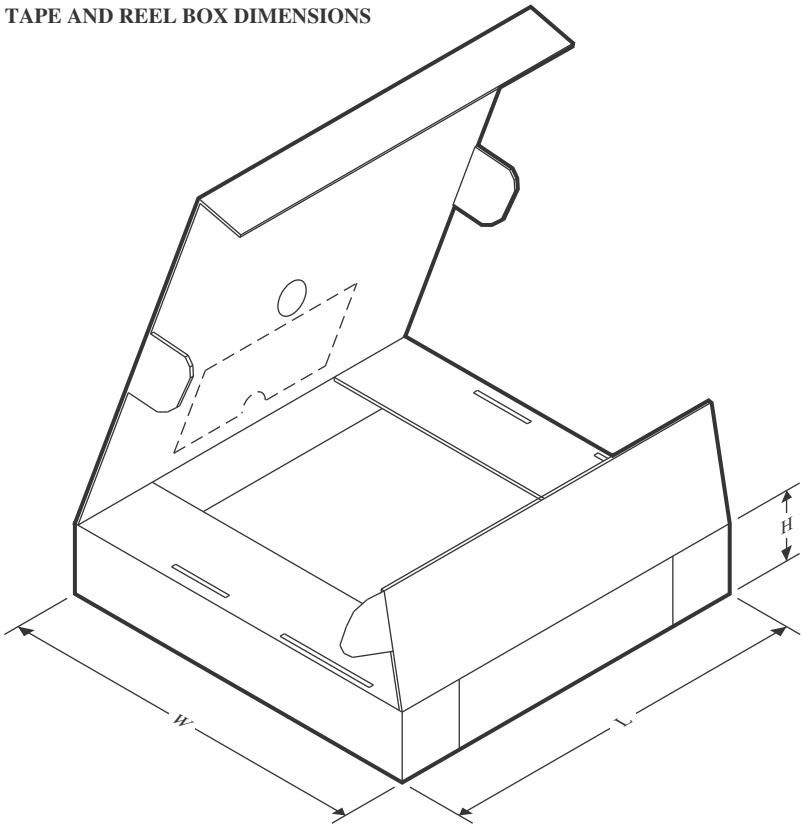
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3003D2PFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

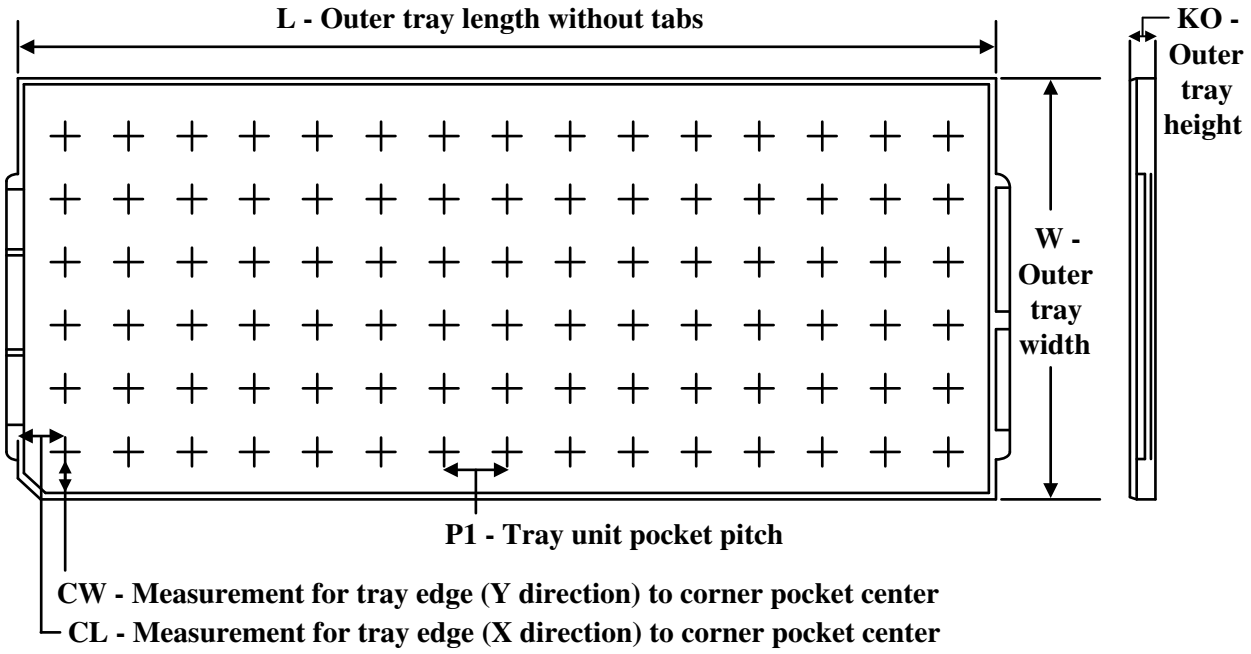
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3003D2PFBR	TQFP	PFB	48	1000	350.0	350.0	43.0

TRAY



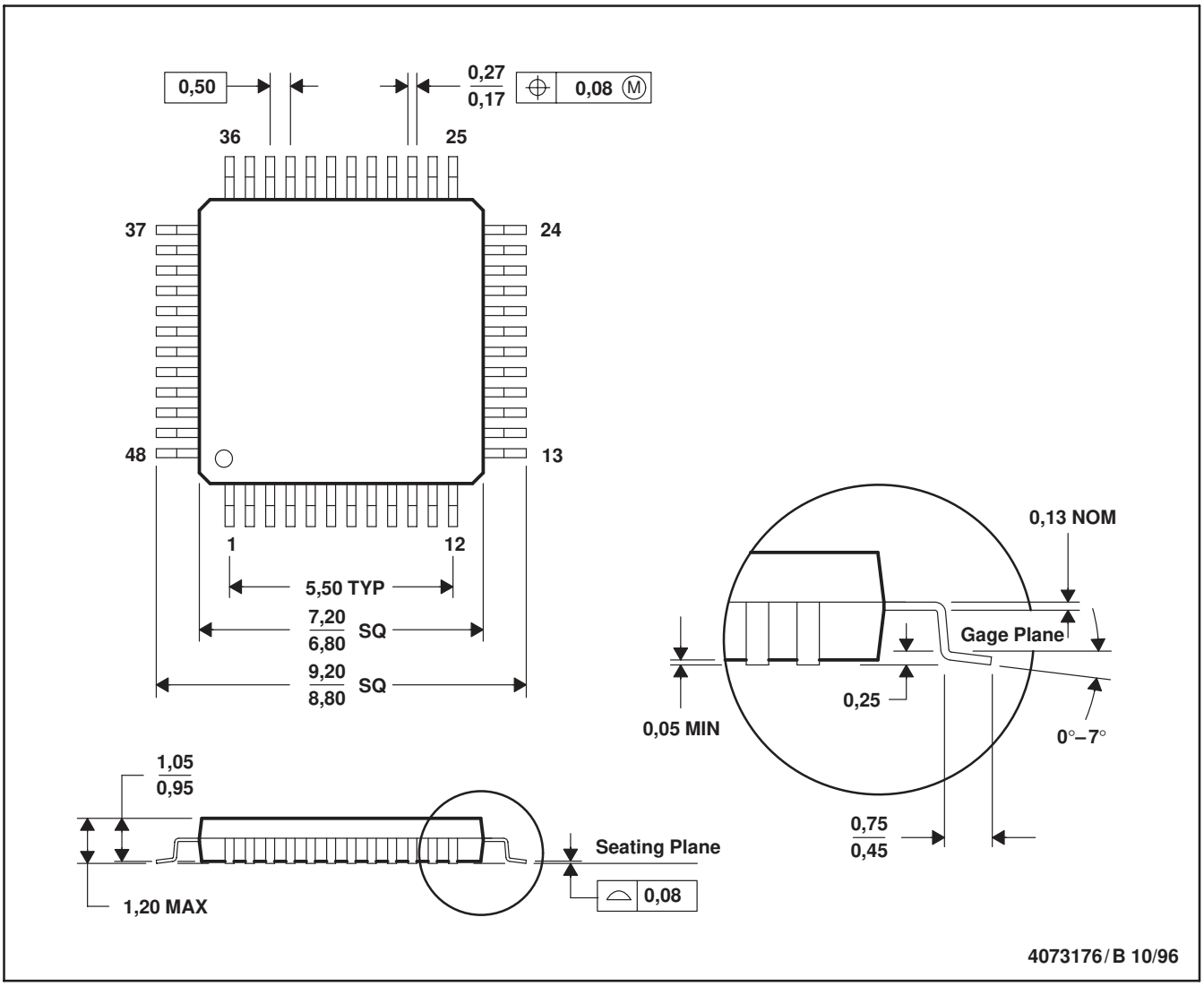
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TPA3003D2PFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

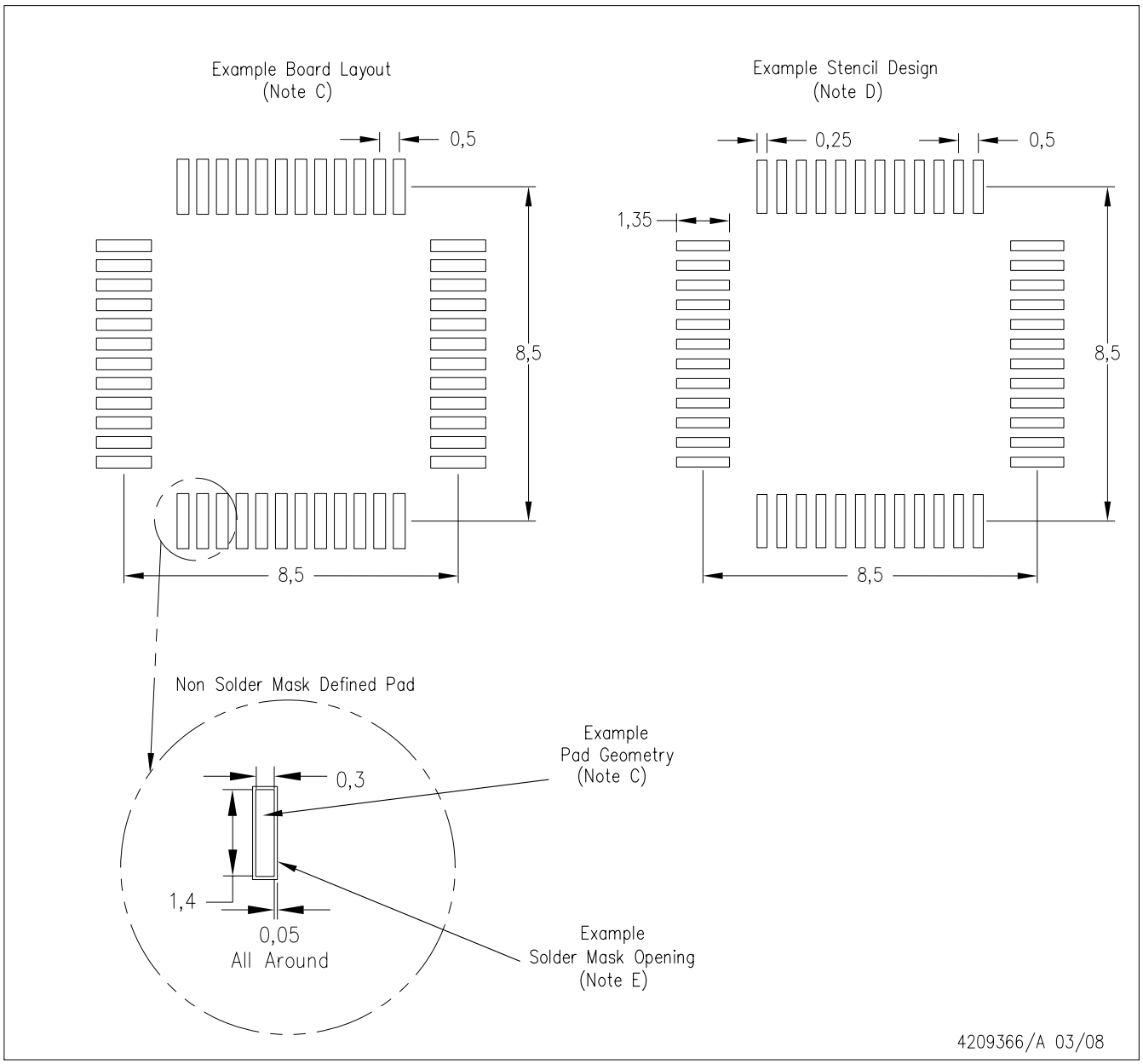
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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