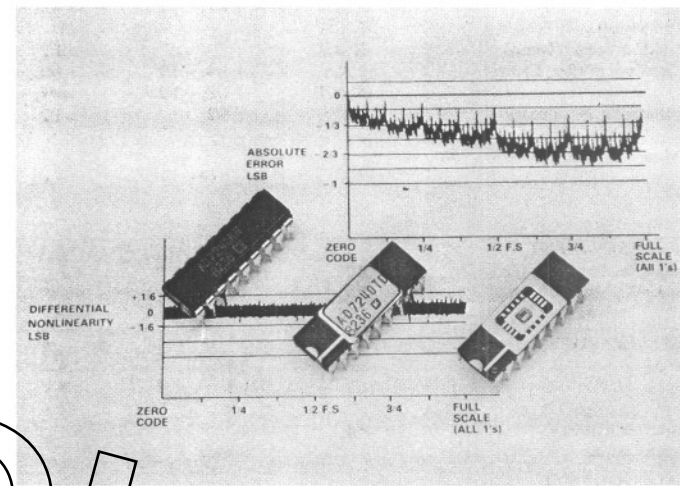
LC²MOS High Speed 12-Bit Voltage DAC

AD7240

FEATURES
- Fast Voltage Settling Time: 550ns to 0.01%
- Total Unadjusted Error: 1LSB max
- Single Supply Operation
- Latch Up Proof (No Protection Schottky Required)
- Superb Differential Nonlinearity: 1/2LSB max over Temperature
- Low Power Dissipation: 30mW

APPLICATIONS
- Battery Powered Instrumentation
- High Speed A/D Converters
- Programmable Gain Amplifiers
- Vector Graphics
- S/D Converters



GENERAL DESCRIPTION

The Analog Devices AD7240 is a fast settling (550ns typically to 1/2LSB) 12-bit voltage output digital to analog converter. It is fabricated using an advanced high speed Linear Compatible CMOS process (LC²MOS) which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

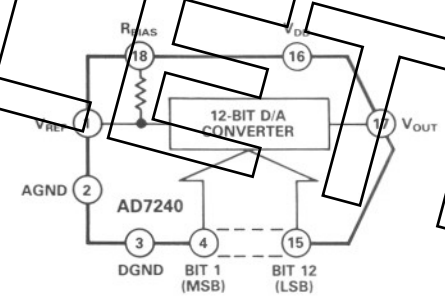
The AD7240 operates with single +15 volts V_{DD} supply and exhibits exceptionally fast settling times due to the small (and code independent) value of capacitance at the output of the DAC.

The AD7240 also gives superior performance to other CMOS DACs when configured in the current steering mode as a multiplying DAC.

PRODUCT HIGHLIGHTS

1. **Single Supply Operation:** Voltage mode operation allows the AD7240 to be run from a single supply rail.
2. **High Speed Voltage Settling:** The high speed LC²MOS process gives the AD7240 extremely small propagation delays. The low capacitance of the AD7240 reduces the time constant at the DAC output. Thus the overall settling time is small (settling to 0.01% – typically 550ns).
3. **Total Unadjusted Error:** Includes gain error, offset error and relative accuracy. Connection of an AD7240 to a fixed reference guarantees the output voltage without external trimming. Connection of two or more DAC's to the same reference means that their output voltages will track to within the accuracy limits of the AD7240.
4. **Guaranteed Monotonicity:** All grades are guaranteed monotonic to 12 bits over all temperature ranges, in both the voltage mode and the current mode.

FUNCTIONAL DIAGRAM



PRICING (100+)

AD7240JN	$ 9.70
AD7240KN	$10.70
AD7240AQ	$11.20
AD7240BQ	$12.20
AD7240SD	$39.95
AD7240TD	$44.80

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 714/842-1717 | Mid-West 312/653-5000 | Texas 214/231-5094

SPECIFICATIONS (V_{DD} = +15V, V_{REF} = +1.23V, AGND = DGND = R_{BIAS} = 0V unless noted otherwise)

Parameter	Version	T_A = +25°C	T_A = T_{min} to T_{max}	Units	Test Conditions/Comments
ACCURACY					
Resolution	All	12	12	Bits min	
Total Unadjusted Error[1,2]	J,A,S	+1/2, −1 1/4	+1/2, −2	LSB max	This specification applies to all codes, however
	K,B,T	+1/2, −1	+1/2, −1 1/2	LSB max	equal or superior specifications apply for
					zero code and Full Scale Code – See Below
Relative Accuracy[1,2]	J,A,S	+1/2, −1 1/4	+1/2, −2	LSB max	
	K,B,T	+1/2, −1	+1/2, −1 1/2	LSB max	
Full Scale (Gain) Error[1,2]	J,A,S	+1/2, −1 1/4	+1/2, −2	LSB max	
	K,B,T	+1/2, −1/2	+1/2, −1/2	LSB max	
Full Scale (Gain) Tempco	J,A,S		±6	ppm/°C max	
(ΔFull Scale/ΔTemp)	K,B,T		±1.2	ppm/°C max	
Zero Code (Offset) Error[1,2]	J,A,S	+1/4, −1/2	+1/2, −1/2	LSB max	
	K,B,T	+1/8, −1/2	+1/4, −1/2	LSB max	
Differential Nonlinearity[1,2]	All	±1/2	±1/2	LSB max	All grades guaranteed monotonic to 12 bits
					T_{min} to T_{max}.
Power Supply Rejection					
(Ratio ΔGain/ΔV_{DD})	All	±0.005	±0.01	% per % max	V_{DD} = +15.5V to +14.5V;
					all digital inputs HIGH
REFERENCE INPUT					
Input Resistance (pin 1)	All	4.7	4.7	kΩ min	Min input resistance is approximately 0.67 × R_{LADDER}.
Input Capacitance[3] (pin 1)	All	40	40	pF min	All digital inputs LOW
		100	100	pF max	All digital Inputs HIGH
DIGITAL INPUTS					
V_{INH}	All	2.4	2.4	V min	
V_{INL}	All	0.8	0.8	V max	
Input Leakage Current	All	±1	±1	μA max	V_{IN} = 0V or 15V.
Input Capacitance	All	8	8	pF max	
Input Coding		Binary			Can be configured for offset binary–see Figures 14 and 16.
ANALOG OUTPUT					
Output Capacitance[3] (pin 17)	All	2.8	2.8	pF max	
Output Resistance (pin 17)	All	7k	7k	Ω min	
		12k	12k	Ω typ	
		15k	15k	Ω max	
Output Resistance Tempco	All	−300	−300	ppm/°C typ	
R_{BIAS}	All	7k	7k	Ω min	
		12k	12k	Ω typ	
		15k	15k	Ω max	
R_{BIAS}–R_{LADDER} Match.	All	0.1	0.1	% typ	
DYNAMIC PERFORMANCE					
Propagation Delay[3,4]	All	100	100	ns max	Measured from 50% of digital input to 10%
					of final analog output.
Voltage Settling Time[3,4,5,6,7]	All	900	900	ns max	To 0.01% of FSR for all 0's to all 1's or all 1's to all 0's.
	J,K	550	550	ns typ	To 0.01% of FSR for all 0's to all 1's or all 1's to all 0's.
	J,K	470	470	ns typ	To 0.04% of FSR for all 0's to all 1's or all 1's to all 0's.
	J,K	400	400	ns typ	To 0.2% of FSR for all 0's to all 1's or all 1's to all 0's.
Glitch Energy[4]	All	45	45	nV secs typ	Around major carry transition.
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V_{min}/V_{max}	Accuracy is guaranteed at +15V ±5%.
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IH}.
I_{DD}	All	100	100	μA max	All digital inputs 0V or V_{DD}.

NOTES
[1]1LSB = V_{REF}/4096.
[2]DAC load $R_L > 10^{10}\Omega$.
[3]Guaranteed by design, not subject to test.
[4]Input logic levels 0 to 5V.
[5]Assuming a maximum external load capacitance of 2.8pF.
[6]Metal ceramic packages typically exhibit 20% higher inter-pin capacitance than plastic packages. Therefore metal ceramic devices typically exhibit settling times approximately 10% longer than plastic parts.
[7]FSR is full scale range.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . −0.3V, +17V
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD}
V_{BIAS}, V_{OUT} to DGND . . . . . ±25V
V_{REF} to DGND . . . . . −0.3V, V_{DD}
AGND to DGND . . . . . −0.3V, V_{DD}
Power Dissipation (Any Package) to 75°C 450mW
Derates above +75°C . . . . . 6mW/°C
Operating Temperature
Commercial . . . . . 0 to +70°C
Industrial . . . . . −25°C to +85°C
Military . . . . . −55°C to +125°C
Storage Temperature . . . . . +65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

SPECIFICATION DEFINITIONS

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes gain error, relative accuracy and zero code offset when configured as shown in Figure 11.

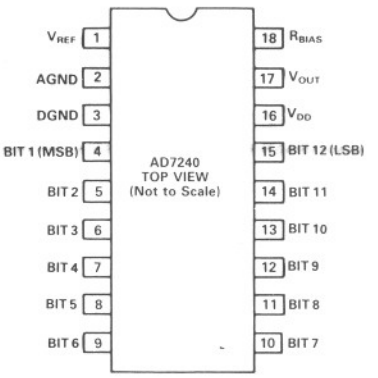
Absolute full scale is V_{REF} – 1LSB (IDEAL) where 1LSB (IDEAL) is $\frac{V_{REF}}{4096}$.

NOTE: "ERROR" defined is ACTUAL VALUE – IDEAL VALUE.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

PIN CONFIGURATION



ORDERING INFORMATION

Total Unadjusted Error	Plastic	Cerdip[1]	Side Brazed Ceramic
$T_A = T_{MIN}$ to T_{MAX}	0 to +70°C	−25°C to +85°C	−55°C to +125°C
+1/2, −2LSB	AD7240JN	AD7240AQ	AD7240SD
+1/4, −1 1/2LSB	AD7240KN	AD7240BQ	AD7240TD

NOTE
[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

Typical Performance Characteristics

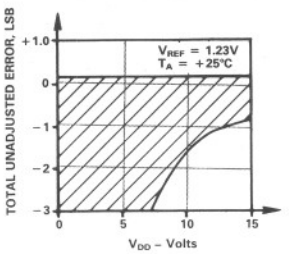


Figure 1. Total Error vs V_{DD} (Shaded Area Shows Typical Range of Total Unadjusted Error vs. Supply Voltage for AD7240JN)

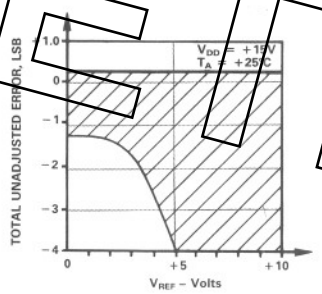


Figure 2. Total Error vs. Reference Voltage (Shaded Area Shows Range of Values of Total Unadjusted Error That Typically Occurs for AD7240JN)

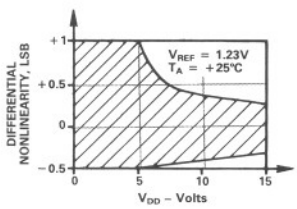


Figure 3. Differential Nonlinearity vs. V_{DD} (Shaded Area Shows Typical Range of DNL vs. Supply Voltage)

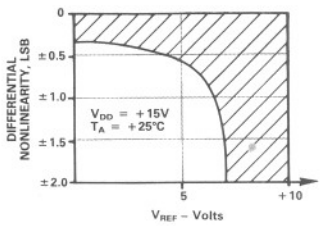


Figure 4. Differential Nonlinearity vs. Reference Voltage (Shaded Area Shows Range of Values of DNL That Typically Occur for K and J Grades)

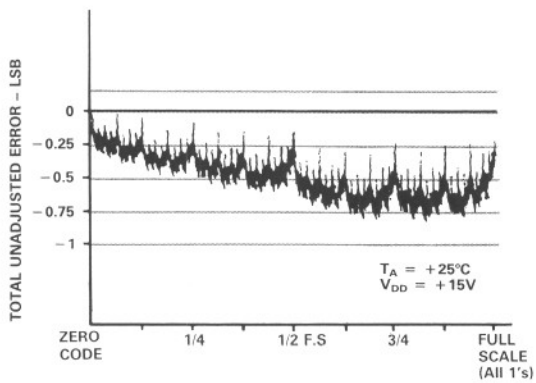


Figure 5. Total Unadjusted Error vs. Digital Code

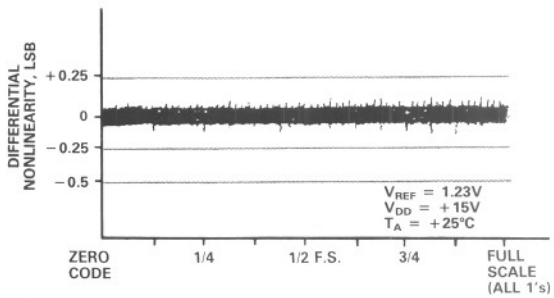


Figure 6. Differential Nonlinearity vs. Digital Code

CIRCUIT INFORMATION

ANALOG SECTION

The AD7240 12-bit voltage DAC consists of a highly stable thin film R-2R ladder and twelve high speed N MOS single pole double throw switches.

The AD7240 has low capacitance at the V_{OUT} terminal, and hence exhibits fast output voltage settling times.

The simplified circuit diagram of the D/A converter is shown in Figure 7.

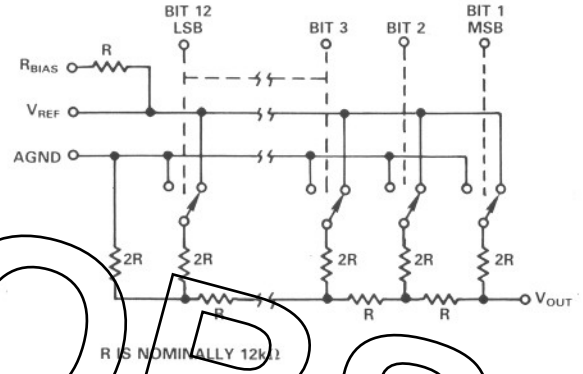


Figure 7. AD7240 Functional Diagram (Inputs High)

DIGITAL SECTION

The 12 digital inputs are designed to be both TTL and CMOS compatible when V_{DD} equals +15V. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from GND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and GND) as practically possible.

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

When operated in the voltage switching mode the AD7240 exhibits code independent (fixed) output capacitance and output resistance. This means that settling time of the AD7240 is virtually the same for all code changes when operated as per Figure 10.

In contrast, the output impedance and thus the settling time of current mode DACs is code dependent. Moreover, with a current mode CMOS DAC the large output capacitance places a limitation on the realizable settling time, even when using a fast output op amp.

The low values of output capacitance of the AD7240 ensure very fast voltage settling when configured with a high speed follower.

SETTLING TIME

The time taken for voltage settling of the AD7240 to less than 1/2LSB is given by the approximation:

*Settling Time	≃	$t_{pd} + 9R(C_{OUT} + C_{EXT})$
t_{pd}	–	Logic Propagation Delay
R	–	DAC Ladder Resistance
C_{OUT}	–	DAC Output Capacitance
C_{EXT}	–	Capacitance due to External Circuit.

*This approximation assumes very high load impedance.

Figure 8 shows the output voltage transient response waveform for the transition resulting when all digital inputs change from 0 volts to +5 volts.

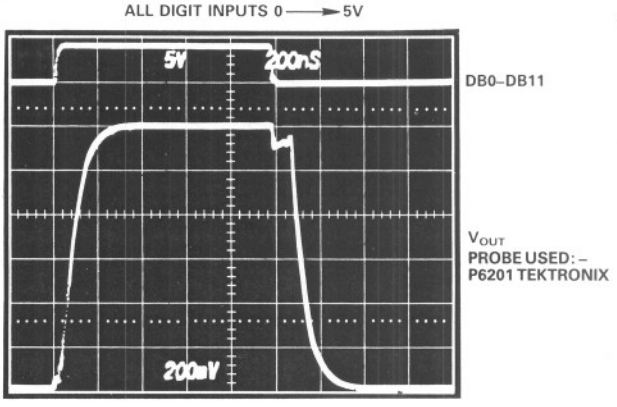


Figure 8. AD7240 Transient Response Waveform

Figure 9 shows the glitch energy waveform for the major transition. Figure 10 shows the circuit used to achieve the waveforms shown in Figures 8 and 9.

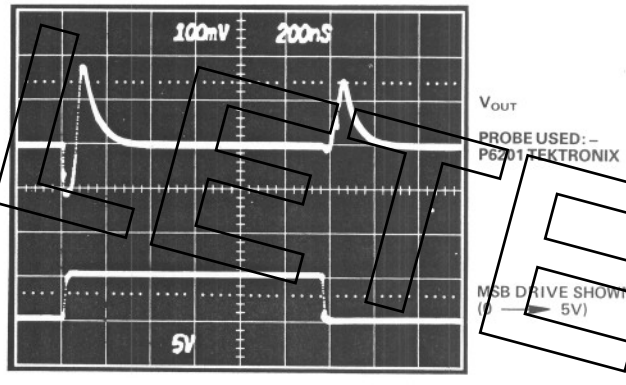


Figure 9. AD7240 – Major Transition Glitch

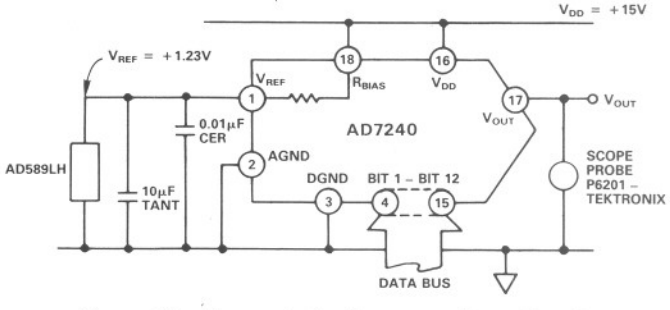


Figure 10. Dynamic Performance Test Circuit

VOLTAGE REFERENCE

The input impedance at the V_{REF} pin of the AD7240 is code dependent and can vary from 7K up to infinity. The nodal capacitance at the reference terminal is also code dependent and typically varies from 40pF to 90pF. Therefore it is essential that the reference be adequately decoupled at pin 1 of the AD7240 in order to present a low output impedance and thus maintain full accuracy under changing load conditions.

APPLICATION INFORMATION

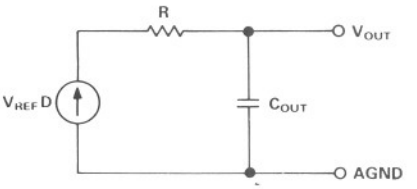
LOAD IMPEDANCE

The AD7240 equivalent output circuit of Figure 11 shows a Thevenin voltage source V_{REF} D with a fixed output resistance and capacitance of R and C_{OUT} respectively. D is a fractional representation of the digital input word N i.e. D = N/4096.

Resistive loading at pin 17 of the AD7240 causes scale factor error. Op amp bias current through the DAC output impedance (12kΩ nominal) introduces an offset term.

For example, a 60MΩ load resistance on pin 17 introduces a 1LSB scale factor error at pin 17. Op amp bias current of 25 nanoamps introduces a 1LSB offset term. Effects of amplifier bias current can be minimized by ensuring the parallel combination of R1 and R2 (Figure 12) is equal to the DAC's output impedance at pin 17 (nominally 12kΩ). If the amplifier circuit (of Figure 12) is configured to provide a gain of +1, resistor R2 should be included and should equal 12kΩ to minimize output error due to bias current.

Figure 11 shows the equivalent circuit of the output of the AD7240.



R – DAC LADDER RESISTANCE (12KΩ TYP)
C_{OUT} – DAC OUTPUT CAPACITANCE (2.8pF MAX)
V_{REF} D – THEVENIN VOLTAGE SOURCE (O < D < 4095/4096)

Figure 11. Equivalent Output Circuit of AD7240

AD7240 OPERATION MODES

The AD7240 can operate in several different modes. Each mode has its own particular characteristics. These are summarized below and discussed in detail in the paragraphs following.

SUMMARY OF OPERATION MODES

Mode	Performance Feature	Circuit Constraints
1. VOLTAGE SWITCHING (Figure 12)	• Single supply operation. • Positive V_{IN} gives Positive V_{OUT} • Reduced charge injection. • Constant output impedance. • Low output capacitance obviates need for extra op amp compensation thus reducing settling time.	• Code dependent input impedance requires well buffered reference voltage. • V_{IN} must never go negative. • For 12-bit linearity max V_{IN} range must be AGND < V_{IN} ≤ +2.0V
2. VOLTAGE SWITCHING WITH AGND BIAS VOLTAGE (Figure 13)	• Single supply operation with variable "zero" output level.	• Same as for 1.
3. VOLTAGE SWITCHING OFFSET BINARY (Figure 14)	• Bipolar Output • Same as 1.	• Needs DUAL rail power supply for op amp. • Same as for 1.
4. CURRENT STEERING (Figures 15 & 16)	• Four quadrant multiplication. • Good power supply rejection. • Low distortion • Constant input impedance at V_{REF} • 1ppm/°C typical gain tempco.	• Needs DUAL rail power supply for op amp. • Output op amp must have low input offset voltage to minimize "noise gain" effects on analog output.
5. CURRENT STEERING WITH AGND BIAS VOLTAGE (Figures 17 and 18)	• Single supply operation. • Four quadrant multiplication. • Good power supply rejection. • Low output leakage current.	• Need op amp with low input offset voltage to minimize "noise gain" effects.

AD7240 Operation Modes

1. VOLTAGE SWITCHING MODE

The circuit in Figure 12 shows the AD7240 connected in the voltage switching mode. Since V_{OUT} is the same polarity as V_{REF}, this configuration allows single supply operation. Note that the voltage V_{REF} must always be positive with respect to DGND in order to prevent parasitic transistor turn-on.

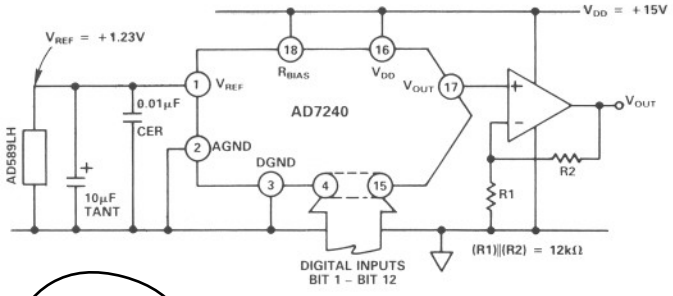


Figure 12. AD7240 in Single Supply Voltage Switching Mode

To maintain linearity, the voltages at V_{REF} and AGND should remain within 2.0 volts of each other for a V_{DD} of +15 volts. If V_{DD} is reduced from 15V or the differential voltage between V_{REF} and AGND is increased to more than 2.0 volts, the accuracy of the DAC will be degraded. Figures 1 and 2 show typical curves illustrating this effect for various values of reference voltage and V_{DD}. A suitable reference for this configuration is the AD589HL – a two terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage. The bandgap reference is conveniently biased by connecting the R_{BIAS} pin to the positive supply. However due to the internal V_{REF} bond wire resistance, the AD589 bias current develops an error voltage which appears in series with the reference voltage on pin 1. This error voltage (0.5 LSB's typ) acts to shift the Total Unadjusted Error plot of Figure 5 in a positive direction. Therefore, R_{BIAS} should only be used in applications which can accommodate this shift, otherwise use an external bias resistor and tie pin 18 to pin 2 (as shown in Figure 14).

Note that the output voltage range has been extended by using a noninverting gain stage.

The output voltage V_{OUT} is expressed as:

$$V_{OUT} = (V_{REF})(D)\left(\frac{R_1 + R_2}{R_2}\right)$$

Where D is a fractional representation of the digital input word ($0 \leq D \leq 4095/4096$).

Fastest settling can be achieved by using dual supply op amp.

2. VOLTAGE SWITCHING MODE WITH AGND BIAS VOLTAGE

AGND can be biased above DGND to provide an offset "zero" analog output voltage level. Figure 13 shows this circuit configuration. Note that the output voltage range has been extended by using a noninverting gain stage to buffer the DAC.

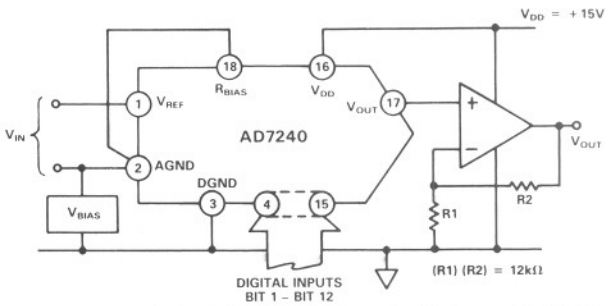


Figure 13. AD7240 in Single Supply Voltage Switching Mode with AGND Bias Voltage

The output voltage V_{OUT} is expressed as:

$$V_{OUT} = (V_{BIAS})\left(\frac{R_1 + R_2}{R_1}\right) + (V_{IN})(D)\left(\frac{R_1 + R_2}{R_1}\right)$$

Where $V_{IN} \leq +2.0V$, and where D is a fractional representation of the digital input word ($0 \leq D \leq 4095/4096$).

The effect of V_{BIAS} on total unadjusted error and differential nonlinearity will be the same as reducing V_{DD} by the amount of the offset (see Figures 1 and 3).

3. VOLTAGE SWITCHING MODE – OFFSET BINARY OPERATION

Figure 14 shows a circuit used to implement offset binary coding in the voltage switching mode. Mismatch between R1 and R2 causes both offset and full scale error, therefore, these resistors must match (to within 0.01%) and track over temperature.

Table I shows the digital code vs output voltage relationship for Figure 14.

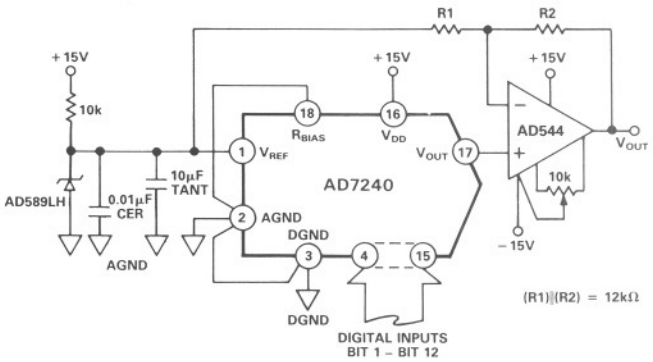


Figure 14. AD7240 in Offset-Binary Voltage-Switching Mode

Digital Input	Analog Output
1111 1111 1111	$+V_{REF}\left\{\frac{2047}{2048}\right\}$
1000 0000 0000	0V
0000 0000 0000	$-V_{REF}$

Table I. Offset Binary Code Table for Figure 14 with R1 = R2

4. CURRENT STEERING MODE

Unipolar Operation (2 Quadrant Multiplication)

The circuit in Figure 15 shows the AD7240 connected in the current steering mode with a unipolar voltage output. In this configuration R_{BIAS} is used as the feedback resistor providing a typical gain error of ±4LSBs. Typical gain T.C. in this mode is 1ppm/°C. Resistors R1 and R2 have been included to allow gain trimming. See Reference 2 for additional information.

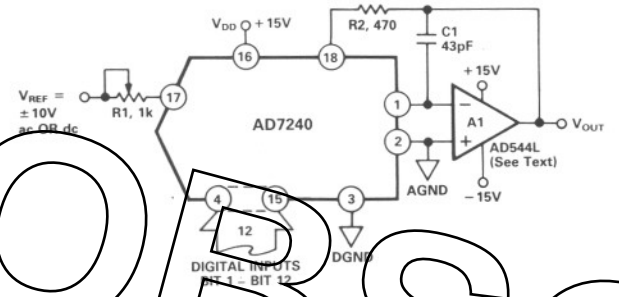


Figure 15. Unipolar Binary Operation (2-Quadrant Multiplication)

Capacitor C1 provides phase compensation and helps to prevent overshoot and ringing when using high speed op amps. Note that the circuit has a constant input impedance of R_{LADDER} at pin 17. V_{REF} can be a fixed dc voltage or an ac signal or a fixed dc or ac current. Table II shows the digital code vs. output voltage relationship for Figure 15.

Digital Input	Analog Output
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\,V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table II. Unipolar Binary Code Table for Circuit of Figure 15

Bipolar Operation (4 Quadrant Multiplication)

Figure 16 and Table III illustrate the recommended circuit and code relationship for Bipolar Operation in the current steering mode. The D/A function itself uses offset binary code. An inverter can be connected to the MSB line to convert offset binary input code to 2's complement code. R3, R4 and R5 must be selected to match within 0.01% and they should have the same temperature coefficients.

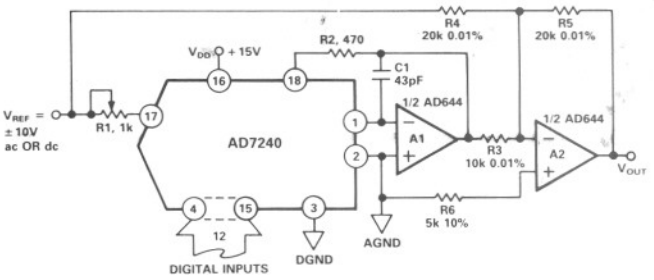


Figure 16. Bipolar Operation (4 Quadrant) Offset Binary Code

Digital Input	Analog Output
1111 1111 1111	$+V_{REF}\cdot\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\cdot\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\cdot\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\cdot\left(\frac{2048}{2048}\right)$

Table III. Offset Binary Table for Circuit of Figure 16

In the current steering mode, the AD7240 has a code dependent output resistance which in turn can cause a code dependent error voltage or "noise gain" at the output of amplifier A1. The maximum amplitude of this error voltage, which adds to the D/A converter nonlinearity, depends on V_{OS} where V_{OS} is the amplifier input offset voltage (Ref 1). To maintain monotonic operation it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation.

5. CURRENT STEERING MODE WITH AGND BIAS VOLTAGE

The AD7240 has been designed so that AGND (pin 2) can be biased to any voltage between DGND and (V_{DD} – 10V). V_{DD} must be kept at least 10V above V_{REF} to ensure that monotonicity is preserved. This feature allows single supply operation in the current steering mode. Figure 17 shows the basic circuit configuration. The AD584 pin programmable reference fixes AGND at +5.0V. The output voltage swing is from +5V to +10V allowing operation from a single +15V power supply.

The output voltage V_{OUT} is

$$V_{OUT} = V_{BIAS} + (D)(V_{BIAS})$$

Where D is a fractional representation of the digital input word ($0 \leq D \leq 4095/4096$).

The circuit of Figure 17 can be modified to allow any full scale range to be chosen. Figure 18 shows the circuit modified to provide an output range of ±2.5V about a "pseudo-analog ground" of +5V i.e. from +2.5V to 7.5V.

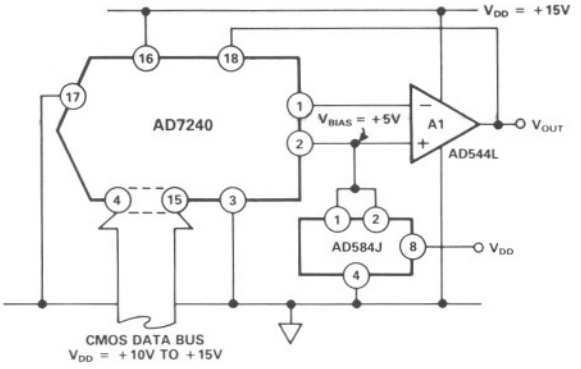


Figure 17. AD7240 in Single Supply Current Steering Mode with AGND Bias Voltage

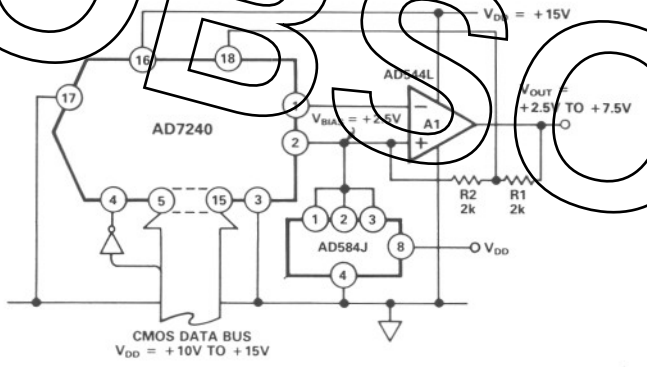


Figure 18. AD7240 in Single Supply Current Steering Mode with AGND Bias Voltage and Gain Resistors (2's Complement Coding)

This voltage range allows operation from a single +10V to +15V power supply. The AD584 pin programmable reference now fixes AGND at +2.5V.

The output voltage V_{OUT} is

$$V_{OUT} = \left(\frac{R_1 + R_2}{R_2}\right)(D)(V_{BIAS}) + (V_{BIAS})$$

Where D is a fractional representation of the digital input word at the DAC ($0 \leq D \leq 4095/4096$).

REFERENCE MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

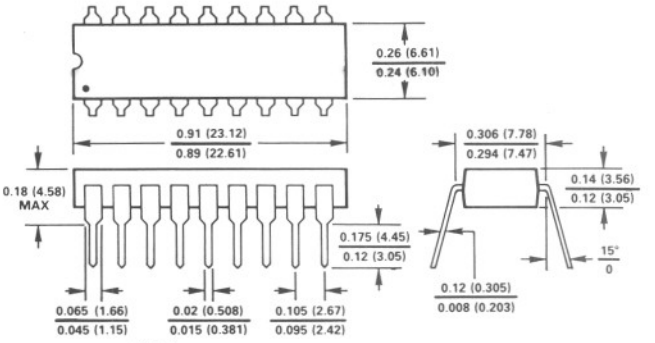
1. Applications Guide to CMOS Multiplying D/A Converters available from Analog Devices, Publication Number G479.
2. Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs – Application Note, Publication Number E630–10–6/81 available from Analog Devices.
3. Analog-Digital Conversion Notes – available from Analog Devices, price $5.95.
4. "Input Resistor Stabilizes MDAC's Gain" – Paul Brokaw, EDN January 7th, 1981; – not available from Analog Devices.

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

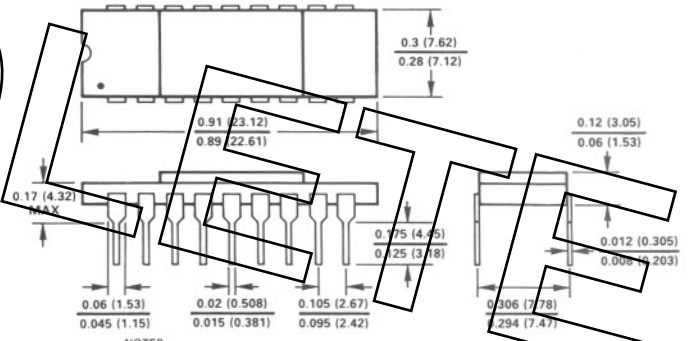
Dimensions shown in inches and (mm).

18-PIN PLASTIC DIP – SUFFIX N



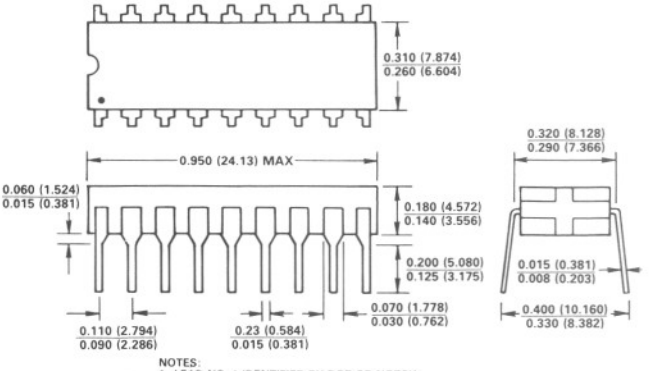
NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

18-PIN CERAMIC DIP – SUFFIX D



NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

18-PIN CERDIP – SUFFIX Q



NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.