

FAST CMOS QUAD 2-INPUT MULTIPLEXER

IDT74FCT257AT/CT/DT OBSOLETE PART

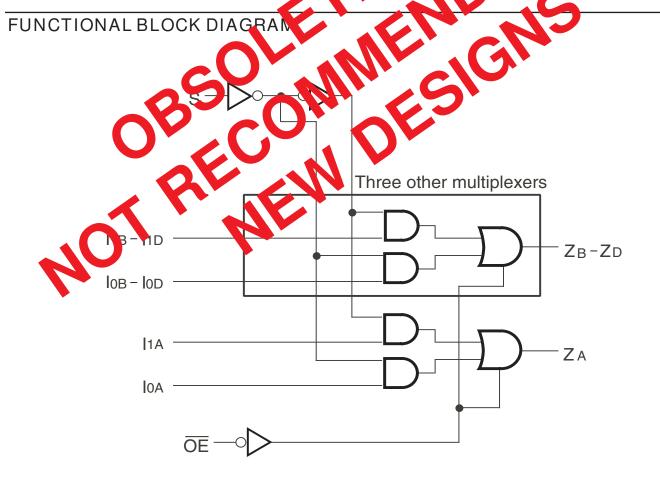
FEATURES:

- · A, C, and D grades
- Low input and output leakage ≤1µA (max.)
- · CMOS power levels
- True TTL input and output compatibility:
 - VOH = 3.3V (typ.)
 - -VOL = 0.3V (typ.)
- High Drive outputs (-15mA IOH, 48mA IOL)
- · Meets or exceeds JEDEC standard 18 specifications
- · Power off disable outputs permit "live insertion"
- · Available in SOIC and QSOP packages

DESCRIPTION:

The FCT257T is a high-speed quad 2-input multiplexer built using an advanced dual metal CMOS technology. Four bits of data from two sources can be selected using the common select input. The four buffered outputs present the selected data in the true (non-inverting) form.

The FCT257T has a common Output Enable (\overline{OE}) in the When \overline{OE} is high, all outputs are switched to a high-impedance state. Flow by the outputs to interface directly with the coriented systems.

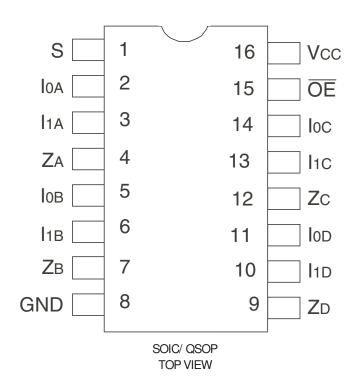


INDUSTRIAL TEMPERATURE RANGE

SEPTEMBER 2009



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
Tstg	Storage Temperature	-65 to +150	°C
Іоит	DC Output Current	-60 to +120	mA

NOTES:

- 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- 2. Inputs and Vcc terminals only.
- 3. Output and I/O terminals only.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Тур.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	рF
Соит	Output Capacitance	Vout = 0V	8	12	рF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description		
Ioa-Iod	Source 0 Data Inputs		
l1A-l1D	Source 1 Data Inputs		
ŌĒ	Output Enable (Active LOW)		
S	Select Input		
ZA-ZD	Outputs		

FUNCTION TABLE(1)

	Inp			
ŌĒ	S	lo	l1	Output Zx
Н	Х	Х	X	Z
L	Н	Х	L	L
L	Н	Х	Н	Н
L	L	L	Х	L
L	L	Н	Х	Н

NOTE:

- 1. H = HIGH Voltage Level
 - L = LOW Voltage Level
 - X = Don't Care
 - Z = High-Impedance



IDT74FCT257AT/CT/DT FASTCMOS QUAD 2-INPUT MULTIPLEXER

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: TA = -40°C to +85°C, $VCC = 5.0V \pm 5\%$

Symbol	Parameter	Test Condit	ions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level		2	_	_	V
VIL	Input LOW Level	Guaranteed Logic LOW Level		_	_	0.8	V
Iн	Input HIGH Current ⁽⁴⁾	Vcc = Max.	VI = 2.7V	_	_	±1	μΑ
lıL	Input LOW Current ⁽⁴⁾	Vcc = Max.	VI = 0.5V	_	_	±1	μΑ
lozh	High Impedance Output Current	Vcc = Max	Vcc = Max Vo = 2.7V		_	±1	μΑ
lozL	(3-State output pins) ⁽⁴⁾	Vo = 0.5V		_	_	±1	
lı	Input HIGH Current ⁽⁴⁾	Vcc = Max., VI = Vcc (Max.)	Vcc = Max., VI = Vcc (Max.)		_	±1	μΑ
VIK	Clamp Diode Voltage	VCC = Min, I _{IN} = -18mA		_	-0.7	-1.2	V
VH	Input Hysteresis	1		_	200		mV
Icc	Quiescent Power Supply Current	Vcc = Max., Vin = GND or Vcc		_	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
Vон	Output HIGH Voltage	Vcc = Min	IOH = -8mA	2.4	3.3		٧
		VIN = VIH or VIL	IOH = -15mA	2	3	_	
Vol	Output LOW Voltage	Vcc = Min IoL = 48mA		_	0.3	0.5	٧
		VIN = VIH or VIL					
los	Short Circuit Current	$Vcc = Max., Vo = GND^{(3)}$		-60	-120	-225	mA
loff	Input/Output Power Off Leakage ⁽⁵⁾	Vcc = 0V, Vin or Vo ≤ 4.5V	_	_	±1	μΑ	

NOTES:

- 1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- 2. Typical values are at Vcc = 5.0V, +25°C ambient.
- 3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- 4. The test limit for this parameter is $\pm 5\mu A$ at $T_A = -55^{\circ} C$.
- 5. This parameter is guaranteed but not tested.



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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Condition	ons ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
Δlcc	Quiescent Power Supply Current TTL Inputs HIGH	$Vcc = Max.$ $Vin = 3.4V^{(3)}$		_	0.5	2	mA
ICCD	Dynamic Power Supply Current ⁽⁴⁾	Vcc = Max. Outputs Open OE = GND One Input Toggling 50% Duty Cycle	VIN = VCC VIN = GND	_	0.15	0.25	mA/ MHz
IC	Total Power Supply Current ⁽⁶⁾	Vcc = Max. Outputs Open fo = 10MHz	VIN = VCC VIN = GND	_	1.5	3.5	mA
		$\frac{50\%}{OE}$ Duty Cycle ${OE}$ = GND One Bit Toggling	VIN = 3.4V VIN = GND	_	1.8	4.5	
		Vcc = Max. Outputs Open fo = 2.5MHz	VIN = VCC VIN = GND	_	1.5	3.5 ⁽⁵⁾	
		50% Duty Cycle OE = GND Four Bits Toggling	VIN = 3.4V VIN = GND	_	2.5	7.5 ⁽⁵⁾	

NOTES:

- 1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- 2. Typical values are at Vcc = 5.0V, $+25^{\circ}C$ ambient.
- 3. Per TTL driven input; (VIN = 3.4V). All other inputs at Vcc or GND.
- 4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- 5. Values for these conditions are examples of Δlcc formula. These limits are guaranteed but not tested.
- 6. IC = IQUIESCENT + INPUTS + IDYNAMIC
 - $IC = ICC + \Delta ICC DHNT + ICCD (foNo)$

Icc = Quiescent Current

 Δlcc = Power Supply Current for a TTL High Input (Vin = 3.4V)

DH = Duty Cycle for TTL Inputs High

NT = Number of TTL Inputs at DH

ICCD = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

fo = Output Frequency

No = Number of Outputs at fo

All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

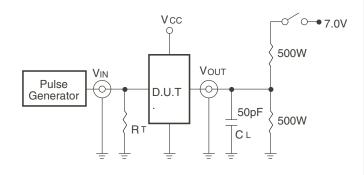
			FCT257AT		FCT2	75CT	FCT2	75DT	
Symbol	Parameter	Condition ⁽¹⁾	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Unit
tPLH	Propagation Delay	CL = 50pF	1.5	5	1.5	4.3	1.5	3.9	ns
tPHL	Ix to Zx	$RL = 500\Omega$							
tPLH	Propagation Delay		1.5	7	1.5	5.2	1.5	4.4	ns
tPHL	S to Zx								
tPZH	Output Enable Time		1.5	7	1.5	6	1.5	4.4	ns
tPZL									
tPHZ	Output Disable Time		1.5	5.5	1.5	5	1.5	4.4	ns
tPLZ									

NOTES:

- 1. See test circuit and waveforms.
- 2. Minimum limits are guaranteed but not tested on Propagation Delays.

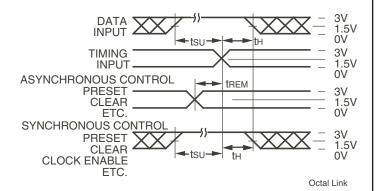


TEST CIRCUITS AND WAVEFORMS

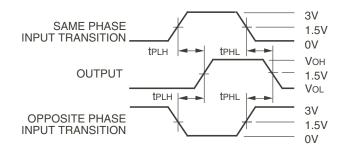


Test Circuits for All Outputs

Octal Link



Set-Up, Hold, and Release Times



Propagation Delay

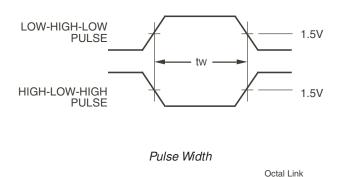
SWITCH POSITION

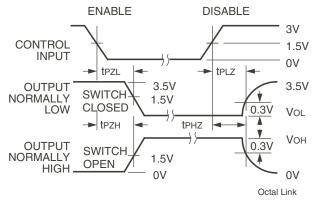
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.





Enable and Disable Times

NOTES:

- 1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- 2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; tF \leq 2.5ns; tR \leq 2.5ns.

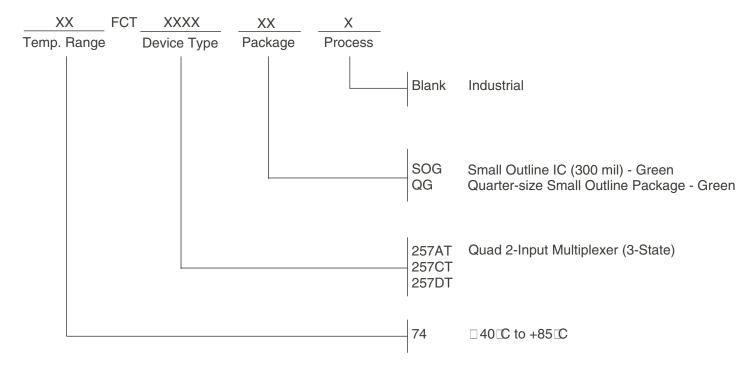
Octal Link



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ORDERING INFORMATION

FASTCMOS QUAD 2-INPUT MULTIPLEXER



Datasheet Document History

09/29/2009 Pg. 6 Updated the ordering information by removing the "IDT" notation and non RoHS part.

PDN# CQ-15-04 issued. See IDT.com for PDN specifics. 08/14/2015

09/03/2019 Datasheet changed to Obsolete Status.

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