TEXAS INSTRUMENTS

DAC1220EVM

Evaluation Module

User's Guide

August 2004

Data Acquisition Products

SBAU102

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It is important to operate this EVM within the specified input and output ranges of 0V to 5V that are described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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Preface

Read This First

About This Manual

This manual describes the DAC1220EVM evaluation fixture and how to use it. Throughout this document, the abbreviation EVM and the term *evaluation module* are synonymous with the DAC1220EVM.

Related Documentation From Texas Instruments

The following documents provide information regarding Texas Instruments integrated circuits used in the assembly of the DAC1220EVM. These documents are available from the TI web site, and are current at the time of the writing of this User's Guide. To obtain a copy of the following TI documents, visit our website at http://www.ti.com/ or call the Texas Instruments Literature Response Center at (800) 477−8924 or the Product Information Center at (972) 644−5580. When ordering, identify the document by both title and literature number.

Data sheet	Literature number
DAC1220 Data Sheet	SBAS273
REF1004 Data Sheet	SBVS002
OPA335 Data Sheet	SBOS245
OPA350 Data Sheet	SBOS099
SN74LVC1G80 Data Sheet	SCES221

Additional Documentation

The following document provides information regarding selected non-TI components, which may be used in the testing of the DAC1220EVM. This document is available from the corresponding manufacturer.

Document	Manufacturer
HPA449 User's Guide	SoftBaugh, http://www.softbaugh.com

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If you have questions regarding either the use of this evaluation module or the information contained in the accompanying documentation, please contact the Texas Instruments Product Information Center at (972) 644−5580 or visit the TI web site at www.ti.com.

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Chapter 1

Overview

The DAC1220EVM is an evaluation fixture designed for the DAC1220 20-bit delta-sigma ($\Delta\Sigma$) digital-to-analog data converter. The EVM is designed for prototyping and evaluation, and includes a reference circuit, an oscillator circuit, and an output buffer amplifier. Use of the output buffer amplifier is optional.

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1.1 Introduction

Many data converter evaluation fixtures contain a computer interface or a microcontroller, but the DAC1220EVM contains only the DAC1220 device and a few supporting components. All DAC1220 pins are accessible through various pins on the analog and digital connectors of the DAC1220EVM.

The DAC1220EVM is designed using a simple card format developed by TI. This simple, consistent design makes the DAC1220EVM very easy to connect to your own prototype system. One can even think of the DAC1220EVM as an alternate package for the DAC1220—one much larger than the device itself, but also much easier to wire up by hand on a test bench.

The DAC1220EVM can be plugged directly into suitable motherboards, such as the HPA449 MSP430 microcontroller development system from SoftBaugh, Inc. (http://www.softbaugh.com). See also TI's web site for example code using the DAC1220EVM with the HPA449.

The DAC1220EVM, together with the HPA449 and the appropriate software, also forms a complete evaluation system for verifying the DAC1220 performance. See the Texas Instruments web site for additional information and software.

1.2 Built-In Accessories

The DAC1220EVM includes a system clock generator and a low-noise voltage reference. Using either of these components is optional; you can select an external system clock and/or an external reference, using the slide switches on the EVM.

The +2.5V reference circuit is based on a REF1004-2.5 voltage reference. Its noise performance is sufficient to allow the DAC1220 to perform at its lowest noise level.

The on-board clock circuit uses a 2.4576MHz crystal. A switch selects between the crystal and an external clock signal applied to the TOUT pin of the serial connector, J2.

1.3 Connectors

The DAC1220 device on the DAC1220EVM is connected through three headers: the analog connector, the serial connector, and the power connector. Pinouts and locations of each connector are given in Chapter 3 of this user's guide.

The analog connector (J1) carries analog I/O. The DAC1220 output appears in buffered and unbuffered versions on this connector. An external voltage reference can be applied to the VREF pins.

The serial connector, J2, carries the DAC1220 serial digital interface, an optional external system clock signal, and an I^2C™ connection to the on-board serial EEPROM.

The power connector (J4) carries the power supplies. The DAC1220EVM requires a +5V supply. The board is designed using a single ground net connected to DGND. An AGND pin is also provided and can be connected to DGND using jumper J5.

The DAC1220 uses separate supplies for its analog and digital sections. A jumper is inserted in each supply line. These jumpers allow the current of each supply to be measured independently.

1.4 Controls

The DAC1220EVM is configured using two slide switches. (See Figure 3−7 for the location of these switches.)

Switch S2 selects the system clock source for the DAC1220. You can select from the 2.4576MHz crystal or an external clock.

Switch S2 selects the reference input. One position selects the external reference input pins on the analog connector (J1); the other position selects the on-board +2.5V reference.

1.5 Setting Up

The way that one configures the DAC1220EVM depends on how it will be used. Consequently, there is no one single procedure to follow for setting up the DAC1220EVM.

Nevertheless, it is useful to remember the following points when you are configuring the board:

- ❑ Make certain that you have a +5V power supply connected to the proper pins on the power connector, J4.
- ❑ If you are not measuring the DAC1220 supply current, remember to place shunts on jumper block J3. Without these shunts, the DAC1220 will not be powered on, and will not work at all.
- ❑ Unless you are using two entirely separate power supplies for analog and digital sources, place a shorting block on jumper J2. This jumper connects the analog and digital supplies together, which is the usual method of operating the DAC1220.
- ❑ Check the system clock switch. If the switch is set to EXT, and you have not connected a clock signal to the external clock input pin on J2 (TOUT), the DAC1220 will not operate.

Chapter 2

Circuit Description

This chapter describes the DAC1220EVM circuit design in detail.

The DAC1220EVM is designed to conform to TI's Modular EVM System. It contains only those parts of the circuit that will typically be used in an application immediately surrounding the DAC1220EVM. This includes:

- ❏ The DAC1220 and associated components
- ❏ An output buffer amplifier
- ❏ A +2.5V voltage reference
- ❏ A 2.4576MHz crystal
- ❏ Controls and I/O connectors

Each of these items is described in detail in this chapter, with the exception of the controls and connectors, which are described in Chapter 3.

The layout of a circuit incorporating the DAC1220 is critical. The layout used on the DAC1220EVM is briefly described in Section 2.5.

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2.1 DAC1220 and Ancillary Components

The DAC1220 requires the following elements in order to operate properly:

- ❑ Filter capacitors
- ❑ Clock source
- ❑ Voltage reference
- ❑ Power connections and bypassing

The output filter capacitors and power connections are described in the following two subsections.

2.1.1 Filter Capacitors

The filter capacitors determine the frequency response of the reconstruction filter in the DAC1220. The selected capacitor values depend on the desired resolution. For 16-bit resolution, smaller capacitors are used; these give a faster settling time at the expense of higher noise. For 20-bit resolution, larger capacitors are used; these give a slower settling time but generate lower noise.

The DAC1220EVM is shipped with the recommended capacitor values for 20-bit mode as given in the product data sheet. If 16-bit operation is desired, the capacitors can easily be removed and replaced because they are mounted to large (0805) surface-mount footprints.

The capacitors are not jumpered or switched due to the high sensitivity of the filter input nodes. This high sensitivity is also the reason that surface-mount capacitors are used instead of through-hole capacitors.

The capacitor type is also a factor. High-quality film capacitors having very low voltage coefficient have been chosen for this EVM. This selection is important for noise and INL performance.

2.1.2 Power

The DAC1220 must be well-bypassed to prevent its digital currents from causing ground bounce. On the DAC1220EVM, 10 multi-layer ceramic capacitors bypass both the AVDD and DVDD pins. These capacitors are placed ahead of the jumpers as close to the device as possible.

Layout is also a critical factor with regard to power supply; see Section 2.5 for details.

2.2 Clock Oscillator

The DAC1220EVM can be used with its on-board 2.4576MHz crystal or with an external clock source. A commonly-available crystal type in a through-hole HC49 package was used.

Selector switch S2 is inserted between the crystal and the DAC. The double-pole switch disconnects the crystal from the device entirely, to better simulate actual application conditions when using an external clock.

As with any CMOS Pierce crystal oscillator circuit, load capacitance is critical. On the DAC1220EVM, slightly lower load capacitor values are used to compensate for the added parasitic capacitance incurred by the switch and longer trace distance between the DAC and the crystal.

2.3 Voltage Reference

The voltage reference circuit is based on the Burr-Brown REF1004-2.5 voltage reference. This device offers low cost, low power consumption, and a relatively uniform noise characteristic well-suited to the DAC1220.

The reference input of the DAC1220 is somewhat demanding, so the REF1004-2.5 is buffered by an OPA350. The output of this is filtered by the large filter capacitor at the amplifier output for low noise. For even lower noise, a tantalum capacitor can be installed at C4.

An external reference voltage can be switched in using switch S1.

2.4 Output Buffer Amplifier

Although the DAC1220 incorporates an on-board amplifier, this is mainly designed as part of the DAC1220 continuous-time reconstruction filter, and has a relatively weak output drive capability. For some loads, a buffer is needed.

The buffer used on the DAC1220EVM is a unity-gain connected OPA335. This device, which is also used in the voltage reference circuit, offers extremely low voltage drift thanks to its auto-zeroing circuit.

Unfortunately, the OPA335 is not rail-to-rail; input voltages over approximately 4.2V cause the device output to swing to the positive supply rail. Although the DAC1220 does not have enough output drive to damage the OPA335, it may be helpful to apply a lower external reference voltage when using the buffer; for example, 2V.

2.5 Layout

The DAC1220EVM employs a two-layer printed circuit board (PCB). This was done to show the possibility of achieving maximum performance for the DAC1220 even on a low-cost PCB.

However, achieving good performance is not accidental. The DAC1220 combines fast digital and precision analog circuitry. The digital circuitry must be prevented from affecting the analog section. The primary enemy is ground current: a sufficient current passing by the appropriate point around the DAC1220 can cause a voltage jump that can appear on the output. Since CMOS circuitry operates using large switching and small quiescent currents, it is particularly prone to causing this phenomenon.

To mitigate this possible interference, large bypassing capacitors are employed at the AVDD and DVDD pins; *snubber* resistors are inserted in the digital lines to reduce the edge speeds of the control signals, and so spread out the current spike; and the layout is designed to give return currents easy paths to their sources, which avoid the sensitive parts of the DAC1220.

The DAC1220 has two extremely sensitive nodes, where the filter capacitors are connected. These pins are surrounded on the top layer by a polygon-fill connected to the voltage reference. This guard plane helps keep high-frequency interference from entering these sensitive nodes.

Chapter 3

Usage

This chapter describes how to use the DAC1220EVM. It also describes the switches, jumpers, and connectors on the EVM in detail.

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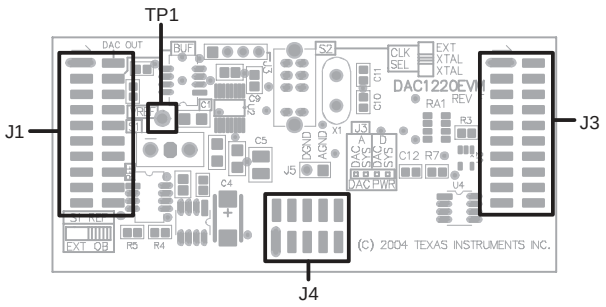
3.1 I/O Connectors and Testpoints

The positions and functions of the connectors and testpoints are shown in Figure 3−1.

Figure 3−1. DAC1220EVM Connectors and Testpoints



Many of the pins on the connectors are not used. On the pinout diagrams in this user's guide, unused pins are not marked. In the pin description tables, unused pins are not listed, and ground pins are listed together, with the exception of the power connector.

J1, J2, and J4 are each treated as a single connector in the schematic and in this user's guide, but they are actually mounted as connector pairs in a pass-through configuration. Each pair has a male surface-mount header on the top (component) side of the board, and a corresponding female surface-mount socket on the bottom (solder) side of the board. On the board itself, the headers mounted on top are suffixed ***A***, and the sockets mounted on the bottom are suffixed ***B***.

In the schematic, the connector pairs are shown as one symbol. For J1, J2, and J4, all bottom-side pins connected to their corresponding top-side pins; for example, J1B pin 1 connects to J1A pin 1, J1B pin 2 connects to J1A pin 2, etc. This convention holds for every pin on connectors J1, J2, and J4.

In all descriptions, connector pairs are treated as a single connector.

3.1.1 J1: Analog Connector

The analog connector pinout is shown in Figure 3−2 and described in Table 3−1.

Figure 3−2. Analog Connector Pinout for the DAC1220EVM

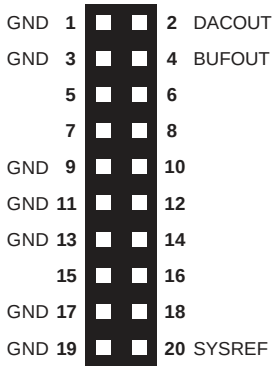


Table 3−1. Analog Connector Pin Descriptions for the DAC1220EVM

Pin No.	Pin Name	Standard Name	Direction	Function	Connection to DAC1220
1	AN0−	AN0−	Output	Signal ground for unbuffered output	Ground
2	AN0+	AN0+	Output	Unbuffered output	Direct
3	AN1−	AN1−	Output	Signal ground for buffered output	Ground
4	AN1+	AN1+	Output	Buffered output	Through buffer
20	SYSREF	REF+	Input	External reference input	n/a

3.1.2 J2: Serial Connector

The serial connector pinout is shown in Figure 3−3 and described in Table 3−2.

Figure 3−3. Serial Connector Pinout for the DAC1220EVM

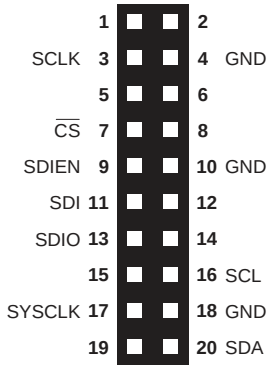


Table 3−2. Serial Connector Pin Descriptions for the DAC1220EVM

Pin Number	Pin Name	Standard Name	Direction	Function
3	SCLK	CLKX	Input	SPI clock
7	CS	FSX	Input	Chip select (Active low)
9	SDIEN	FSR	Input	Driver enable
11	SDI	DX	Input	SPI data in (MOSI)
13	SDIO	DR	I/O	SPI data in/out
17	SYSCLK	TOUT	Input	External clock input
16	SCL	SCL	I/O	I^2C clock
18	SDA	SDA	I/O	I^2C data
4, 10, 18	GND	DGND	Power	Ground

The DAC1220 serial interface is a bidirectional variant of SPI™. It uses an input clock, SCLK, and a bidirectional data line called SDIO.

Most SPI controllers do not have a bidirectional data line; they have an output line, typically called SDO, MOSI, or MISO, and an input line, typically called SDI, MISO, or SOMI. To more easily support these interfaces, the DAC1220EVM includes a tristate buffer connected to the serial connector input line. The buffer can be enabled and disabled using pin 9 on the serial connector; a low on this line activates the buffer.

If you use an SPI interface, set this line low before writing data to the DAC1220EVM, and high when receiving data from the DAC1220EVM. Be certain to only activate the line when the DAC1220 is not sending data. However, the 100Ω resistor in the SDIO line should prevent excessive current consumption during driver contention.

The interface can easily be bit-banged. To bit-bang in bidirectional mode, fix pin 9 high, and use only the DR pin for both transmit and receive.

SCL and SDA are used to communicate with the I^2C serial EEPROM.

3.1.3 J4: Power Connector

The power connector pinout is shown in Figure 3−4 and described in Table 3−3

Figure 3−4. Power Connector Pinout for the DAC1220EVM

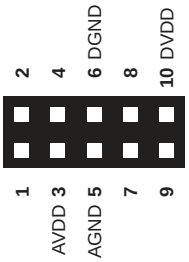


Table 3−3. Power Connector Pin Descriptions for the DAC1220EVM

Pin Number	Pin Name	Standard Name	Function
3	AVDD	+5VA	Analog power supply
5	GND	AGND	Analog/main ground
6	DGND	DGND	Digital ground from motherboard
10	DVDD	+5VD	Digital power supply

The DAC1220 has separate analog and digital power supply connections. Both supplies must be +5V. The motherboard must supply both voltages; however, both may (and usually do) come from the same source.

The DAC1220 has separate analog and digital ground connections for internal layout reasons; the DAC1220EVM uses a single ground plane. The motherboard may have separate ground domains on AGND and DGND. The DAC1220EVM takes its ground connection from AGND. You can connect DGND to AGND on the DAC1220EVM using jumper J5, as described in section 3.2.2.

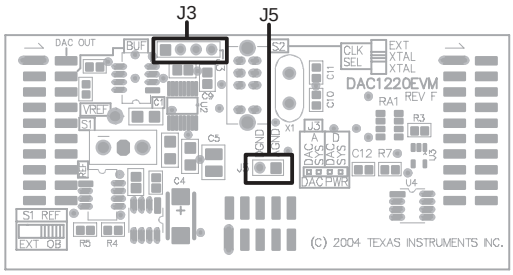
3.1.4 Testpoints

There is one testpoint on the board; it is marked TP1. The testpoint is connected to the DAC1220 VREF input. This testpoint is positioned very near the chip VREF input, which allows its reference to be measured with good accuracy. This is useful for calibration purposes.

3.2 Jumpers

The jumpers are shown in Figure 3−5.

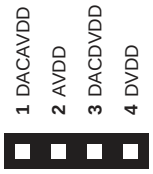
Figure 3−5. DAC1220EVM Jumpers



3.2.1 J3: DAC1220 Supply Current Measurement Jumpers

Jumper block J3 is shown in Figure 3−6.

Figure 3−6. Jumper Block J3 on the DAC1220EVM



This jumper block can be used to measure the current drawn by the DAC1220 power supplies.

For normal operation, when not measuring current, place shorting blocks across both jumper positions in the block.

3.2.2 J5: DAC1220 Analog-Digital Ground Shorting Jumpers

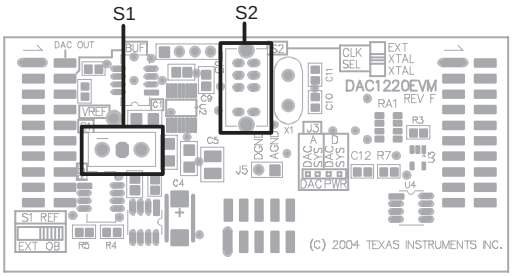
This jumper is used to connect the analog and digital grounds together.

If you are using a single power supply, you should usually place a shorting block across this jumper. If you are using two different supplies (each with its own ground), you should usually leave this jumper unconnected.

3.3 Switches

The positions and functions of the switches are shown in Figure 3−7.

Figure 3−7. DAC1220EVM Switches



3.3.1 S1: Reference Input Select

S1 selects between the DAC1220EVM onboard +2.5V reference and an external reference voltage provided on J1 pin 20 (SYSREF). The left position of the switch selects the external reference, and the right position selects the onboard reference.

The DAC1220EVM uses a single-ended reference voltage; J1, pin 18 is not connected.

The external reference is filtered on board with a 1µf MLC capacitor. It may be useful to apply a larger filtering capacitor at the voltage source.

3.3.2 S2: System Clock Select

This switch selects which of the two available clock sources on the DAC1220EVM will be provided to the DAC1220.

When the slider is moved all the way up, the external clock source provided on J2, pin 17 (SYSCLK) is selected. Note that if this position is selected and no clock is provided on pin 17, the DAC1220 will not operate.

The other two positions both select the onboard 2.4576MHz crystal. This is the frequency used in DAC1220 datasheet characterizations.

There is no difference between the middle and bottom positions of S2.

Chapter 4

Schematic and Layout

This chapter contains the complete bill of materials, schematic, and PCB layout for the DAC1220EVM.

Note:

Board layouts are not to scale. These are intended to show how the board is laid out; they are not intended to be used for manufacturing DAC1220EVM PCBs.

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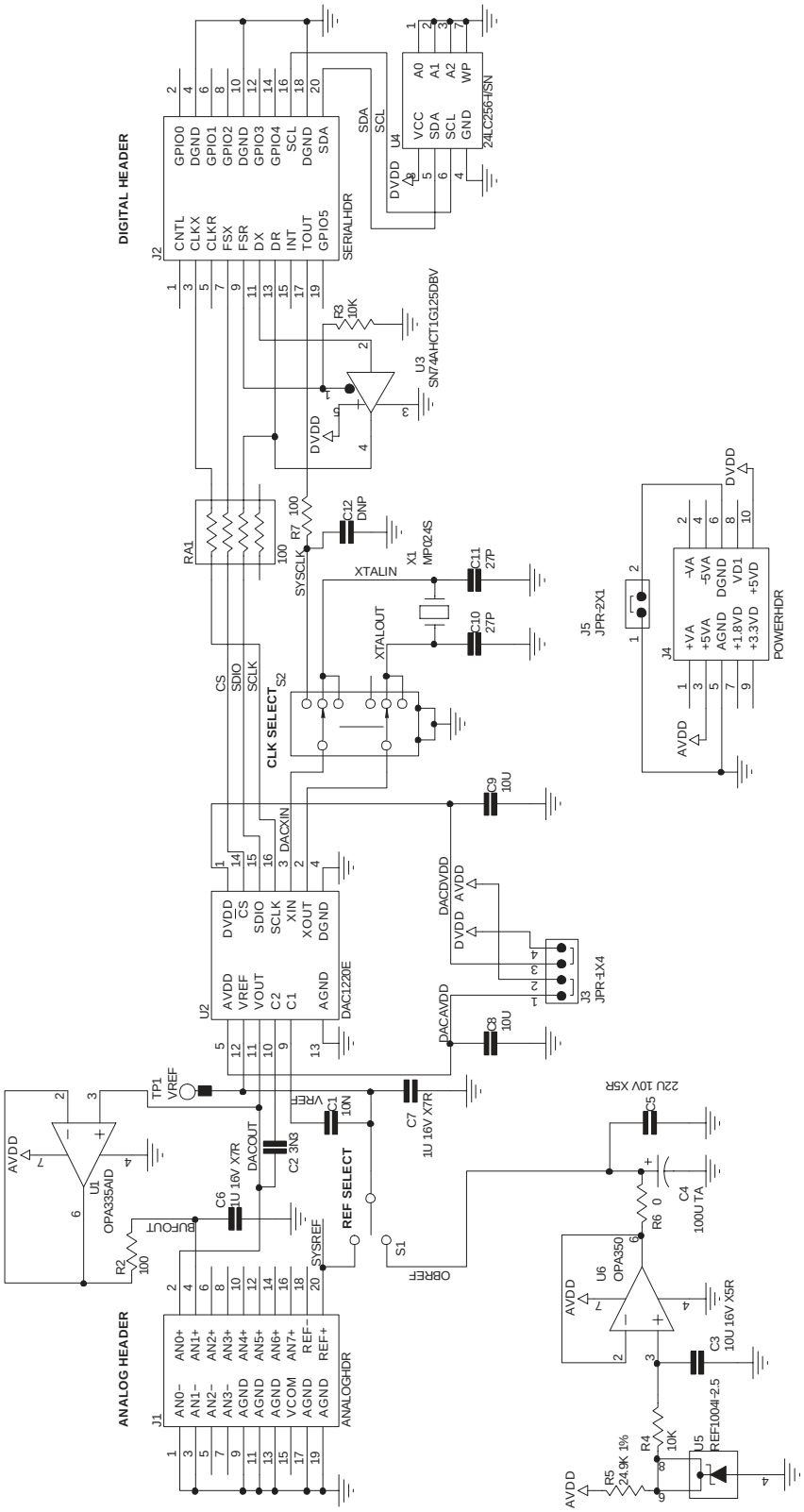
4.1 Schematic

Figure 4−1. DAC1220EVM Schematic



4.2 Board Layout

Figure 4−2. DAC1220EVM—Layer 1 (Top)

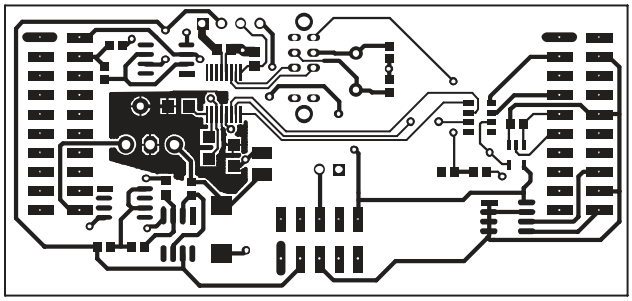
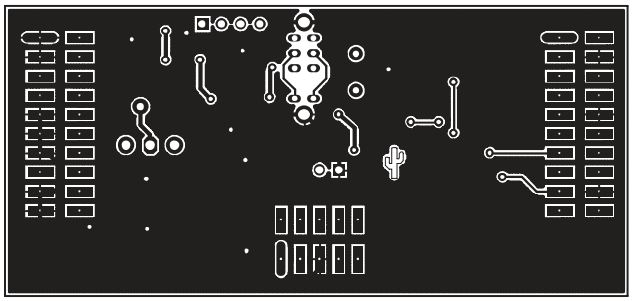


Figure 4−3. DAC1220EVM—Layer 2 (Bottom side, viewed from top)



4.3 Bill of Materials

Table 4−1. Bill of Materials

Reference Designator	Description	Vendor	Part Number
R2, R7	100Ω 1/16W 5% chip resistor	Panasonic	ERJ-3GEYJ101V
R3, R4	10kΩ 1/16W 5% chip resistor	Panasonic	ERJ-3GEYJ103V
R5	24.9kΩ 1/16W 1% chip resistor	Panasonic	ERJ-3EKF24R9V
R6	0Ω 1/10W 5% chip resistor	Panasonic	ERJ-3GEY0R00V
RA1	100Ω resistor array	CTS	744C083101JTR
C1	10nF 50V 2% PPS film capacitor	Panasonic	ECH-U1H103GX5
C2	3.3nF 50V 2% PPS film capacitor	Panasonic	ECH-U1H332GX5
C5	22µF 16V X5R 20% ceramic chip resistor	TDK	C3225X5R1C226M
C6	1µF 16V X5R 10% ceramic chip resistor	TDK	C1608X5R1C105K
C7	1µF 16V X7R 10% ceramic chip resistor	TDK	C3216X7R1C226M
C8, C9, C3	10µF 6.3V X5R 20% ceramic chip resistor	TDK	C2012X5R0J106M
U1	Operational amplifier	Texas Instruments	OPA335AID
U2	Digital-to-analog converter	Texas Instruments	DAC1220E
U3	Tri-state buffer	Texas Instruments	SN74AHCT1G125DBV
U4	256K I^2C EEPROM	Microchip	24LC256-I/SN
U5	2.5V voltage reference	Texas Instruments	REF1104I-2.5
U6	Operational amplifier	Texas Instruments	OPA350UA
X1	2.4576MHz crystal, 25pF load	CTS	MP024S