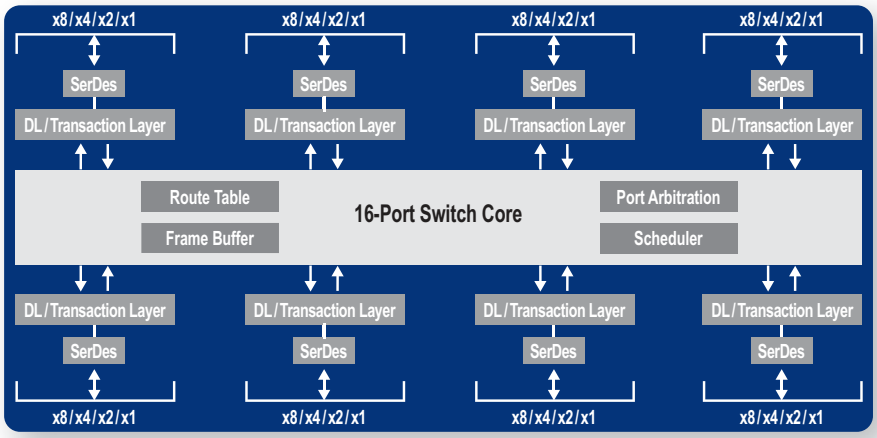
64-Lane 16-Port PCIe® Gen3 System Interconnect Switch

Integrated Device Technology

POWER MANAGEMENT | ANALOG & RF | **INTERFACE & CONNECTIVITY** | CLOCKS & TIMING | MEMORY & LOGIC | TOUCH & USER INTERFACE | VIDEO & DISPLAY | AUDIO

FEATURES

- **High Performance Non-Blocking Switch Architecture**
  - 64-lane 16-port PCIe switch
  - Integrated SerDes supports 8.0 GT/s Gen3, 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
  - Delivers up to 128 GBps (1024 Gbps) of switching capacity
  - Low latency cut-through architecture
  - Multicast compliant to Spec
  - Supports up to 2 KB maximum payload size
  - Request metering for maximum system throughput
- **Standards and Compatibility**
  - PCI Express Base Specification 3.0 compliant
  - Implements the following optional PCI Express features:
    - *Advanced Error Reporting (AER) on all ports*
    - *Access Control Services (ACS)*
    - *Alternative Routing ID (ARI) ECN*
    - *Internal Error Reporting (IER) ECN*
    - *Atomic operations ECN*
    - *TLP processing hints (TPH) ECN*
    - *Latency Tolerance Reporting (LTR) ECN*
    - *Optimized Buffer Flush/Fill (OBFF) ECN*
  - PCI Power Management Spec
    - *Supports D0, D3hot and D3 power management states*
  - Active State Power Management (ASPM)
- **Switch Initialization/Configurability**
  - Supports x8, x4, x2 and x1 ports
  - Automatic per port link width negotiation
  - Automatic lane reversal
  - Autonomous and software managed link width and speed control
  - Per lane SerDes configuration
  - Supports Global and Local reference port clock input
  - Crosslink support
  - 54 General Purpose I/O
  - Supports Root (BIOS, OS, or driver), Serial EEPROM, pin strapping, or SMBus switch initialization
  - No power sequencing requirements
- **Multi-Root Support**
  - Supports up to 16 fully independent switch partitions
  - Configurable downstream port device numbering
  - Supports dynamic reconfiguration of switch partitions
  - Movable upstream port within and between switch partitions
- **Reliability, Availability and Serviceability (RAS)**
  - ECRC support
  - AER on all ports
  - SECDED ECC protection on all internal RAMs
  - End-to-end data path parity protection
  - Ability to generate an interrupt (INTx or MSI) on link up/down transitions
  - Hot-plug supported on all downstream switch ports
  - On-chip link activity and status outputs available including the upstream ports
  - Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG
- **Development Tools**
  - 89KTPES64H16G3 Evaluation Board
  - PCIe Browser Software
  - Provides ODS (On-Die Scope)
  - Built-in PRBS generator and checker
  - Documentation and support at: **www.IDT.com**
- **Packaged in a 35mm x 35mm 1156-ball FCBGA**

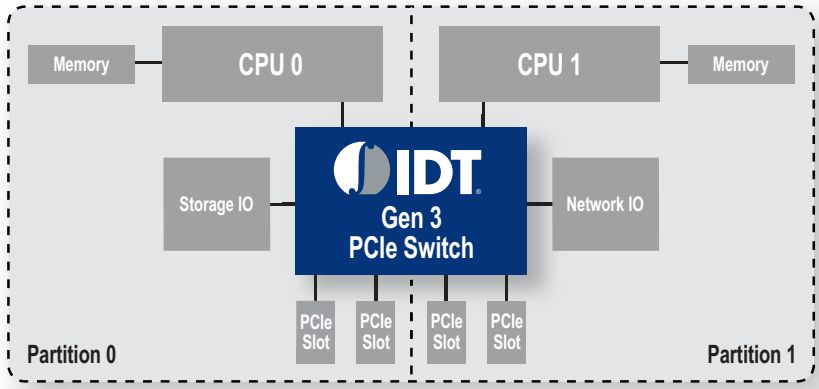


64 PCI Express Lanes - Up to 8 x8 ports or 16 x4 ports

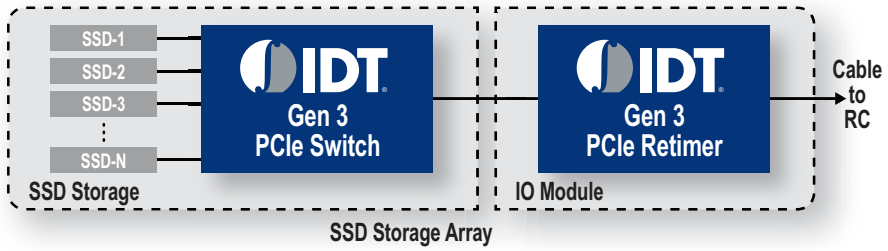
Device Overview

The 89H64H16G3 is a 64-lane, 16-port system interconnect switch optimized for PCI Express® Gen3 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Utilizing standard PCI Express Gen3 interconnect, the 89H64H16G3 provides the most efficient system interconnect switching solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. Each lane is capable of 8 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base specification 3.0.



Enterprise Server



SSD Storage Array

PB_IDT89H64H16G3_REVA0911