

## **Integrated Device Technology**

# 64-Lane 16-Port PCle® Gen3 System Interconnect Switch

POWER MANAGEMENT | ANALOG & RF | INTERFACE & CONNECTIVITY | CLOCKS & TIMING

### **FEATURES**

### High Performance Non-Blocking Switch Architecture

- 64-lane 16-port PCle switch
- Integrated SerDes supports 8.0 GT/s Gen3, 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
- Delivers up to 128 GBps (1024 Gbps) of switching capacity
- Low latency cut-through architecture
- Multicast compliant to Spec
- Supports up to 2 KB maximum payload size
- Request metering for maximum system throughput

### • Standards and Compatibility

- PCI Express Base Specification 3.0 compliant
- Implements the following optional PCI Express features:
  - Advanced Error Reporting (AER) on all ports
  - Access Control Services (ACS)
  - Alternative Routing ID (ARI) ECN
  - Internal Error Reporting (IER) ECN
  - Atomic operations ECN
  - TLP processing hints (TPH) ECN
  - Latency Tolerance Reporting (LTR) ECN
  - Optimized Buffer Flush/Fill (OBFF) ECN
- PCI Power Management Spec
  - Supports D0, D3hot and D3 power management states
- Active State Power Management (ASPM)

### • Switch Initialization/Configurability

- Supports x8, x4, x2 and x1 ports
- Automatic per port link width negotiation
- Automatic lane reversal
- Autonomous and software managed link width and speed control
- Per lane SerDes configuration
- Supports Global and Local reference port clock input
- Crosslink support
- 54 General Purpose I/O
- Supports Root (BIOS, OS, or driver), Serial EEPROM, pin strapping, or SMBus switch initialization
- No power sequencing requirements

### • Multi-Root Support

- Supports up to 16 fully independent switch partitions
- Configurable downstream port device numbering
- Supports dynamic reconfiguration of switch partitions
- Movable upstream port within and between switch partitions

### • Reliability, Availability and Serviceability (RAS)

- ECRC support
- AER on all ports
- SECDED ECC protection on all internal RAMs
- End-to-end data path parity protection
- Ability to generate an interrupt (INTx or MSI) on link up/down transitions
- Hot-plug supported on all downstream switch ports
- On-chip link activity and status outputs available including the upstream ports
- Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG

### • Development Tools

- 89KTPES64H16G3 Evaluation Board
- PCle Browser Software
- Provides ODS (On-Die Scope)
- Built-in PRBS generator and checker
- Documentation and support at: www.IDT.com
- Packaged in a 35mm x 35mm 1156-ball FCBGA

# x8/x4/x2/x1 x8/x4/x2/x1

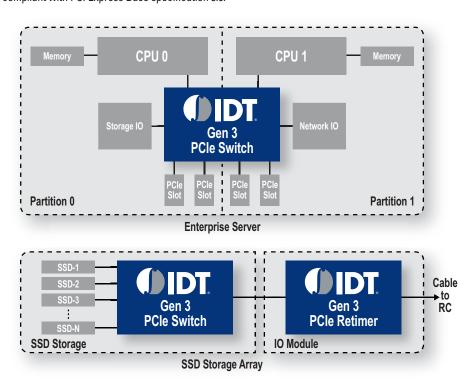
| TOUCH & USER INTERFACE | VIDEO & DISPLAY | AUDIO

64 PCI Express Lanes - Up to 8 x8 ports or 16 x4 ports

### **Device Overview**

The 89H64H16G3 is a 64-lane, 16-port system interconnect switch optimized for PCI Express® Gen3 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Utilizing standard PCI Express Gen3 interconnect, the 89H64H16G3 provides the most efficient system interconnect switching solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. Each lane is capable of 8 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base specification 3.0.



DISCLAIMER Integrated Device Technology, Inc. (IDT) and its subsidiaries reserve the right to modify the products and/or specifications described herein at any time and at IDT's sole discretion. All information in this document, including descriptions or product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when stated in customer products. The information contained herein is provided without preparationary of any kind, whether express or implied, clinically, but not limited by, the subtibility of IDT's products for any particular purpose, an implied variantly of machine and the products. The information contained herein is predicted properly right to forther. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties. IDT's products are not intended for use in life support systems or similar devices where the failture or antiferrotion of an IDT product is not an amend edoes so the propertor of similar devices where the failture or antiferrotion of an IDT product is not an amend edoes so the source of the product of similar devices where the failture or antiferrotion of an IDT product is not an amend edoes so the source of the product of similar devices where the failture or antiferrotion of an IDT product is not a manner does so that the properties of the product is an amend edoes and the product of the product of the health or safety of users. Approve using an IDT product is not a manner does so the product of similar devices where the health or safety the health or safety of users. Approve using an IDT product is not a manner does so that the product of similar devices where the failture or antiferrotion is not an amend one so that the product of similar the product of the product of the product of the product of the health or safety the health or

Integrated Device Technology, IDT and the IDT logo are registered trademarks of IDT. Other trademarks and service marks used herein, including protected names, logos and designs, are the property of IDT or their respective third party owners. © Copyright 2011. All rights reserved.

PB\_IDT89H64H16G3\_REVA0911