User's Guide

TPS563900 Buck Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS563900EVM-574 evaluation module (PWR574) as well as for the TPS563900 dc/dc converter. Also included are the performance specifications, the schematic, and the bill of materials for the TPS563900EVM-574.

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1 Introduction

1.1 Background

The TPS563900 is a dual output current mode control dc/dc converter with output rated for up to 3.5 A. The input voltage range is 4.5 V to 18 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1. The TPS563900 features I^{2}C VID control. The output voltage for each channel can be set within the range of 0.68 V to 1.95 V. This evaluation module is designed to demonstrate the small printed-circuit-board (PCB) areas that may be achieved when designing with the TPS563900 regulator. The switching frequency is externally set at a nominal 500 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS563900 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS563900 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS563900 provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 20 V for the TPS563900EVM-574.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS563900EVM-574	VIN = 4.5 V to 18 V	V_{OUT1} = V_{OUT2} = 0 A to 3.5 A

1.2 Performance Specification Summary

A summary of the TPS563900EVM-574 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.0 V for V_{OUT1} and 1.1 V for V_{OUT2}, unless otherwise specified. The TPS563900EVM-574 is designed and tested for V_{IN} = 4.5 V to 18 V with the VIN and PVIN pins connect together. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS563900EVM-574 Performance Specification Summary

Specification	Test Conditions		MIN	TYP	MAX	Unit
V_{IN} voltage range (PVIN = VIN)			4.5	12	18	V
V_{IN} start voltage (internal UVLO)				2.12		V
V_{IN} stop voltage (internal UVLO)				1.74		V
Output voltage set point, V_{OUT1}				1.0		V
Output current range, V_{OUT1}	V_{IN} = 4.5 V to 18 V		0		3.5	A
Output voltage set point, V_{OUT2}				1.1		
Output current range, V_{OUT2}	V_{IN} = 4.5 V to 18 V		0		3.5	
Line regulation, V_{OUT1} and V_{OUT2}	I_O = 1.75 A, V_{IN} = 4.5 V to 18 V			±0.02		%
Load regulation, V_{OUT1} and V_{OUT2}	V_{IN} = 5 V, I_O = 0 A to 3.5 A			±0.35		%
Load transient response, V_{OUT1} and V_{OUT2}	I_O = 0.5 A to 2.5 A	Voltage change		–40		mV
		Recovery time		100		µs
	I_O = 2.5 A to 0.5 A	Voltage change		40		mV
		Recovery time		100		µs
Output ripple voltage, V_{OUT1} and V_{OUT2}	I_O = 3.5 A			10		mVPP
Output rise time, V_{OUT1} and V_{OUT2}				1		ms
Operating frequency				500		kHz

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS563900. Some modifications can be made to this module.

1.3.1 Output Voltage Setpoint

The output voltage of the EVM is set either externally using a voltage divider or internally using the integrated I^{2}C interface. The external adjustment of the output voltage for V_{OUT1} is set by the resistor divider network of R10 and R11. The external adjustment of the output voltage for V_{OUT2} is set by the resistor divider network of R16 and R17. R10 and R16 are fixed at 40.2 kΩ. To change the output voltage of V_{OUT1} or V_{OUT2}, it is necessary to change the value of resistor R11 or R17. Changing the value of R11 or R17 can change the output voltage

in the range of 0.68 V to 1.95 V. The value of R11 or R17 for a specific output voltage can be calculated using Equation 1 or Equation 2.

$$R11 = \frac{R10 \times 0.6V}{V_{OUT} - 0.6V} \quad (1)$$

or

$$R17 = \frac{R16 \times 0.6V}{V_{OUT} - 0.6V} \quad (2)$$

The output voltage can also be set using the optional VID control using the I^2C interface. The EVM is designed so that the J2 connector is compatible with the HPA172 USB Interface Adapter. Using that control and TPS563900 GUI_ver_0_0_0_2 software allows the output voltage to be programmed to any of 128 preset voltages from 0.68 V to 1.95 V. JP2-2 and JP2-3 should be covered to select the default address. JP3 should be open to allow the I^2C pull up to be supplied from the USB adapter, available from www.ti.com/tool/usb-to-gpio. The USB adapter is also available from the TI eStore. See the TPS563900 datasheet (SLVSCC7) for a complete description of the available codes. With the software running and the cable attached, run the GUI interface software (SLVC558). Figure 1-1 shows the GUI interface.

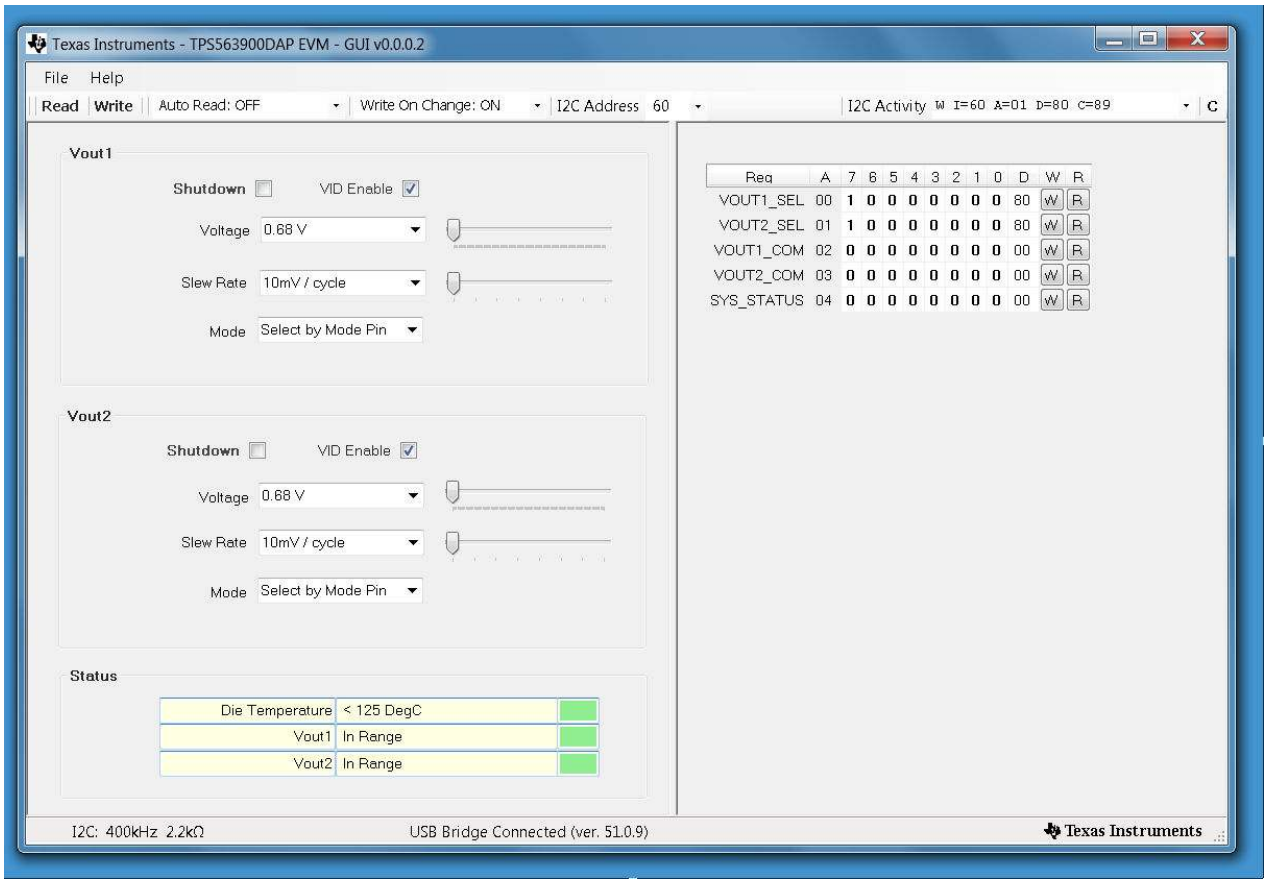

Figure 1-1. TPS563900 GUI_ver_0_0_0_2 Screen

To change the output voltages, ensure that the VID Enable check boxes are checked. The voltages can be interactively changed using the slide controls when "Write On Change: ON" is active. See the TPS563900 datasheet for further details.

1.3.2 Slow-Start Time

The slow-start time can be adjusted by changing the value of C7 or C8 for V_{OUT1} or V_{OUT2}. Use Equation 3 or Equation 4 to calculate the required value of C7 or C8 for desired slow-start times.

$$C7(nF) = \frac{Tss(ms) \times 6\ \mu A}{0.6\ V} \quad (3)$$

or

$$C8(nF) = \frac{Tss(ms) \times 6\ \mu A}{0.6\ V} \quad (4)$$

The EVM is set for a slow-start time of 1 ms using C7 = C8 = 10 nF.

1.3.3 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R3 and R4 or R5 and R6 for V_{OUT1} or V_{OUT2}. Use Equation 5 and Equation 6 to calculate required resistor values for different start voltages.

$$R3 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (5)$$

or

$$R5 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (6)$$

Use Equation 7 or Equation 8 to calculate required resistor values for different stop voltages.

$$R4 = \frac{R3 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R3(I_p + I_h)} \quad (7)$$

or

$$R6 = \frac{R5 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R5(I_p + I_h)} \quad (8)$$

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS563900EVM-574 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS563900EVM-574 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 5 A must be connected to J1 through a pair of 20-AWG wires. The loads must be connected to J3 and J4 through a pair of 20-AWG wires. The maximum load current capability is 3.5 A for each output. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP11 is used to monitor V_{OUT1} with TP12 as the ground reference. TP15 is used to monitor V_{OUT2} with TP15 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	VIN input voltage connector. (See Table 1-1 for V_{IN} range.)
J2	I^2C interface connector.
J3	V_{OUT1}, 1.0 V at 3.5 A maximum
J4	V_{OUT2}, 1.1 V at 3.5 A maximum
JP1	MODE select. Cover JP1-2 and JP1-3 to select forced CCM mode. Leave open to select PSM pulse skipping mode for increased light-load efficiency
JP2	ADDR select. Normally cover JP2-2 and JP2-3.
JP3	Jumper to select internal LDO as I^2C pull up voltage. Normally open to allow pull up voltage from the USB interface adapter.
JP4	2-pin header for V_{OUT1} enable. Connect EN to ground to disable, open to enable.
JP5	2-pin header for V_{OUT2} enable. Connect EN to ground to disable, open to enable.
TP1	VIN test point at VIN connector.
TP2	GND test point at VIN connector.
TP3	LDO output test point.
TP4	External I^2C pull up voltage test point.
TP5	V_{OUT1} enable test point.
TP6	V_{OUT2} enable test point.
TP7	V_{OUT1} slow start test point.
TP8	V_{OUT2} slow start test point.
TP9	V_{OUT1} LX1 switching node test point.

Table 2-1. EVM Connectors and Test Points (continued)

Reference Designator	Function
TP10	Test point in V_{OUT1} voltage divider network. Used for loop response measurements when output voltage is set using external resistor divider network.
TP11	Output voltage test point at V_{OUT1} connector.
TP12	GND test point at V_{OUT1} connector.
TP13	V_{OUT2} LX2 switching node test point.
TP14	Test point in V_{OUT2} voltage divider network. Used for loop response measurements when output voltage is set using external resistor divider network.
TP15	Output voltage test point at V_{OUT2} connector.
TP16	GND test point at V_{OUT2} connector.
TP17	Analog GND test point.
TP18	I^2C SDA test point.
TP19	I^2C SCL test point.

2.2 Efficiency

Figure 2-1 and Figure 2-2 show the efficiency for the TPS563900EVM-574 in CCM at an ambient temperature of 25°C.

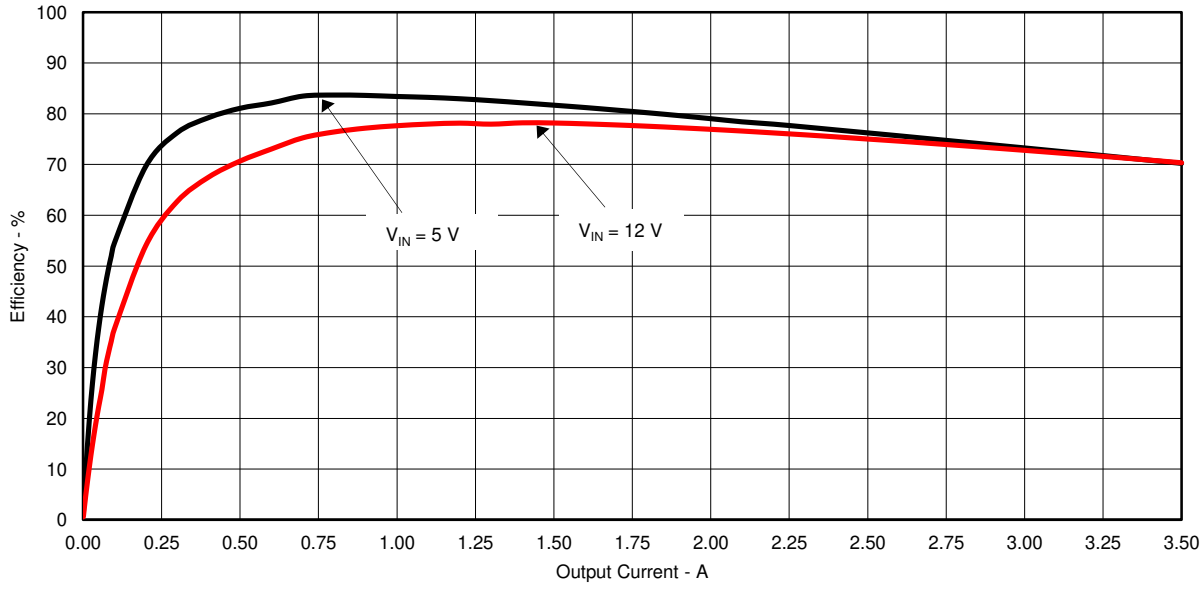

Figure 2-1. TPS563900EVM-574 V_{OUT1} CCM Efficiency

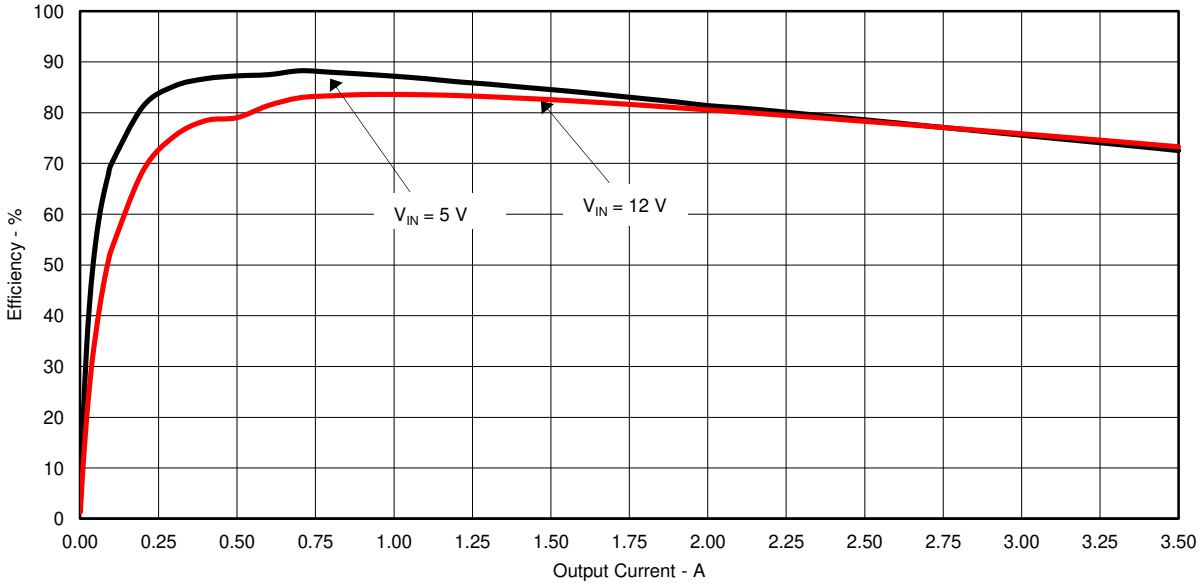

Figure 2-2. TPS563900EVM-574 V_{OUT2} CCM Efficiency

Figure 2-3 and Figure 2-4 show the efficiency for the TPS563900EVM-574 in CCM using a semi-log scale to more easily show efficiency at lower output currents. The ambient temperature is 25°C.

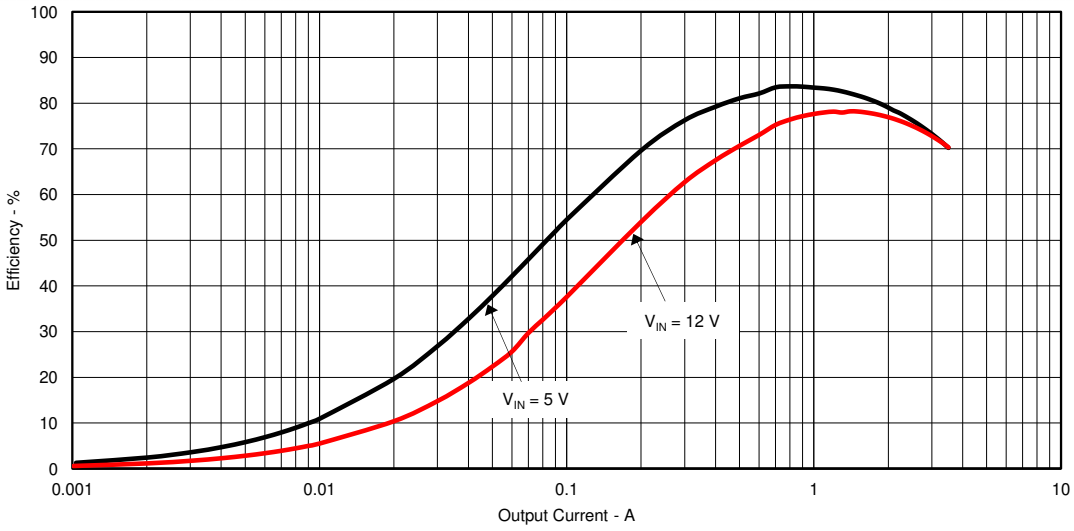

Figure 2-3. TPS563900EVM-574 V_{OUT1} CCM Low Current Efficiency

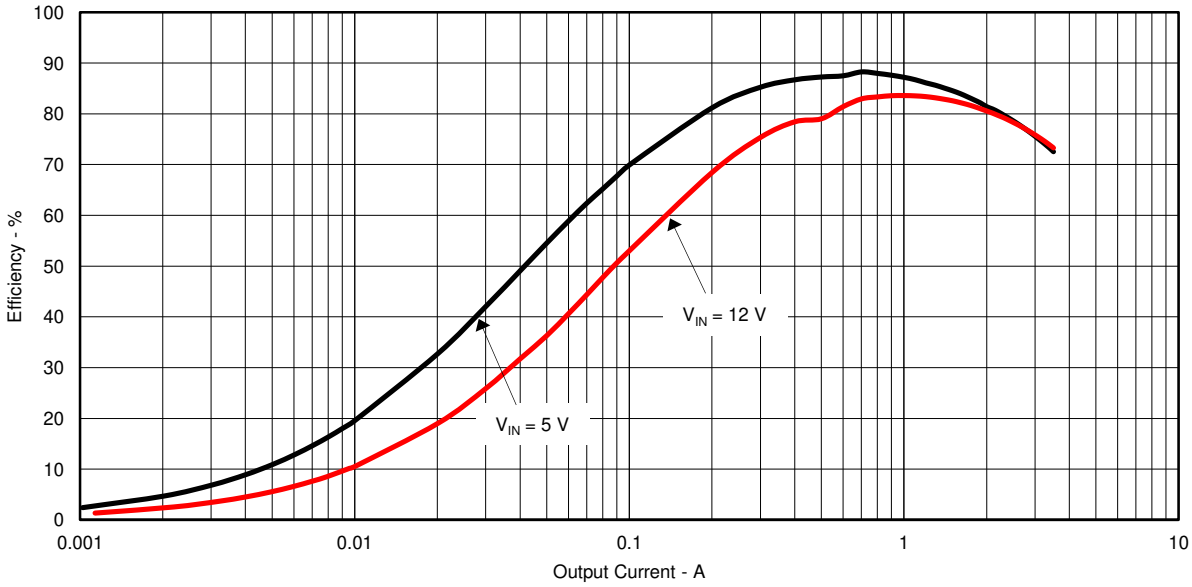

Figure 2-4. TPS563900EVM-574 V_{OUT2} CCM Low Current Efficiency

Figure 2-5 and Figure 2-6 show the efficiency for the TPS563900EVM-574 in SKIP mode at an ambient temperature of 25°C.

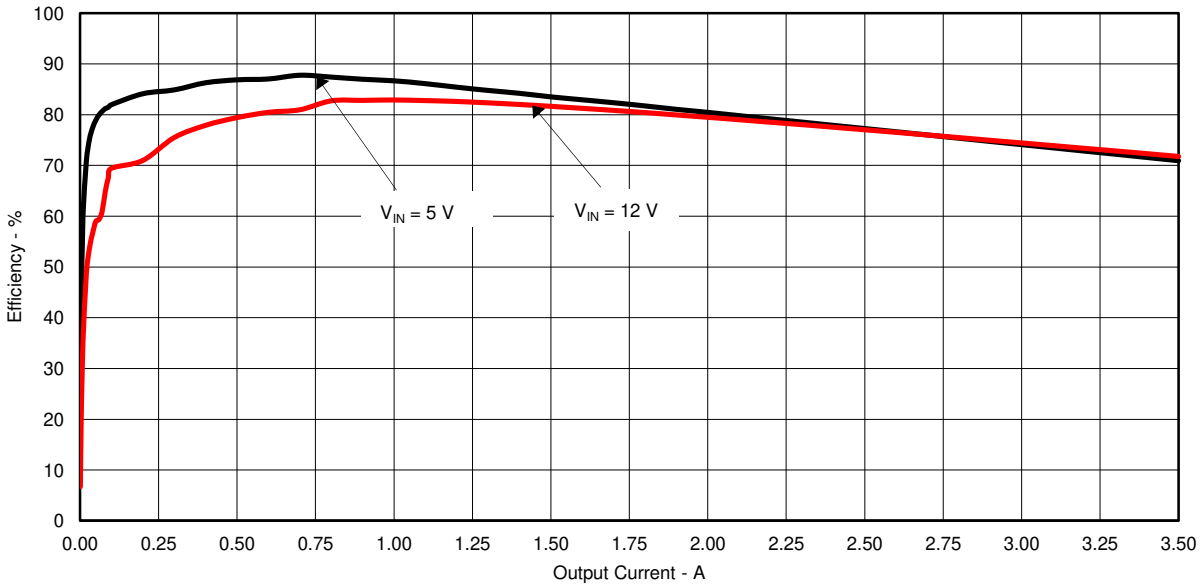

Figure 2-5. TPS563900EVM-574 V_{OUT1} SKIP Mode Efficiency

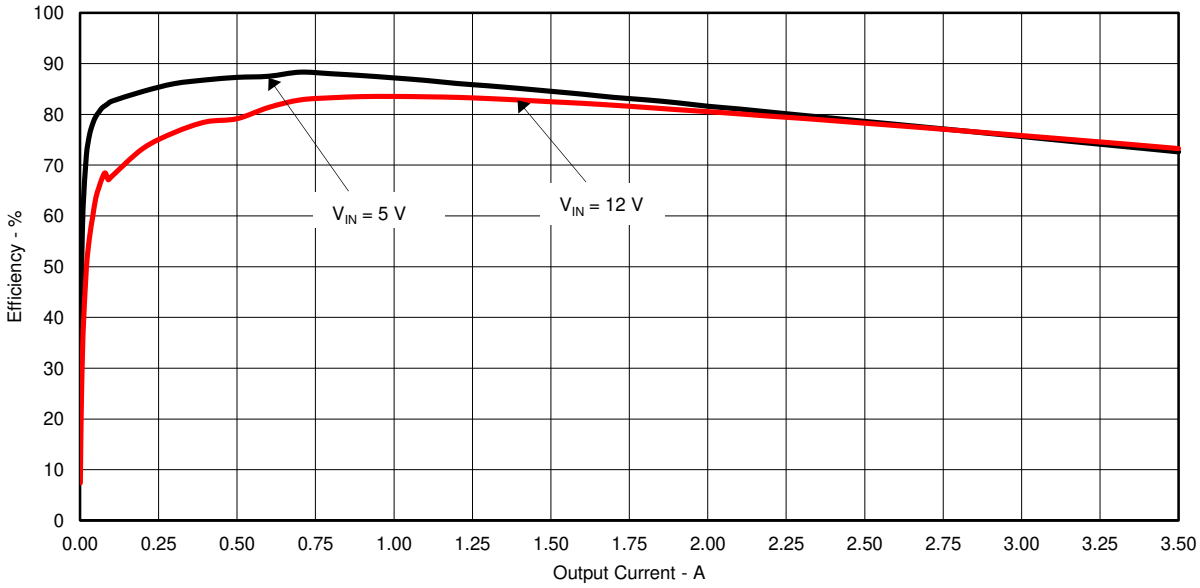

Figure 2-6. TPS563900EVM-574 V_{OUT2} SKIP Mode Efficiency

Figure 2-7 and Figure 2-8 show the efficiency for the TPS563900EVM-574 in SKIP mode using a semi-log scale to more easily show efficiency at lower output currents. The ambient temperature is 25°C.

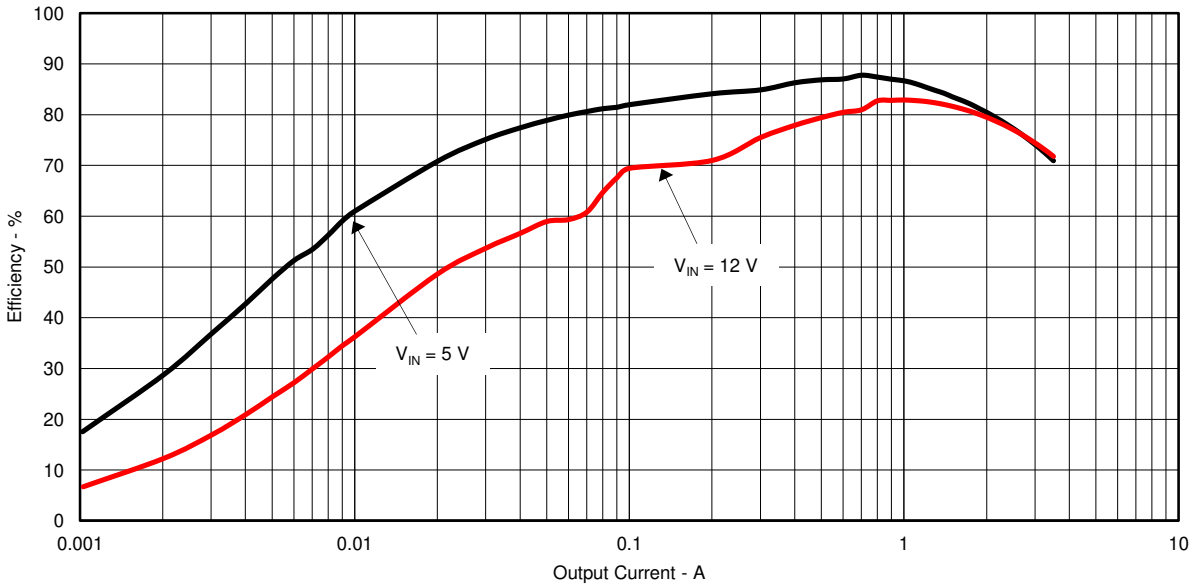

Figure 2-7. TPS563900EVM-574 V_{OUT1} SKIP Mode Low Current Efficiency

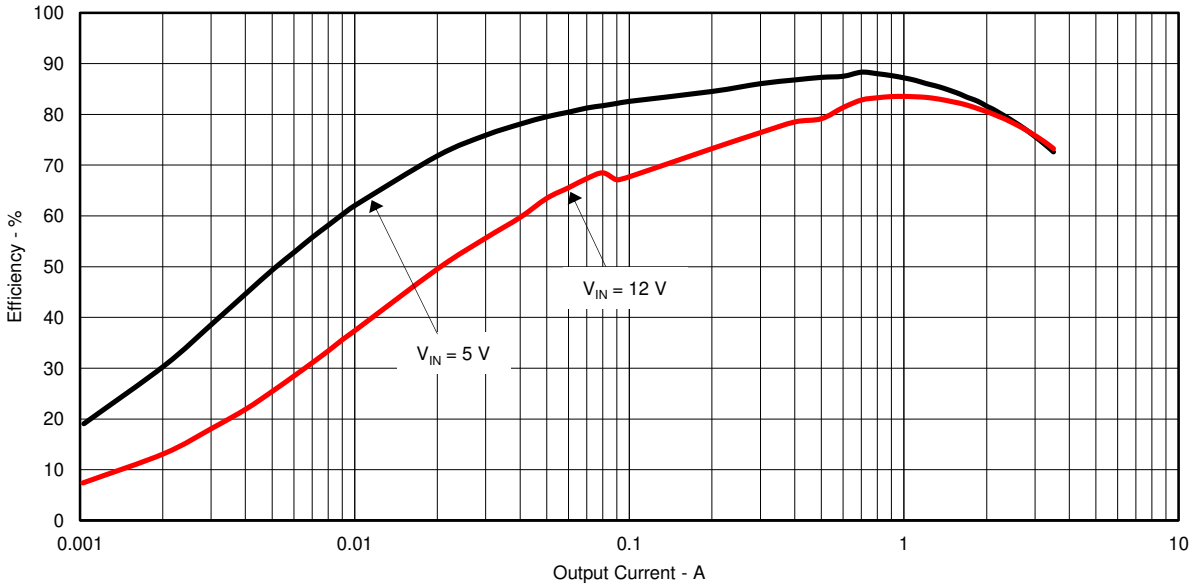

Figure 2-8. TPS563900EVM-574 V_{OUT2} SKIP Mode Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 2-9 and Figure 2-10 show the load regulation for the TPS563900EVM-574 in CCM.

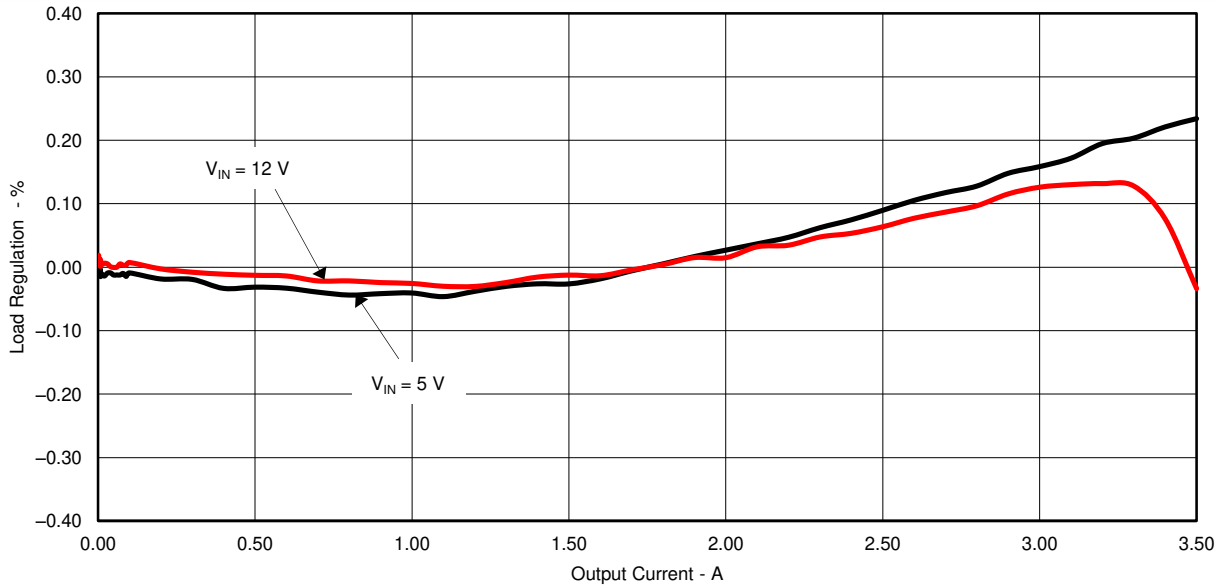

Figure 2-9. TPS563900EVM-574 V_{OUT1} CCM Load Regulation

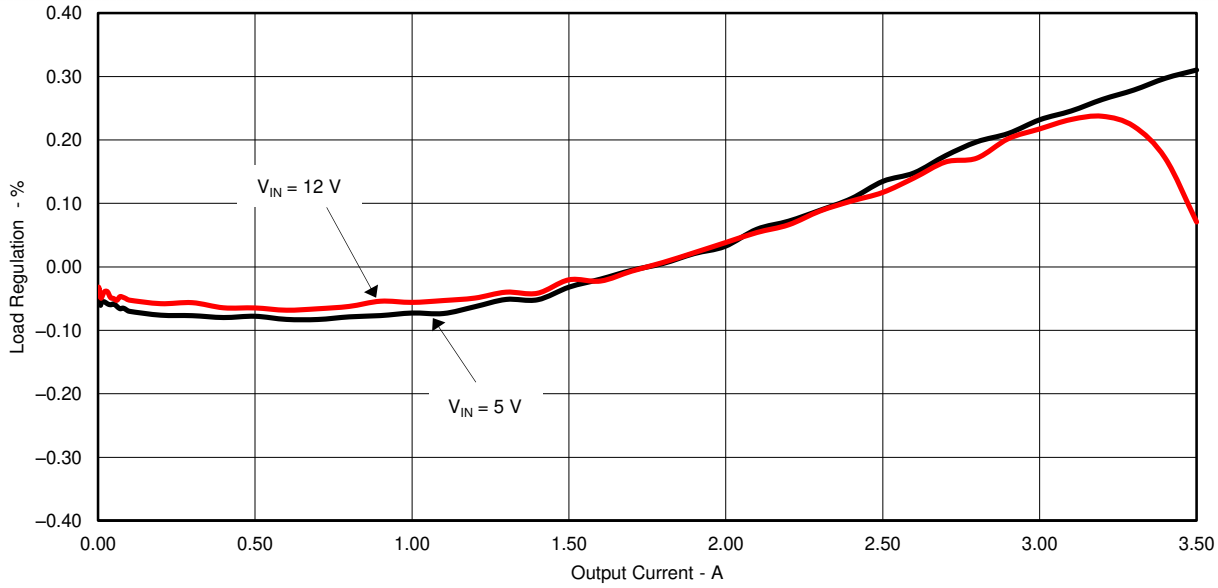

Figure 2-10. TPS563900EVM-574 V_{OUT2} CCM Load Regulation

Figure 2-11 and Figure 2-12 show the load regulation for the TPS563900EVM-574 in SKIP mode.

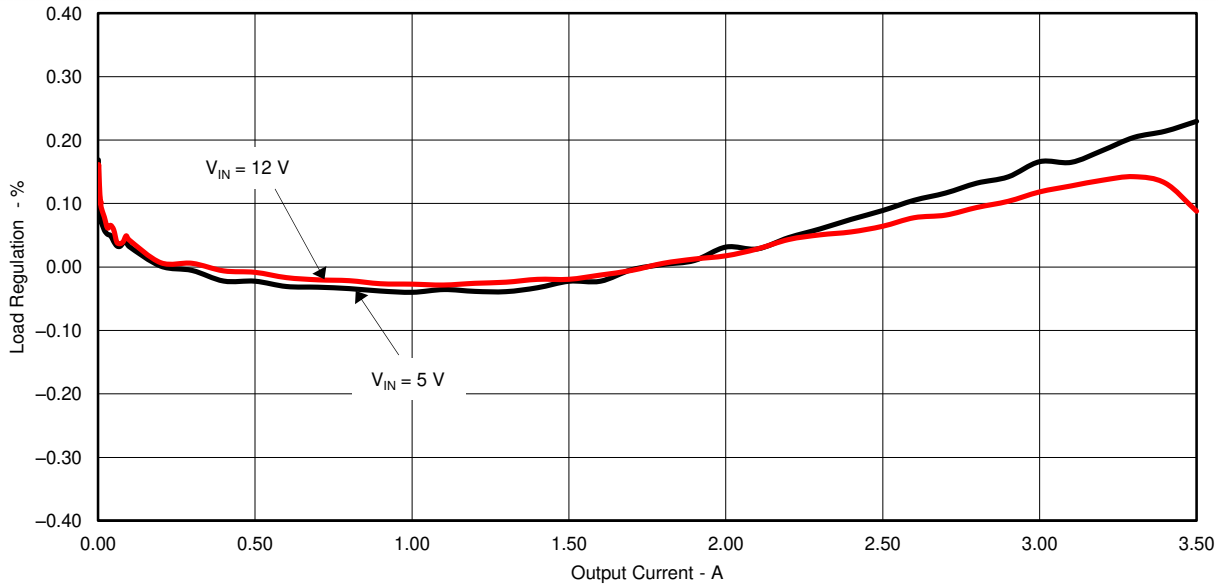

Figure 2-11. TPS563900EVM-574 V_{OUT1} SKIP Mode Load Regulation

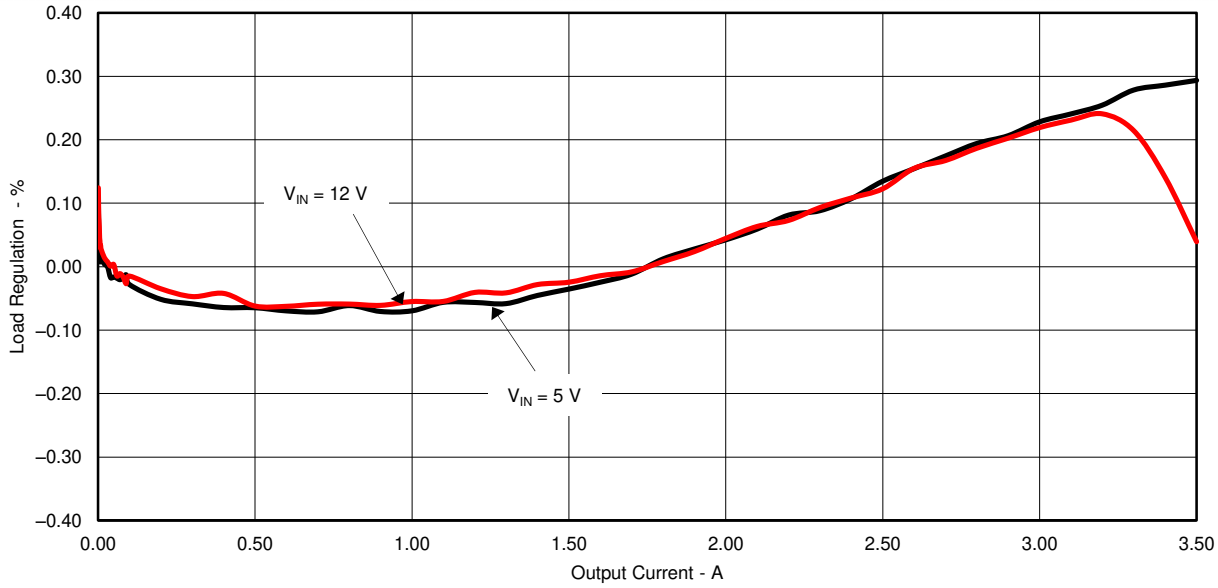

Figure 2-12. TPS563900EVM-574 V_{OUT2} SKIP Mode Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-13 and Figure 2-14 show the line regulation for the TPS563900EVM-574 in CCM.

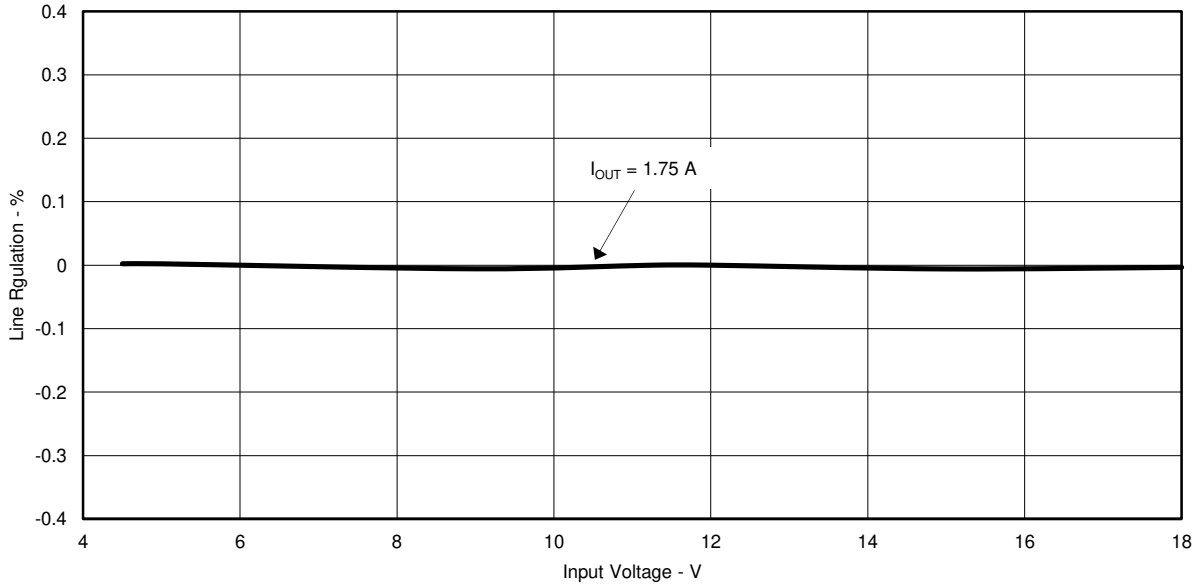

Figure 2-13. TPS563900EVM-574 V_{OUT1} CCM Line Regulation

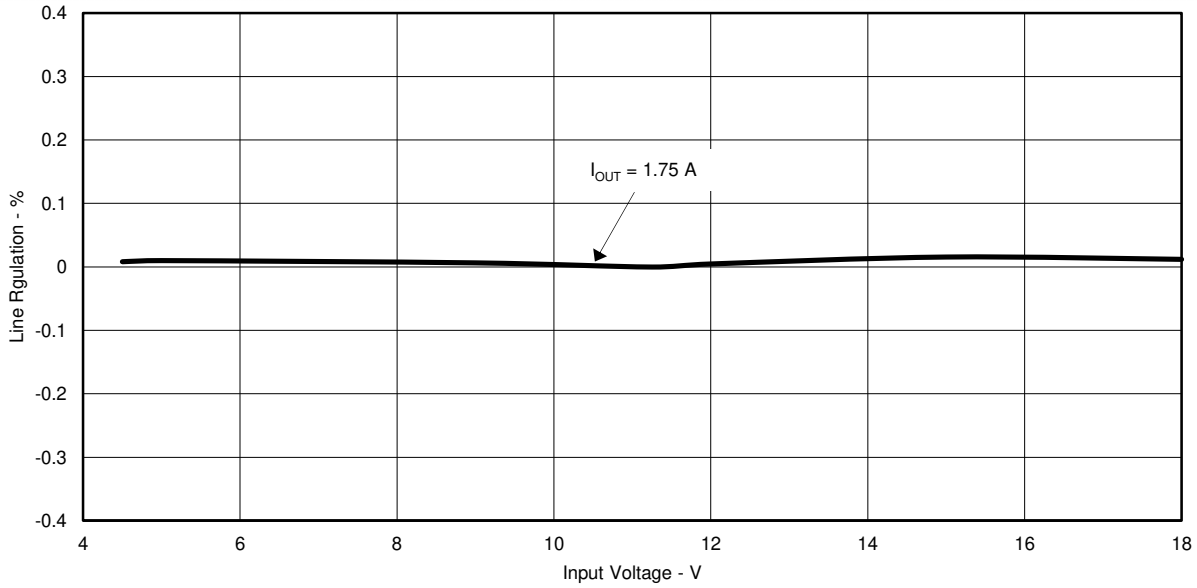

Figure 2-14. TPS563900EVM-574 V_{OUT2} CCM Line Regulation

Figure 2-15 and Figure 2-16 show the line regulation for the TPS563900EVM-574 in SKIP mode.

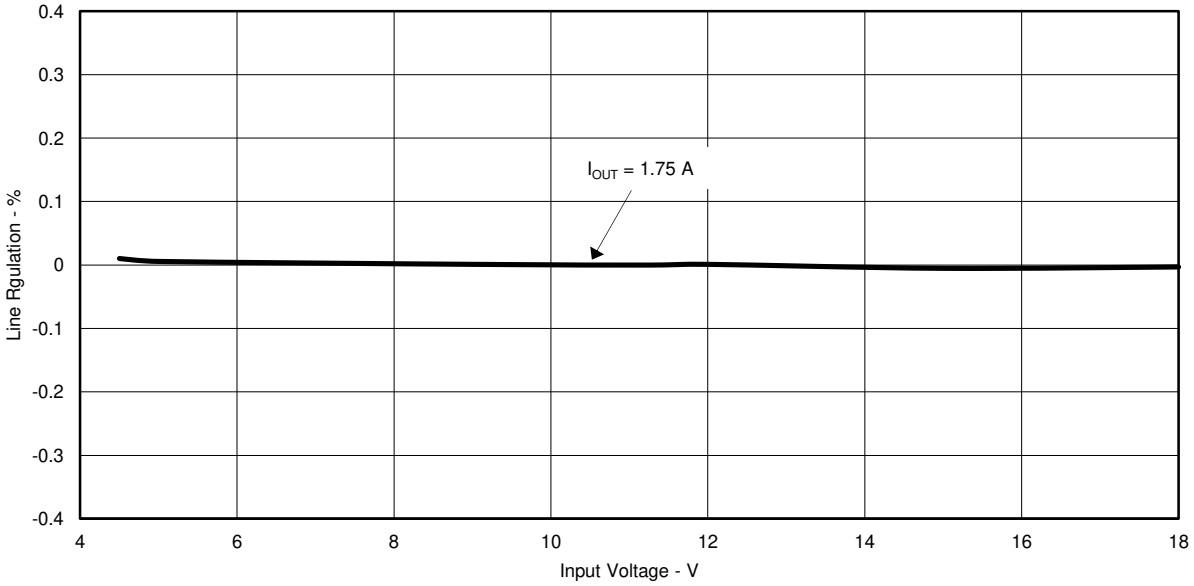

Figure 2-15. TPS563900EVM-574 V_{OUT1} SKIP Mode Line Regulation

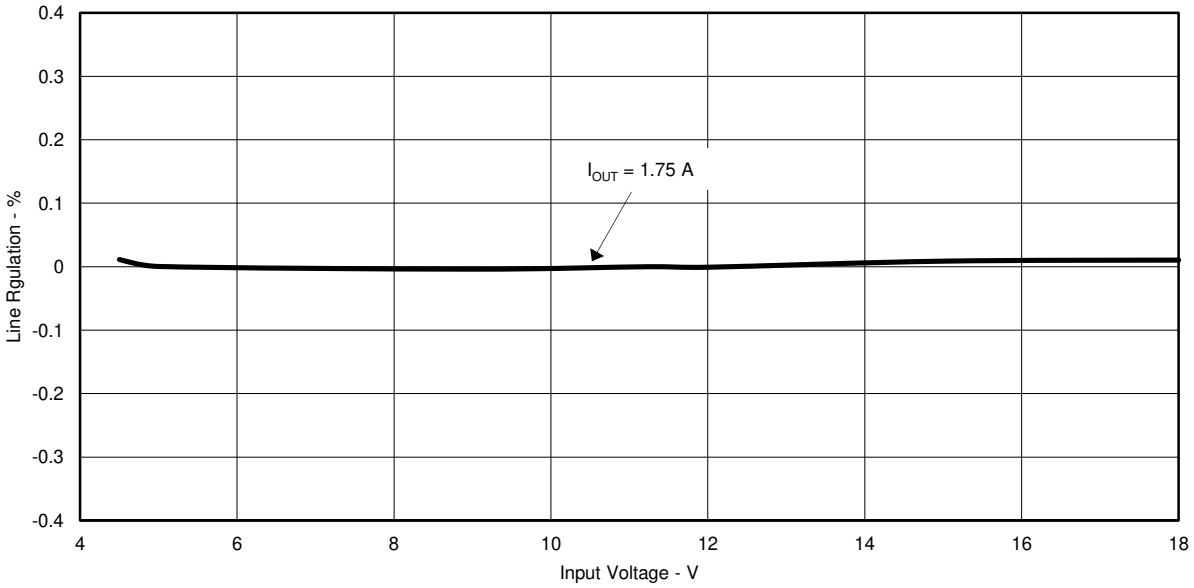

Figure 2-16. TPS563900EVM-574 V_{OUT2} SKIP Mode Line Regulation

2.5 Load Transients

Figure 2-17 and Figure 2-18 show the TPS563900EVM-574 response to load transients. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

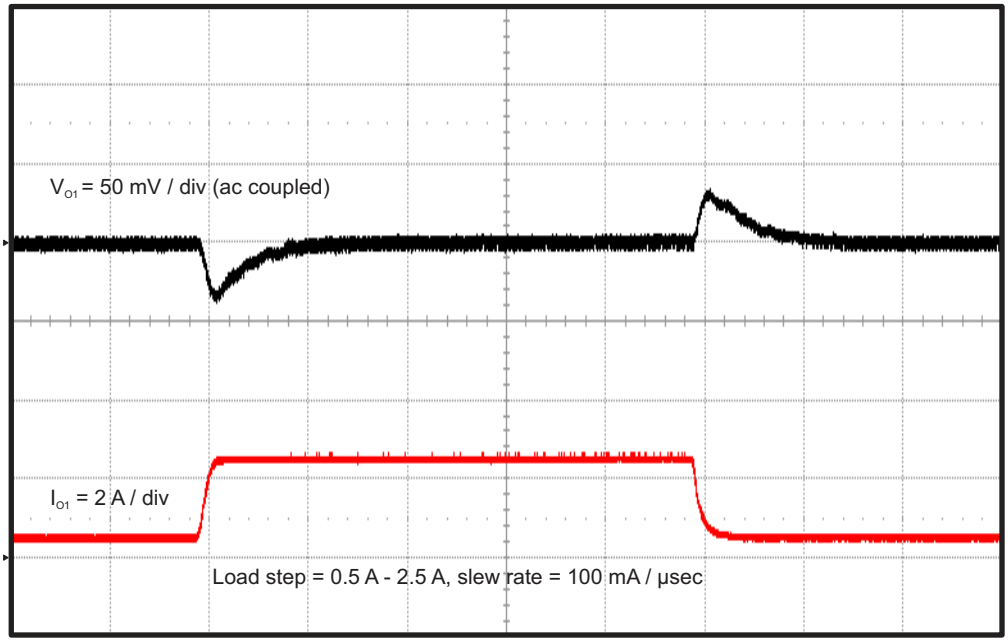

Figure 2-17. TPS563900EVM-574 V_{OUT1} Transient Response

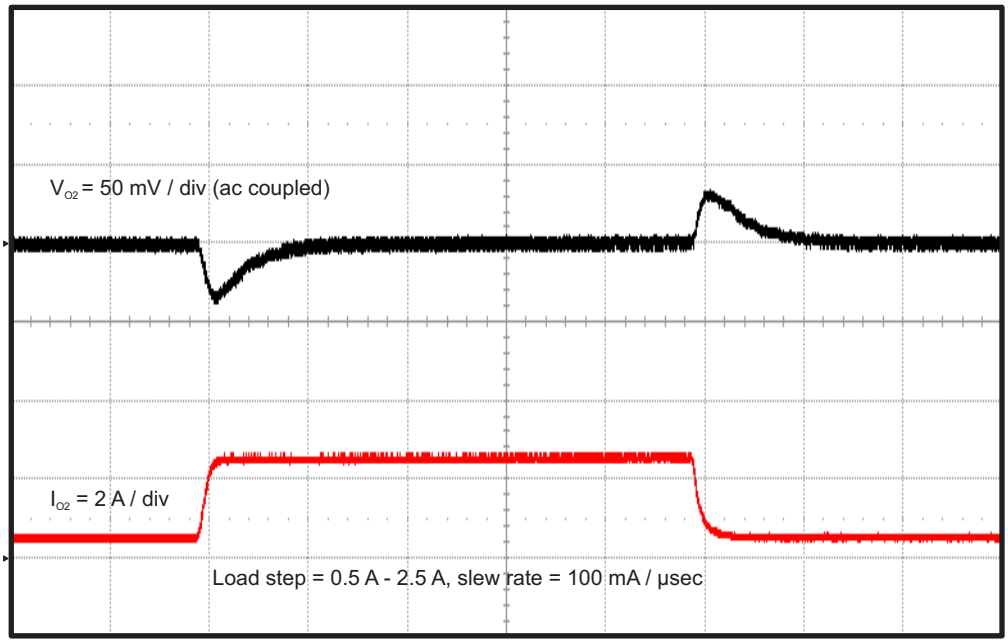

Figure 2-18. TPS563900EVM-574 V_{OUT2} Transient Response

2.6 Loop Characteristics

Figure 2-19 and Figure 2-20 show the TPS563900EVM-574 loop-response characteristics when the output voltage is set by the external resistor divider network. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 1.75 A.

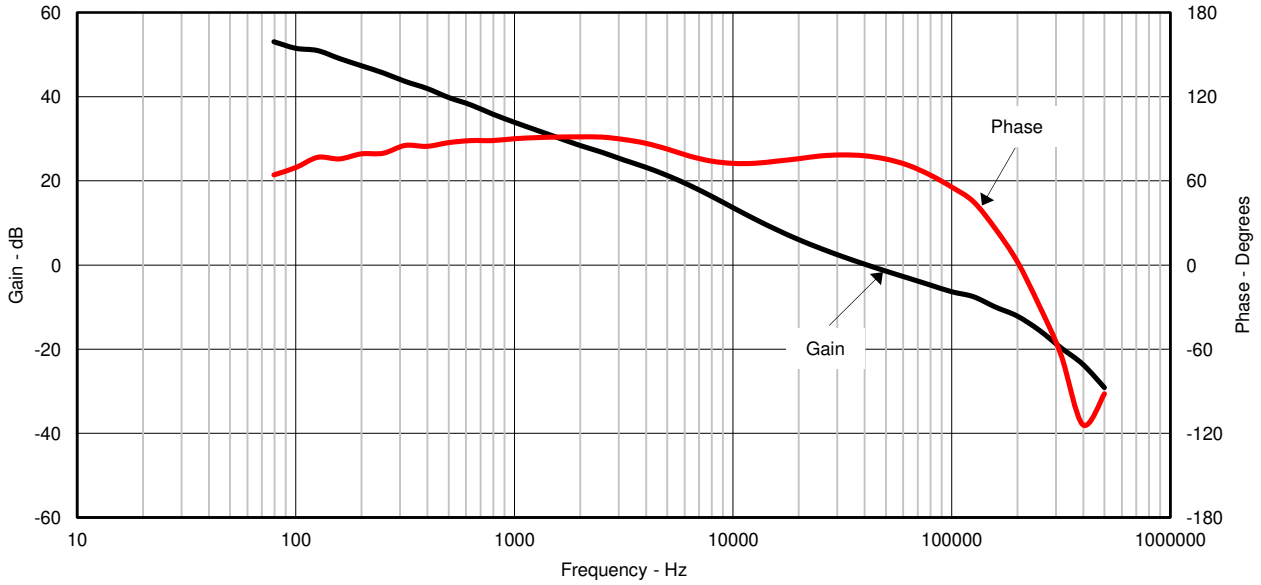

Figure 2-19. TPS563900EVM-574 Loop Response, V_{OUT1} Set by Resistor Divider

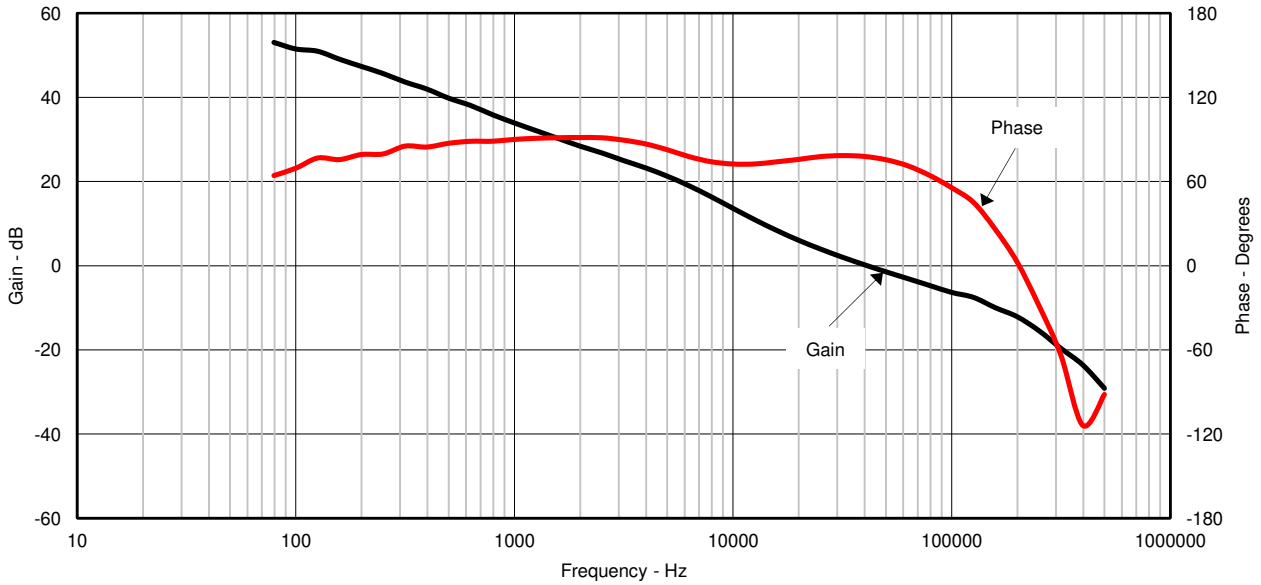

Figure 2-20. TPS563900EVM-574 Loop Response, V_{OUT2} Set by Resistor Divider

2.7 Output Voltage Ripple

Figure 2-21, Figure 2-22, and Figure 2-23 show the TPS563900EVM-574 output voltage ripple. The output currents are as shown in the figures. V_{IN} = 12 V. The ripple voltage is measured directly across the output capacitors.

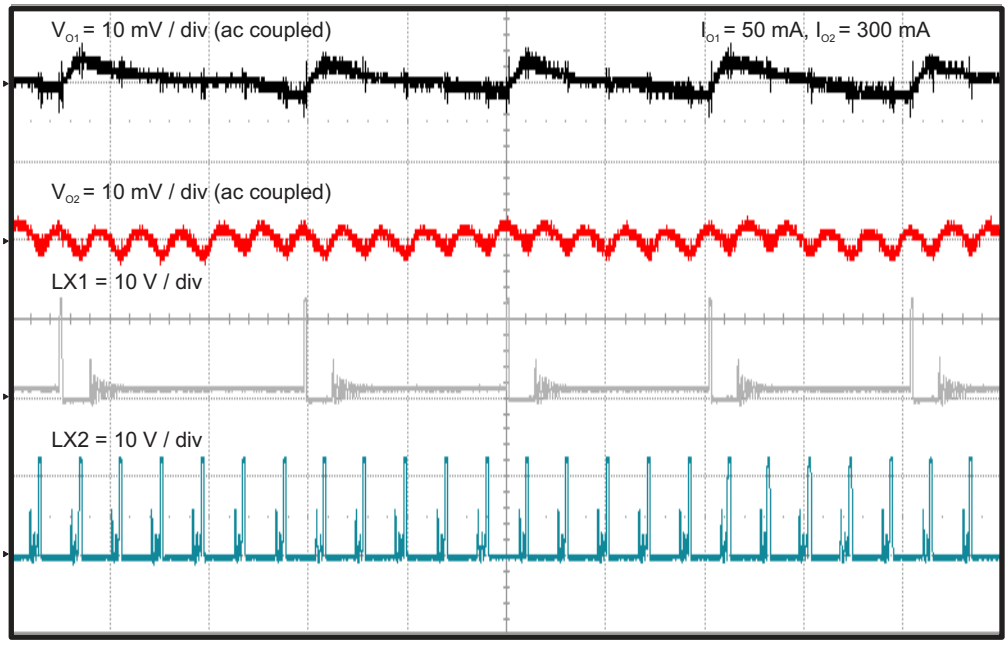

Figure 2-21. TPS563900EVM-574 Output Ripple for Light Loads in SKIP Mode

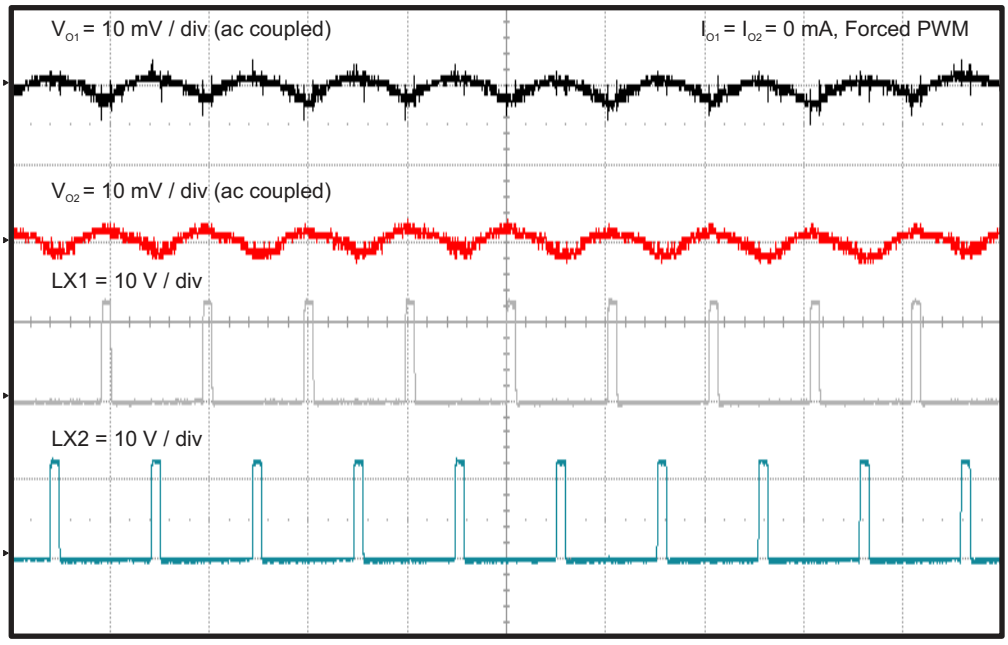

Figure 2-22. TPS563900EVM-574 Output Ripple for No Load in CCM

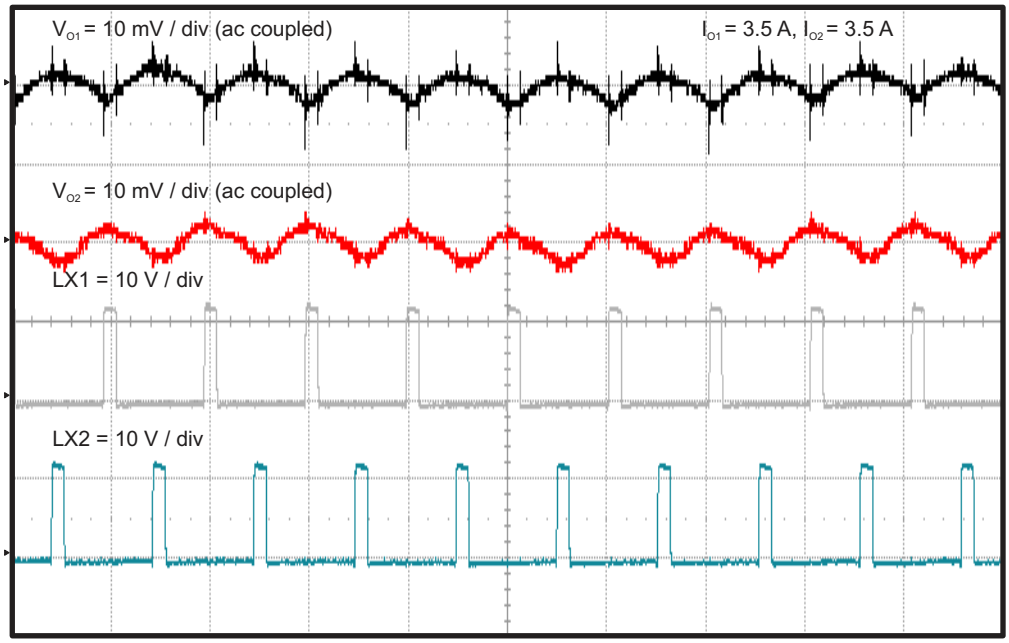

Figure 2-23. TPS563900EVM-574 Output Ripple for Full Load CCM

2.8 Powering Up

Figure 2-24 shows the start-up waveforms for the TPS563900EVM-574 relative to EN1. EN2 is not shown, but the timing is the same relative to V_{IN} and EN1. The input voltage for these plots is 12 V and the load is 1 Ω.

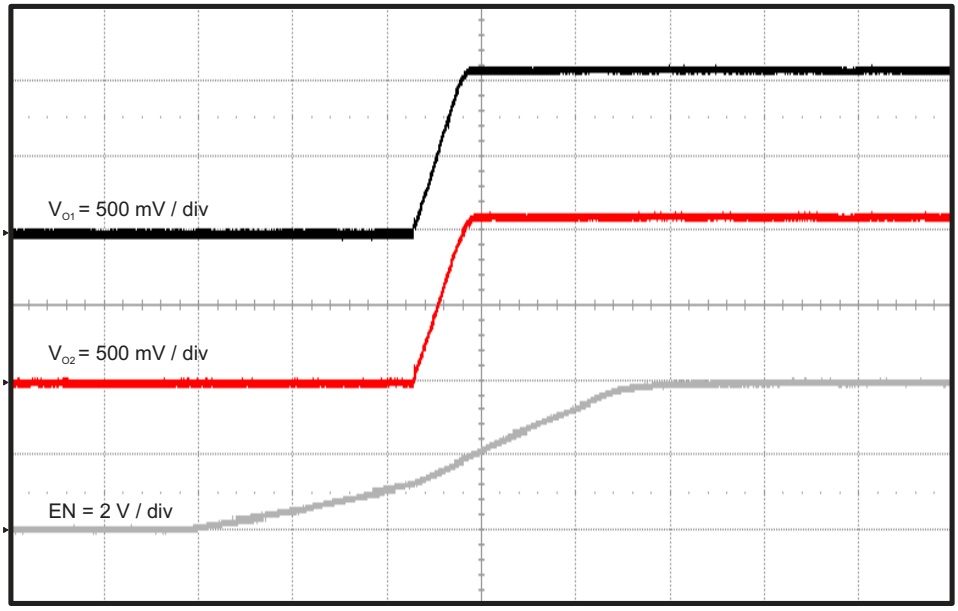

Figure 2-24. TPS563900EVM-574 Start Up

2.9 Shutting Down

Figure 2-25 shows the shut down waveforms for the TPS563900EVM-574 relative to EN1. EN2 is not shown, but the timing is the same relative to V_{IN} and EN1. The input voltage for these plots is 12 V and the load is 1 Ω.

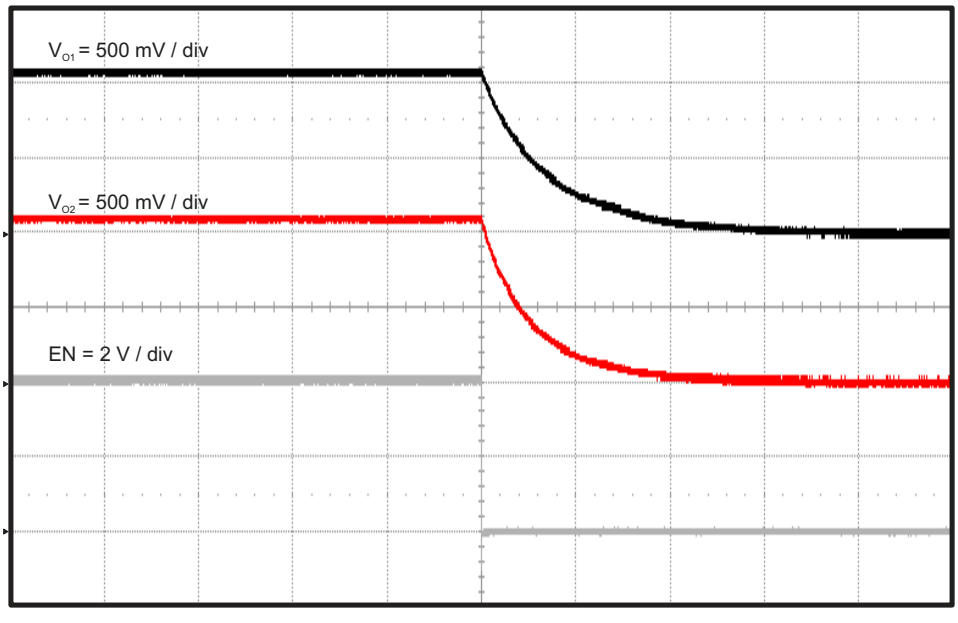

Figure 2-25. TPS563900EVM-574 Shut Down

3 Board Layout

This section provides a description of the TPS563900EVM-574 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS563900EVM-574 is shown in Figure 3-1 through Figure 3-5. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT1}, V_{OUT2} and switching nodes. Also on the top layer are connections for the remaining pins of the TPS563900 and a large area filled with ground. The internal layer-1 is dedicated to a power ground plane. The internal layer-2 contains additional V_{IN}, V_{OUT1} and V_{OUT2} copper fill areas as well as signal routing traces. The bottom layer contains a power ground plane only. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board .

The input decoupling capacitors (C1 and C2) and V7V LDO output capacitor C3 and bootstrap capacitors (C9 and C19) are all located as close to the IC as possible. Additionally, the voltage set point resistor divider components are kept close to the IC. The voltage divider network ties to the output voltages at the point of regulation, the copper V_{OUT1} and V_{OUT2} traces on the internal layer-2 near the J3 and J4 output connectors respectively. For the TPS563900, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply.

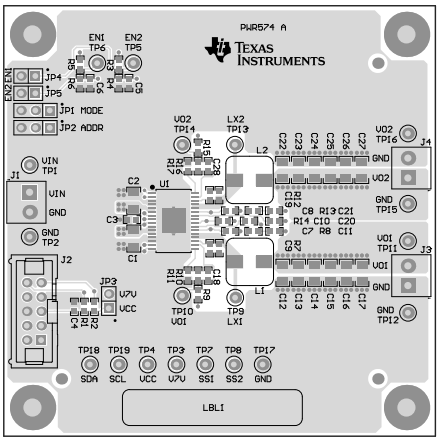

Figure 3-1. TPS563900EVM-574 Top-Side Assembly

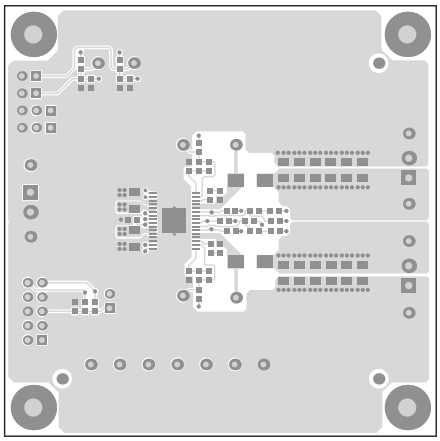

Figure 3-2. TPS563900EVM-574 Top-Side Layout

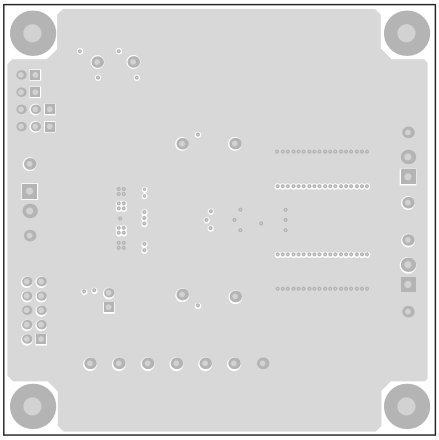

Figure 3-3. TPS563900EVM-574 Internal Layer-1 Layout

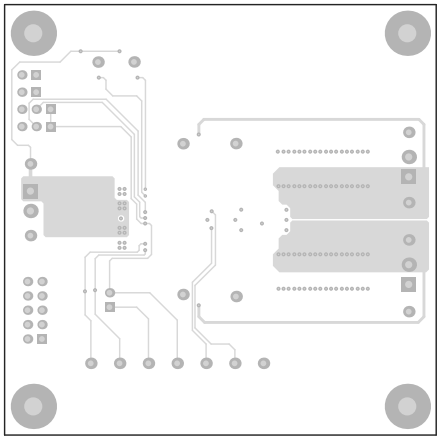

Figure 3-4. TPS563900EVM-574 Internal Layer-2 Layout

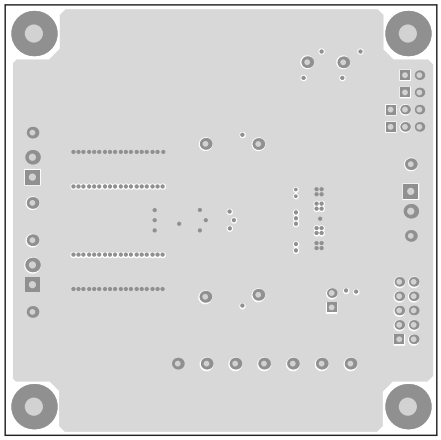

Figure 3-5. TPS563900EVM-574 Bottom-Side Layout

4 Schematic and Bill of Materials

This section presents the TPS563900EVM-574 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS563900EVM-574.

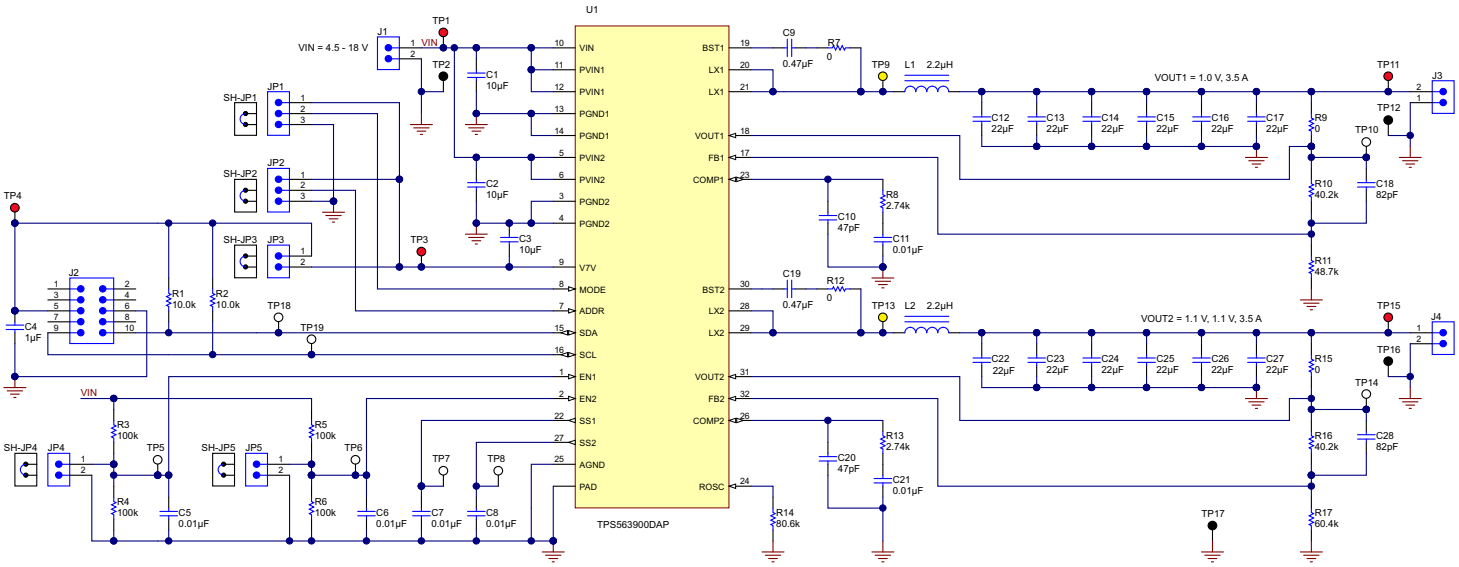

Figure 4-1. TPS563900EVM-574 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS563900EVM-574.

Table 4-1. TPS563900EVM-574 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C2	2	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 1206	1206	GRM31CR61E106KA12L	MuRata
C3	1	10uF	CAP, CERM, 10uF, 10V, +/-10%, C0G/NP0, 0603	0603	C1608X5R1A106M	TDK
C4	1	1uF	CAP, CERM, 1uF, 25V, +/-10%, X5R, 0603	0603	GRM188R61E105KA12D	MuRata
C5, C6, C7, C8, C11, C21	6	0.01uF	CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0603	0603	GRM188R71H103KA01D	MuRata
C9, C19	2	0.47uF	CAP, CERM, 0.47uF, 25V, +/-10%, X5R, 0603	0603	GRM188R61E474KA12D	MuRata
C10, C20	2	47pF	CAP, CERM, 47pF, 50V, +/-5%, C0G/NP0, 0603	0603	GRM1885C1H470JA01D	MuRata
C12, C13, C14, C15, C16, C17, C22, C23, C24, C25, C26, C27	12	22uF	CAP, CERM, 22uF, 10V, +/-10%, X5R, 1206	1206	GRM31CR61A226KE19L	MuRata
C18, C28	2	82pF	CAP, CERM, 82pF, 50V, +/-5%, C0G/NP0, 0603	0603	GRM1885C1H820JA01D	MuRata
H1, H2, H3, H4	4		Machine Screw, Round, 4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L 4-40 Nylon	Standoff	1902C	Keystone
J1, J3, J4	3		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
J2	1		Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH	5x2 Shrouded header	N2510-6002-RB	3M
JP1, JP2	2		Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	3x1 Header	TSW-103-07-G-S	Samtec
JP3, JP4, JP5	3		Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	2x1 Header	TSW-102-07-G-S	Samtec
L1, L2	2	2.2uH	Inductor, Shielded Drum Core, Superflux, 2.2uH, 9A, 0.0115 ohm, SMD	WE-HC4	744311220	Wurth Elektronik eiSos
LBL1	1		Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	PCB Label 1.25"H x 0.250"W	THT-13-457-10	Brady
R1, R2	2	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R3, R4, R5, R6	4	100k	RES, 100k ohm, 1%, 0.1W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R7, R9, R12, R15	4	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R8, R13	2	2.74k	RES, 2.74k ohm, 1%, 0.1W, 0603	0603	CRCW06032K74FKEA	Vishay-Dale
R10, R16	2	40.2k	RES, 40.2k ohm, 1%, 0.1W, 0603	0603	CRCW060340K2FKEA	Vishay-Dale
R11	1	48.7k	RES, 48.7k ohm, 1%, 0.1W, 0603	0603	CRCW060348K7FKEA	Vishay-Dale
R14	1	80.6k	RES, 80.6k ohm, 1%, 0.1W, 0603	0603	CRCW060380K6FKEA	Vishay-Dale
R17	1	60.4k	RES, 60.4k ohm, 1%, 0.1W, 0603	0603	CRCW060360K4FKEA	Vishay-Dale
SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5	5	1x2	Shunt, 2mm, Gold plated, Black	2mm Shunt, Closed Top	2SN-BK-G	Samtec
TP1, TP3, TP4, TP11, TP15	5	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP2, TP12, TP16, TP17	4	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP5, TP6, TP7, TP8, TP10, TP14, TP18, TP19	8	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
TP9, TP13	2	Yellow	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
U1	1		4.5V to 18V Input, 3A/3A Dual Synchronous Step-Down SWIFT Converter With I2C Controlled VID, DAP0032A	DAP0032A	TPS563900DAP	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A

4.3 Reference

1. *TPS563900 4.5-V to 18-V Input, 3.5-A/3.5-A Dual Synchronous Step-Down Converter With I²C Controlled VID* data sheet (SLVSCC7)

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2014) to Revision A (July 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	3
• Updated the user's guide title.	3

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