82078 64 PIN
CHMOS SINGLE-CHIP FLOPPY DISK CONTROLLER

- **Small Footprint and Low Height Packages**
- **Supports Standard 5.0V as well as Low Voltage 3.3V Platforms**
  - **— Selectable 3.3V and 5.0V Configuration**
  - **— 5.0V Tolerant Drive Interface**
- **Enhanced Power Management**
  - **— Application Software Transparency**
  - **— Programmable Powerdown Command**
  - **— Save and Restore Commands for Zero-Volt Powerdown**
  - **— Auto Powerdown and Wakeup Modes**
  - **— Two External Power Management Pins**
  - **— Consumes no Power when in Powerdown**
- **Integrated Analog Data Separator**
  - **— 250 Kbps**
  - **— 300 Kbps**
  - **— 500 Kbps**
  - **— 1 Mbps**
  - **— 2 Mbps**
- **Programmable Internal Oscillator**
- **Floppy Drive Support Features**
  - **— Drive Specification Command**
  - **— Media ID Capability Provides Media Recognition**
  - **— Drive ID Capability Allows the User to Recognize the Type of Drive**
  - **— Selectable Boot Drive**
  - **— Standard IBM and ISO Format Features**
  - **— Format with Write Command for High Performance in Mass Floppy Duplication**
- **Integrated Tape Drive Support**
  - **— Standard 1 Mbps/500 Kbps/ 250 Kbps Tape Drives**
  - **— New 2 Mbps Tape Drive Mode**
- **Perpendicular Recording Support for 4 MB Drives**
- **Integrated Host/Disk Interface Drivers**
- **Fully Decoded Drive Select and Motor Signals**
- **Programmable Write Precompensation Delays**
- **Addresses 256 Tracks Directly, Supports Unlimited Tracks**
- **16 Byte FIFO**
- **Single-Chip Floppy Disk Controller Solution for Portables and Desktops**
  - **— 100% PC AT* Compatible**
  - **— 100% PS/2* Compatible**
  - **— 100% PS/2 Model 30 Compatible**
  - **— Fully Compatible with Intel386™ SL Microprocessor SuperSet**
- **Integrated Drive and Data Bus Buffers**
- **Available in 64 Pin QFP Package**

The 82078, a 24 MHz crystal, a resistor package, and a device chip select implements a complete solution. All programmable options default to 82078 compatible values. The dual PLL data separator has better performance than most board level/discrete PLL implementations. The FIFO allows better system performance in multi-master (e.g., Microchannel, EISA).

The 82078 maintains complete software compatibility with the 82077SL/82077AA/8272A floppy disk controllers. It contains programmable power management features while integrating all of the logic required for floppy disk control. The power management features are transparent to any application software. There are two versions of 82078 floppy disk controllers, the 82078SL and 82078-1.

The 82078 is fabricated with Intel's advanced CHMOS III technology and is also available in a 44-lead QFP package.

*Other brands and names are the property of their respective owner.

October 1995 **Order Number: 290475-004**

82078 64 Pin CHMOS Single-Chip Floppy Disk Controller

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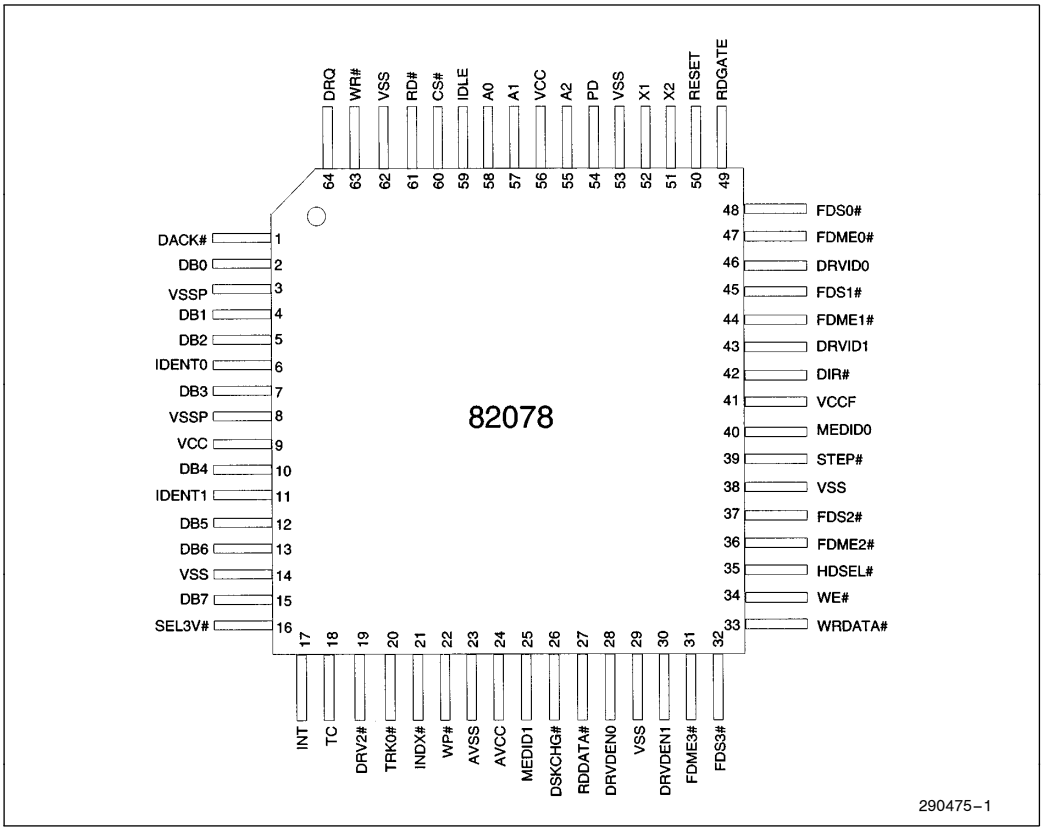


Figure 1-0. 82078 Pinout

Table 1-0. 82078 (64 Pin) Description

Symbol	Pin #	I/O	@ H/W Reset	Description
HOST INTERFACE				
RESET	50	I	N/A	**RESET:** A high level places the 82078 in a known idle state. All registers are cleared except those set by the Specify command.
A0 A1 A2	58 57 55	I	N/A	**ADDRESS:** Selects one of the host interface registers: **A2 A1 A0 Access Register** 0 0 0 R Status Register A SRA 0 0 1 R/W Status Register B SRB 0 1 0 R/W Digital Output Register DOR 0 1 1 R/W Tape Drive Register TDR 1 0 0 R Main Status Register MSR 1 0 0 W Data Rate Select Register DSR 1 0 1 R/W Data Register (FIFO) FIFO 1 1 0 Reserved 1 1 1 R Digital Input Register DIR 1 1 1 W Configuration Control Register CCR
CS#	60	I	N/A	**CHIP SELECT:** Decodes the base address range and qualifies RD# and WR#.

Table 1-0. 82078 (64 Pin) Description (Continued)

Symbol	Pin #	I/O	@ H/W Reset	Description
HOST INTERFACE (Continued)				
RD#	61	I	N/A	**READ:** Read control signal for data transfers from the floppy drive to the system.
WR#	63	I	N/A	**WRITE:** Write control signal for data transfers to the floppy drive from the system.
DRQ	64	O		**DMA REQUEST:** Requests service from a DMA controller. Normally active high, but will go to high impedance in AT and Model 30 modes when the appropriate bit is set in the DOR.
DACK#	1	I	N/A	**DMA ACKNOWLEDGE:** Control input that qualifies the RD#, WR# inputs in DMA cycles. Normally active low, but is disabled in AT and Model 30 modes when the appropriate bit is set in the DOR.
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	2 4 5 7 10 12 13 15	I/O		**DATA BUS:** 12 mA data bus.
IDENT0 IDENT1	6 11	I	N/A	**IDENTITY:** These inputs decode between the several operation modes available to the user. These pins have no effect on the DRVDEN pins. **IDENT0 IDENT1 INTERFACE** 1 1 AT mode 1 0 ILLEGAL 0 1 PS/2 mode 0 0 Model 30 **AT MODE:** Major options are: enables DMA gate logic, TC is active high, Status Register B is available based on a bit the powerdown command. **PS/2 MODE:** Major options are: no DMA gate logic, TC is active low, Status Registers A & B are available. **MODEL 30 MODE:** Major options are: enable DMA gate logic, TC is active high, Status Registers A & B are available.
INT	17	O		**INTERRUPT:** Signals a data transfer in non-DMA mode and when status is valid. Normally active high, but goes to high impedance when the appropriate bit is set in the DOR.
TC	18	I	N/A	**TERMINAL COUNT:** Control line from a DMA controller that terminates the current disk transfer. TC is effective only when qualified by DACK#. This input is active high in the AT, and Model 30 modes when the appropriate bit is set in the DOR.
X1 X2	52 51		N/A	**EXTERNAL CLOCK OR CRYSTAL:** Connection for a 24 MHz fundamental mode parallel resonant crystal. X1 can also be driven by an external clock (external oscillator) which can be either at 48 MHz or 24 MHz. If external oscillator is used then the PDOSC bit can be set to turn off the internal oscillator. Also, if a 48 MHz exernal oscillator is used then the CLK48 bit must be set in the enhanced CONFIGURE command.

Table 1-0. 82078 (64 Pin) Description (Continued)

Symbol	Pin #	I/O	@ H/W Reset	Description
POWER MANAGEMENT				
SEL3V#	16	I	N/A	**SELECT 3.3V:** This is a control pin that is used to select between 3.3V operation and 5.0V operation. This is an active low signal and selects 3.3V mode of operation when tied to ground.
PD	54	O		**POWERDOWN:** This pin is active high whenever the part is in powerdown state, either via DSR POWERDOWN bit or via the Auto Powerdown Mode. This pin can be used to disable an external oscillator's output.
IDLE	59	O		**IDLE:** This pin indicates that the part is in the IDLE state and can be powered down. IDLE state is defined as MSR = 80H, INT = 0, and the head being ''unloaded'' (as defined in Section 4.0, Power Management Features). Whenever the part is in this state, IDLE pin is active high. If the part is powered down by the Auto Powerdown Mode, IDLE pin is set high and if the part is powered down by setting the DSR POWERDOWN bit, IDLE pin is set low.
PLL SECTION				
RDDATA#	27	I	N/A	**READ DATA:** Serial data from the floppy disk.
RDGATE	49	O		**READ GATE:** This signal is basically used for diagnostic purposes.
DISK CONTROL				
DRV2#	19	I	N/A	**DRIVE2:** This is an active low signal that indicates whether a second drive is installed and is reflected in SRA.
TRK0#	20	I	N/A	**TRACK0:** This is an active low signal that indicates that the head is on track 0.
INDX#	21	I	N/A	**INDEX:** This is an active low signal that indicates the beginning of the track.
WP#	22	I	N/A	**WRITE PROTECT:** This is an active low signal that indicates whether the floppy disk in the drive is write protected.
MEDID1 MEDID0	25 40	I	N/A	**MEDIA ID:** These are active high signals that are output from the drive to indicate the density type of the media installed in the floppy drive. These should be tied low if not being used.
DSKCHG#	26	I	N/A	**DISK CHANGE:** This is an input from the floppy drive reflected in the DIR.
DRVDEN0 DRVDEN1	28 30	O		**DRIVE DENSITY:** These signals are used by the floppy drive to configure the drive for the appropriate media.
FDME3# FDME2# FDME1# FDME0#	31 36 44 47	O		**FLOPPY DRIVE MOTOR ENABLE:** Decoded motor enables for drives 0 to 3. The motor enable pins are directly controlled via the DOR and are a function of the mapping based on BOOTSEL bits in the TDR.
FDS3# FDS2# FDS1# FDS0#	32 37 45 48	O		**FLOPPY DRIVE SELECT:** Decoded floppy drive selects for drives 0 to 3. These outputs are decoded from the select bits in the DOR and are a function of the mapping based on BOOTSEL bits in the TDR.
WRDATA#	33	O		**WRITE DATA:** MFM serial data to the drive. Precompensation value is selectable through software.

Table 1-0. 82078 (64 Pin) Description (Continued)

Symbol	Pin #	I/O	@ H/W Reset	Description
DISK CONTROL (Continued)				
WE#	34	O		**WRITE ENABLE:** Floppy drive control signal that enables the head to write onto the floppy disk.
HDSEL#	35	O		**HEAD SELECT:** Selects which side of the floppy disk is to be used for the corresponding data transfer. It is active low and an active level selects head 1, otherwise it defaults to head 0.
STEP#	39	O		**STEP:** Supplies step pulses to the floppy drive to move the head between tracks.
DIR#	42	O		**DIRECTION:** It is an active low signal which controls the direction the head moves when a step signal is present. The head moves inwards towards the center if this signal is active.
DRVID0 DRVID1	46 43	I	N/A	**DRIVE ID:** These signals are input from the floppy drive and indicate the type of drive being used. These should be tied low if not being used.
POWER AND GROUND SIGNALS				
V_{CCF}	41		N/A	**VOLTAGE:** +5V for 5V floppy drive and 3.3V for 3.3V floppy drive.*
V_{CC}	9 56		N/A	**VOLTAGE:** +5V or 3.3V
V_{SSP}	3 8		N/A	**GROUND:** 0V
V_{SS}	14 29 38 53 62		N/A	**GROUND:** 0V
AV_{CC}	24		N/A	**ANALOG VOLTAGE**
AV_{SS}	23		N/A	**ANALOG GROUND**

***NOTE:**
The digital power supply V_{CC} and the analog power supply AV_{CC} should either be the same or regulated to be within 0.1V of either.

1.0 INTRODUCTION

The 82078, a 24 MHz (or 48 MHz) oscillator, a resistor package and a chip select implement a complete design. The power management features of the 82078 are transparent to application software, the 82078 seems awake to the software even in power-down mode. All drive control signals are fully decoded and have 24 mA (12 mA @ 3.3V) drive buffers. Signals returned from the drive are sent through on-chip input buffers with hysteresis for noise immunity. The integrated analog data separator needs no external compensation of components, yet allows for wide motor variation with exceptionally low soft error rates. The microprocessor interface has 12 mA drive buffers on the data bus plus 100% hardware register compatibility for PC-AT and Microchannel systems. The 16-byte FIFO with programmable thresholds is extremely useful in multi-master systems (Micro-Channel, EISA) or systems with large bus latency.

The 82078 features:

- 3.3V operation
- Small QFP package
- 2 Mbps data rate for tape drives
- Register enhancements from the 82077SL

Several pin changes accommodate the reduced pin count (from the 68 pin 82077SL) and the added features. Functional compatibility refers to software transparency between 82077SL/AA and the 82078. The 64 pin part will implement a superset of the features required to support all platforms, but is not pin to pin compatible to the 82077SL.

The 82078SL is capable of operating at both 3.3V and 5.0V. The 82078-1 only operates at 5.0V but has an available 2 Mbps tape drive data rate. All other features are available on both parts.

Part Specification	3.3V	5.0V	2 Mbps Data Rate
82078SL	X	X	
82078-1		X	X

Figure 1-1 is a block diagram of the 82078.

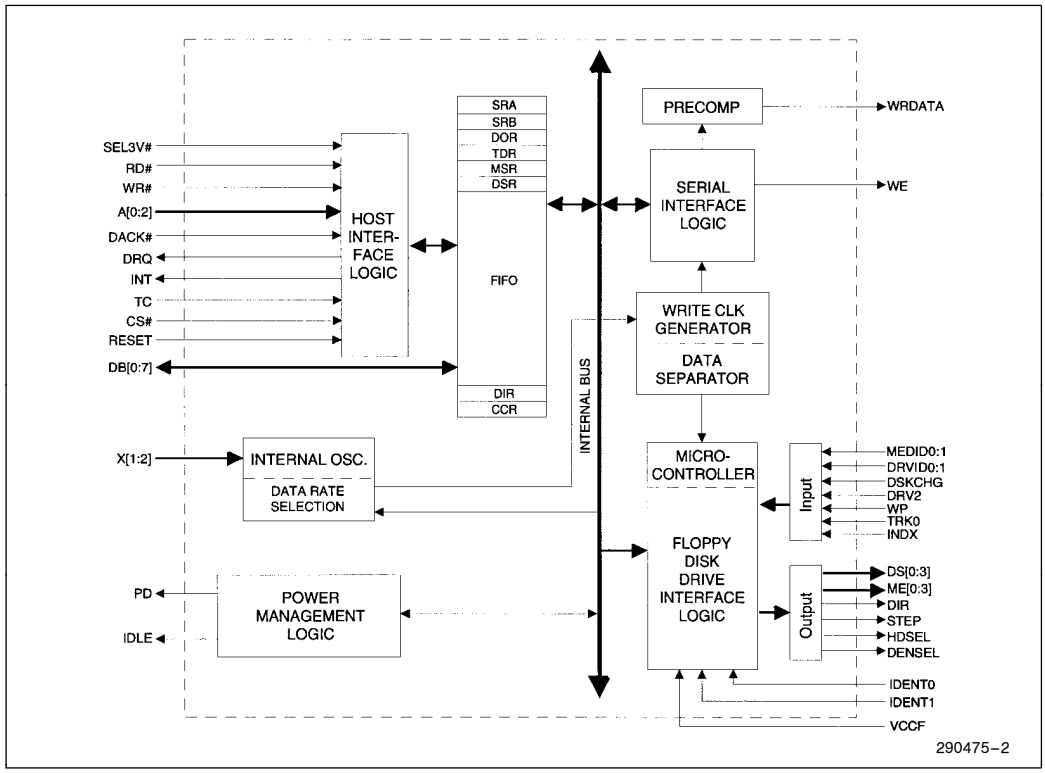


Figure 1-1. 82078 Block Diagram

2.0 MICROPROCESSOR INTERFACE

The interface consists of the standard asynchronous signals: RD#, WR#, CS#, A0–A2, INT, DMA control and a data bus. The address lines select between configuration registers, the FIFO and control/status registers. This interface can be switched between PC AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC-AT.

2.1 Status, Data and Control Registers

As shown below, the base address range is supplied via the CS# pin. For PC-AT or PS/2 designs, the primary and secondary address ranges are 3F0 Hex to 3F7 Hex and 370 Hex to 377 Hex respectively.

A2	A1	A0	Access Type	Register	
0	0	0	R	Status Register A	SRA
0	0	1	R/W	Status Register B	SRB
0	1	0	R/W	Digital Output Register	DOR
0	1	1	R/W	Tape Drive Register	TDR
1	0	0	R	Main Status Register	MSR
1	0	0	W	Data Rate Select Register	DSR
1	0	1	R/W	Data (First In First Out)	FIFO
1	1	0		Reserved	
1	1	1	R	Digital Input Register	DIR
1	1	1	W	Configuration Control Register	CCR

In the following sections, the various registers are shown in their powerdown state. The ''UC'' notation stands for a value that is returned without change from the active mode. The notation ''*'' means that the value is reflecting the required status (for powerdown). ''n/a'' means not applicable. ''X'' indicates that the value is undefined.

2.1.1 STATUS REGISTER A (SRA, PS/2 MODE)

This register is read-only and monitors the state of the interrupt pin and several disk interface pins. This register is part of the register set, and is not accessible in PC-AT mode.

This register can be accessed during powerdown state without waking up the 82078 from its powerdown state.

Bits	7	6	5	4	3	2	1	0
Function	INT PENDING	DRV2#	STEP	TRK0#	HDSEL	INDX#	WP#	DIR
H/W Reset State	0	DRV2#	0	TRK0#	0	INDX#	WP#	0
Auto PD State	0*	UC	0*	1	0*	1	1	0*

The INT PENDING bit is used by software to monitor the state of the 82078 INTERRUPT pin. By definition, the INT PENDING bit is low in powerdown state. The bits reflecting the floppy disk drive input pins (TRK0, INDEX, and WP) are forced inactive. Floppy disk drive outputs (HDSEL, STEP, and DIR) also go to their inactive, default state.

As a read-only register, there is no default value associated with a reset other than some drive bits will change with a reset. The INT PENDING, STEP, HDSEL, and DIR bits will be low after reset.

2.1.2 STATUS REGISTER A (SRA, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	INT PENDING	DRQ	STEP F/F	TRK0	HDSEL#	INDX#	WP	DIR#
H/W Reset State	0	0	0	TRK0	1	INDX#	WP	1
Auto PD State	0*	0*	0	0	1*	0	0	1*

This register has the following changes in PS/2 Model 30 Mode. Disk interface pins (Bits 0, 1, 2, 3, and 4) are inverted from PS/2 Mode. The DRQ bit monitors the status of the DMA Request pin. The STEP bit is latched with the Step output going active and is cleared with a read to the DIR register, Hardware or Software RESET.

The DRQ bit is low by definition for 82078 to be in powerdown. The bits reflecting the floppy disk drive input pins (TRK0, INDEX, and WP) are forced to reflect an inactive state. The floppy disk drive outputs (HDSEL, STEP, and DIR) also go to their inactive, default state.

2.1.3 STATUS REGISTER B (SRB, ENHANCED AT/EISA)

In the AT/EISA mode the SRB is made available whenever the EREG EN bit in the auto powerdown command is set. The register functionality is defined as follows (bits 7 through 3 are reserved):

PD and IDLE reflect the values on the corresponding pins. The signal on the IDLE pin can be masked by setting IDLEMSK bit high in this register. The IDLE bit will remain unaffected. Since some systems will use the IDLE pin to provide interrupt to the SMM power management, its disabling allows less external interrupt logic and reduction in board space. Only hardware reset will clear the IDLEMSK bit to zero.

When the IDLEMSK bit is set, the user cannot distinguish between auto powerdown and DSR powerdown (i.e., by using the IDLE pin).

IDLEMSK	IDLE (pin)
0	unmasked
1	masked

SRB								
Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R	RSVD	RSVD	RSVD	RSVD	RSVD	IDLEMSK	PD	IDLE
H/W Reset	X	X	X	X	X	0	PD	IDLE
Auto PD	X	X	X	X	X	UC	UC	UC
W	0	0	0	0	0	IDLEMSK	RSVD	RSVD
H/W Reset	n/a	n/a	n/a	n/a	n/a	0	n/a	n/a
Auto PD	n/a	n/a	n/a	n/a	n/a	UC	n/a	n/a

2.1.4 STATUS REGISTER B (SRB, PS/2 MODE)

Bits	7	6	5	4	3	2	1	0
Function	1	1	DRIVE SEL 0	WRDATA TOGGLE	RDDATA TOGGLE	WE	MOT EN1	MOT EN2
H/W Reset State	1	1	0	0	0	0	0	0
Auto PD State	1	1	UC	0	0	0*	0	0

As the only drive input, RDATA TOGGLE's activity reflects the level as seen on the cable.

The two TOGGLE bits do not read back the state of their respective pins directly. Instead, the pins drive a Flip/Flop which produces a wider and more reliable read pulse. Bits 6 and 7 are undefined and always return to a 1.

After any reset, the activity on the TOGGLE pin is cleared. Drive select and Motor bits cleared by the RESET pin and not software resets.

2.1.5 STATUS REGISTER B (SRB, MODEL 30 MODE)

Bits	7	6	5	4	3	2	1	0
Function	DRV2#	DS1#	DS0#	WRDATA F/F	RDDATA F/F	WE F/F	DS3#	DS2#
H/W Reset State	DRV2#	1	1	0	0	0	1	1
Auto PD State	UC	UC	UC	0	0	0*	UC	UC

This register has the following changes in Model 30 Mode. Bits 0, 1, 5, and 6 return the decoded value of the Drive Select bits in the DOR register. Bits 2, 3, and 4 are set by their respective active going edges and are cleared by reading the DIR register. The WRDATA bit is triggered by raw WRDATA signals and is not gated by WE. Bits 2, 3, and 4 are cleared to low level by either Hardware or Software RESET.

2.1.6 DIGITAL OUTPUT REGISTER (DOR)

The Digital Output Register contains the drive select and motor enable bits, a reset bit and a DMA GATE# bit.

Bits	7	6	5	4	3	2	1	0
Function	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMA GATE#	RESET#	DRIVE SEL1	DRIVE SEL2
H/W Reset State	0	0	0	0	0	0	0	0
Auto PD State	0*	0*	0*	0*	UC	1*	UC	UC

The MOT ENx bits directly control their respective motor enable pins (FDME0–3). The DRIVE SELx bits are decoded to provide four drive select lines and only one may be active at a time. Standard programming practice is to set both MOT ENx and DRIVE SELx bits at the same time.

Table 2-1 lists a set of DOR values to activate the drive select and motor enable for each drive.

Table 2-1. Drive Activation Value

Drive	DOR Value
0	1CH
1	2DH
2	4EH
3	8FH

The DMAGATE# bit is enabled only in PC-AT and Model 30 Modes. If DMAGATE# is set low, the INT and DRQ outputs are tri-stated and the DACK# and TC inputs are disabled. DMAGATE# set high will enable INT, DRQ, TC, and DACK# to the system. In PS/2 Mode DMAGATE# has no effect upon INT, DRQ, TC, or DACK# pins, they are always active.

The DOR reset bit and the Motor Enable bits have to be inactive when the 82078 is in powerdown. The DMAGATE# and DRIVE SEL bits are unchanged. During powerdown, writing to the DOR does not awaken the 82078 with the exception of activating any of the motor enable bits. Setting the motor enable bits active (high) will wake up the part.

This RESET# bit clears the basic core of the 82078 and the FIFO circuits when the LOCK bit is set to ''0'' (see Section 5.3.2 for LOCK bit definitions). Once set, it remains set until the user clears this bit. This bit is set by a chip reset and the 82078 is held in a reset state until the user clears this bit. The RESET# bit has no effect upon the register.

2.1.7 TAPE DRIVE REGISTER (TDR AT/EISA, PS/2, MODEL 30)

Bits	7	6	5	4	3	2	1	0
Function	—	—	—	—	—	—	TAPE SEL1	TAPE SEL0
H/W Reset State	—	—	—	—	—	—	0	0
Auto PD State	—	—	—	—	—	—	UC	UC

(—) means these bits are not writable and remain tri-stated if read.

This register allows the user to assign tape support to a particular drive during initialization. Any future references to that drive number automatically invokes tape support. Hardware reset clears this register; software resets have no effect. By default, the tape select bits are hardware RESET to zeros, making Drive 0 not available for tape support.

2.1.8 ENHANCED TAPE DRIVE REGISTER (TDR, AT, PS/2, MODEL 30, EREG EN = 1)

In the PS/2 and Model 30 mode and AT/EISA mode the extended TDR is made available only when the EREG EN bit is set, otherwise the bits are tri-stated. The register functionality is defined as follows:

TDR								
Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R	MEDID1	MEDID0	DRVID1	DRVID0	BOOTSEL1	BOOTSEL0	TAPESEL1	TAPESEL0
H/W Reset	MEDID1	MEDID0	DRVID1	DRVID0	0	0	0	0
Auto PD	UC	UC	UC	UC	UC	UC	UC	UC
W	0	0	0	0	BOOTSEL1	BOOTSEL0	TAPESEL1	TAPESEL0
H/W Reset	n/a	n/a	n/a	n/a	0	0	0	0
Auto PD	n/a	n/a	n/a	n/a	BOOTSEL1	BOOTSEL0	TAPESEL1	TAPESEL0

MEDID1, MEDID0 reflect the values on the respective pins. Similarly, the DRVID0, DRVID1 reflect the values on the DRVID1 and DRVID0 pins.

The TAPESEL1, TAPESEL0 functionality is retained as defined in the non-enhanced TDR, except that the application of boot drive restriction (boot drive cannot be a tape drive) depends on what drive selected is by the BOOTSEL1, BOOTSEL0 bits.

The BOOTSEL1, BOOTSEL0 are not reset by software resets and are decoded as shown below. These bits allow for reconfiguring the boot up drive and only reset by hardware reset. A drive can be enabled by remapping the internal DS0 and ME0 to one of the other drive select and motor enable lines (Refer to ''Selectable Boot Drives'' in the Design applications chapter). Once a non-default value for BOOTSEL1 and BOOTSEL0 is selected, all programmable bits are virtual designations of drives, i.e., it is the user's responsibility to know the mapping scheme detailed in the following table.

BOOTSEL1	BOOTSEL0	Mapping:
0	0	DS0 ⟶ FDS0, ME0 ⟶ FDME0 DS1 ⟶ FDS1, ME1 ⟶ FDME1 DS2 ⟶ FDS2, ME2 ⟶ FDME2
0	1	DS0 ⟶ FDS1, ME0 ⟶ FDME1 DS1 ⟶ FDS0, ME1 ⟶ FDME0 DS2 ⟶ FDS2, ME2 ⟶ FDME2
1	0	DS0 ⟶ FDS2, ME0 ⟶ FDME2 DS1 ⟶ FDS1, ME1 ⟶ FDME1 DS2 ⟶ FDS0, ME2 ⟶ FDME0
1	1	Reserved

2.1.9 DATARATE SELECT REGISTER (DSR)

Bits	7	6	5	4	3	2	1	0
Function	S/W RESET	POWER DOWN	PDOSC	PRE COMP2	PRE COMP1	PRE COMP0	DRATE SEL1	DRATE SEL0
H/W Reset State	0	0	0	0	0	0	1	0
Auto PD State	S/W RESET	POWER DOWN	PDOSC	PRE COMP2	PRE COMP1	PRE COMP0	DRATE SEL1	DRATE SEL0

This register ensures backward compatibility with the 82072 floppy controller and is write-only. Changing the data rate changes the timings of the drive control signals. To ensure that drive timings are not violated when changing data rates, choose a drive timing such that the fastest data rate will not violate the timing.

The PDOSC bit is used to implement crystal oscillator power management. The internal oscillator in the 82078 can be programmed to be either powered on or off via PDOSC. This capability is independent of the chip's powerdown state. Auto powerdown mode and powerdown via POWERDOWN bit has no effect over the power state of the oscillator.

In the default state the PDOSC bit is low and the oscillator is powered up. When this bit is programmed to a one, the oscillator is shut off. Hardware reset clears this bit to a zero. Neither of the software resets (via DOR or DSR) have any effect on this bit. Note, PDOSC should only be set high when the part is in the powerdown state, otherwise the part will not function correctly and must be hardware reset once the oscillator has turned back on and stabilized. Setting the PDOSC bit has no effect on the clock input to the 82078 (the X1 pin). The clock input is separately disabled when the part is powered down. The SAVE command checks the status of PDOSC, however, the RESTORE command will not restore the bit high.

S/W RESET behaves the same as DOR RESET except that this reset is self cleaning.

POWERDOWN bit implements direct powerdown. Setting this bit high will put the 82078 into the powerdown state regardless of the state of the part. The part is internally reset and then put into powerdown. No status is saved and any operation in progress is aborted. A hardware or software reset will exit the 82078 from this powerdown state.

PRECOMP 0-2 adjusts the WRDATA output to the disk to compensate for magnetic media phenomena known as bit shifting. The data patterns that are susceptible to bit shifting are well understood and the 82078 compensates the data pattern as it is written to the disk. The amount of pre-compensation is dependent upon the drive and media, but in most cases the default value is acceptable.

Table 2-2. Precompensation Delays

PRECOMP	Precompensation Delays	
DSR[432]	x1 @ 24 MHz	x1 @ 48 MHz if CLK48 = 1, enabled only @ 2 Mbps if CLK48 = 0, enabled at all data rates
111	0.00 ns–disabled	
001	41.67	20.84
010	83.34	41.67
011	125.00	62.5
100	166.67	83.34
101	208.33	104.17
110	250.00	125
000	DEFAULT	

Table 2-3. Default Precompensation Delays

Data Rate	Precompensation Delays (ns)
2 Mbps	20.84
1 Mbps	41.67
0.5 Mbps	125
0.3 Mbps	125
0.25 Mbps	125

The 82078 starts pre-compensating the data pattern starting on Track 0. The CONFIGURE command can change the track that pre-compensating starts on. Table 2-2 lists the pre-compensation values that can be selected and Table 2-3 lists the default pre-compensation values. The default value is selected if the three bits are zeroes.

DRATE 0-1 select one of the four data rates as listed in Table 2-4. The default value is 250 Kbps after a ''Hardware'' reset. Other ''Software'' Resets do not affect the DRATE or PRECOMP bits.

Table 2-4. Data Rates

DRATESEL1	DRATESEL0	DATA RATE
1	1	1 Mbps
0	0	500 Kbps
0	1	300 Kbps
1	0	250 Kbps

2.1.10 MAIN STATUS REGISTER (MSR)

Bits	7	6	5	4	3*	2	1	0
Function	RQM	DIO	NON DMA	CMD BSY	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY
H/W Reset State	0	X	X	X	X	X	X	X
Auto PD State	1	0	0	0	0	0	0	0

The Main Status Register is a read-only register and is used for controlling command input and result output for all commands.

RQM—Indicates that the host can transfer data if set to 1. No access is permitted if set to a 0.

DIO—Indicates the direction of a data transfer once RQM is set. A 1 indicates a read and a 0 indicates a write is required.

NON-DMA—This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfers and the reading of result bytes.

COMMAND BUSY—This bit is set to a one when a command is in progress. This bit goes active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (SEEK, RECALIBRATE commands), this bit returns to a 0.

DRV x BUSY—These bits are set to ones when a drive is in the seek portion of a command, including seeks and recalibrates.

Some example values of the MSR are:

- MSR = 80H; The controller is ready to receive a command.
- MSR = 90H; executing a command or waiting for the host to read status bytes (assume DMA mode).
- MSR = D0H; waiting for the host to write status bytes.

2.1.11 FIFO (DATA)

All command parameter information and disk data transfers go through the FIFO. The FIFO is 16 bytes in size and has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to an 8272A compatible mode after a ''Hardware'' reset (Reset via pin 32). ''Software'' Resets (Reset via DOR or DSR register) can also place the 82078 into 8272A compatible mode if the LOCK bit is set to ''0'' (See the definition of the LOCK bit), maintaining PC-AT hardware compatibility. The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 2-5 gives several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold\#} \times 1/\text{DATA RATE} \times 8 - 1.5\ \mu s = \text{DELAY}$$

Table 2-5. FIFO Threshold Examples

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	$1 \times 8\ \mu s - 1.5\ \mu s = 6.5\ \mu s$
2 bytes	$2 \times 8\ \mu s - 1.5\ \mu s = 14.5\ \mu s$
8 bytes	$8 \times 8\ \mu s - 1.5\ \mu s = 62.5\ \mu s$
15 bytes	$15 \times 8\ \mu s - 1.5\ \mu s = 118.5\ \mu s$

FIFO Threshold Examples	Maximum Delay to Servicing at 500 Kbps Data Rate
1 byte	$1 \times 16\ \mu s - 1.5\ \mu s = 14.5\ \mu s$
2 bytes	$2 \times 16\ \mu s - 1.5\ \mu s = 30.5\ \mu s$
8 bytes	$8 \times 16\ \mu s - 1.5\ \mu s = 126.5\ \mu s$
15 bytes	$15 \times 16\ \mu s - 1.5\ \mu s = 238.5\ \mu s$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the 82078 enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred. An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC.

2.1.12 DIGITAL INPUT REGISTER (DIR, PC-AT MODE)

This register is read only in all modes. In PC-AT mode only bit 7 is driven, all other bits remain tri-stated.

Bits	7	6	5	4	3	2	1	0
Function	DSK CHG	—	—	—	—	—	—	—
H/2 Reset State	DSK CHG	—	—	—	—	—	—	—
Auto PD State	0	—	—	—	—	—	—	—

(—) means these bits are tri-stated when read.

DSKCHG monitors the pin of the same name and reflects the opposite value seen on the disk cable. The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits remain tri-stated.

2.1.13 DIGITAL INPUT REGISTER (DIR, PS/2 MODE)

DIR								
R/W	7	6*	5*	4*	3	2	1	0
R	DSK CHG	IDLE	PD	IDLEMSK	1	DRATE SEL1	DRATE SEL0	HIGH DENS#
H/W Reset	DSK CHG	1	1	1	1	1	0	1
Auto PD	0	1	1	UC	1	UC	UC	UC

(*) These bits are only available when PS2 STAT = 1: Bits 5 and 6 show the status of PD (powerdown) and IDLE respectively. Bit 4 shows the status of IDLEMSK, this bit disables the IDLE pin when active.

Bit 3 returns a value of ''1'', and the DRATE SEL1–0 return the value of the current data rate selected (see Table 2-4 for values).

HIGHDENS# is low whenever the 500 Kbps or 1 Mbps data rates are selected. It is high when either 250 Kbps, 300 Kbps, or 2 Mbps is selected.

The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits (as applicable) remain unchanged.

The Drive Specification Command modifies the DRATE SEL bits. Refer to Table 6-2 for a description.

2.1.14 DIGITAL INPUT REGISTER (DIR, MODEL 30 MODE)

Bits	7	6*	5*	4*	3	2	1	0
Function	DSK CHG#	IDLE	PD	IDLEMSK	DMA GATE#	NOPREC	DRATE SEL1	DRATE SEL0
H/W Reset State	N/A	0	0	0	0	0	1	0
Auto PD State	1	1	1	UC	UC	UC	UC	UC

(*) These bits are only available when PS2 STAT = 1: Bits 5 and 6 show the status of PD (powerdown) and IDLE respectively. Bit 4 shows the status of IDLEMSK, this bit disables the IDLE pin when active. Bit 7 (DSKCHG) is inverted in Model 30 Mode.

The DSKCHG# bit is forced inactive along with all the inputs from the floppy disk drive. All the other bits (as applicable) remain unchanged.

The Drive Specification Command modifies the DRATE SEL bits. Refer to Table 6-2 for information regarding the mapping of these bits.

Bit 3 reflects the value of DMAGATE# bit set in the DOR register.

Bit 2 reflects the value of NOPREC bit set in the CCR register.

2.1.15 CONFIGURATION CONTROL REGISTER (CCR, PC AT and PS/2 MODES)

This register sets the datarate and is write only.

Bits	7	6	5	4*	3	2	1	0
Function	—	—	—	IDLEMSK	—	—	DRATE SEL1	DRATE SEL0
H/W Restate State	—	—	—		—	—	1	0
Auto PD State	—	—	—	IDLEMSK	—	—	DRATE SEL1	DRATE SEL0

(*) This bit is enabled only when PS2 STAT = 1 (Powerdown Mode). Refer to the table in the Data Rate Select Register for values. Unused bits should be set to 0. IDLEMSK is not available in the CCR for PC AT mode. In PC AT, IDLEMSK is available in the SRB.

2.1.16 CONFIGURATION CONTROL REGISTER (CCR, MODEL 30 MODE)

Bits	7	6	5	4*	3	2	1	0
Function	—	—	—	IDLEMSK	—	NOPREC	DRATE SEL1	DRATE SEL0
H/W Reset State	—	—	—	0	—	0	1	0
Auto PD State	—	—	—	UC	—	UC	UC	UC

(*) This bit is enabled only when PS2 STAT = 1 (Powerdown Mode). NOPREC has no function, and is reset to ''0'' with a Hardware RESET only.

2.2 Reset

There are three sources of reset on the 82078; the RESET pin, a reset generated via a bit in the DOR and a reset generated via a bit in the DSR. All resets take the 82078 out of the powerdown state.

In entering the reset state, all operations are terminated and the 82078 enters an idle state. Activating reset while a disk write activity is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, and the 82078 waits for a new command. Drive polling will start unless disabled by a new CONFIGURE command.

2.2.1 RESET PIN ("HARDWARE") RESET

The RESET pin is a global reset and clears all registers except those programmed by the SPECIFY command. The DOR Reset bit is enabled and must be cleared by the host to exit the reset state.

2.2.2 DOR RESET vs DSR RESET ("SOFTWARE" RESET)

These two resets are functionally the same. The DSR Reset is included to maintain 82072 compatibility. Both will reset the 82072 core which affects drive status information. The FIFO circuits will also be reset if the LOCK bit is a "0" (see definition of the LOCK bit). The DSR Reset clears itself automatically while the DOR Reset requires the host to manually clear it. DOR Reset has precedence over the DSR Reset. The DOR Reset is set automatically upon a pin RESET. The user must manually clear this reset bit in the DOR to exit the reset state.

The t30a specification in the A.C. Specifications gives the minimum amount of time that the DOR reset must be held active. This amount of time that the DOR reset must be held active is dependent upon the data rate. The 82078 requires that the DOR reset bit must be held active for at least 0.5 μs at 250 Kbps. This is less than a typical ISA I/O cycle time.

2.3 DMA Transfers

DMA transfers are enabled with the SPECIFY command and are initiated by the 82078 by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting DACK# and addresses need not be valid (CS# can be held inactive during DMA transfers).

3.0 DRIVE INTERFACE

The 82078 has integrated all of the logic needed to interface to a floppy disk or a tape drive which use floppy interface. All drive outputs have 24 mA drive capability and all inputs use a receive buffer with hysteresis. The internal analog data separator requires no external components, yet allows for an extremely wide capture range with high levels of read-data jitter, and ISV. The designer needs only to run the 82078 disk drive signals to the disk or tape drive connector.

3.1 Cable Interface

Generally, 5.25″ drive uses open collector drivers and 3.5″ drives (as used on PS/2) use totem-pole drivers. The output buffers on the 82078 do not change between open collector or totem-pole, they are always totem-pole.

DRVDEN0 and DRVDEN1 connect to pins 2 and 6 or 33 (on most disk drives) to select the data rate sent from the drive to the 82078. The polarity of DRVDEN0 and DRVDEN1 can be programmed through the Drive Specification command (see the command description for more information).

When the 82078SL is operating at 3.3V, the floppy drive interface can be configured to either 5.0V or 3.3V, via the V_{CCF} (pin 41). The drive interface follows the voltage level on V_{CCF}. A selectable drive interface allows the system designer the greatest flexibility when designing a low voltage system.

3.2 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When lock is achieved, the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called Data Window, is used to internally sample the serial data. One state of Data Window is used to sample the data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

To support reliable disk reads the data separator must track fluctuations in the read data frequency. Frequency errors primarily arise from two sources: motor rotation speed variation and instantaneous speed variation (ISV). A second condition, and one that opposes the ability to track frequency shifts is the response to bit jitter.

The internal data separator consists of two analog phase lock loops (PLLs) as shown in Figure 3-1. The two PLLs are referred to as the reference PLL and the data PLL. The reference PLL (the master PLL) is used to bias the data PLL (the slave PLL). The reference PLL adjusts the data PLL's operating point as a function of process, junction temperature and supply voltage. Using this architecture it was possible to eliminate the need for external trim components.

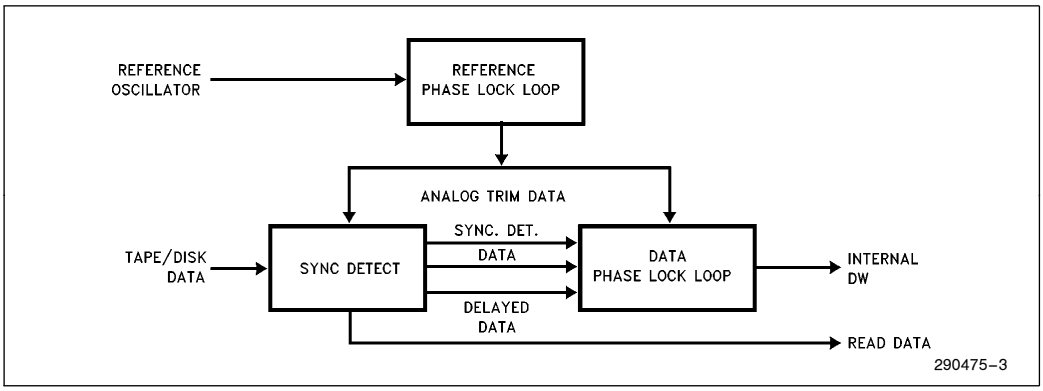


Figure 3-1. Data Separator Block Diagram

PHASE LOCK LOOP OVERVIEW

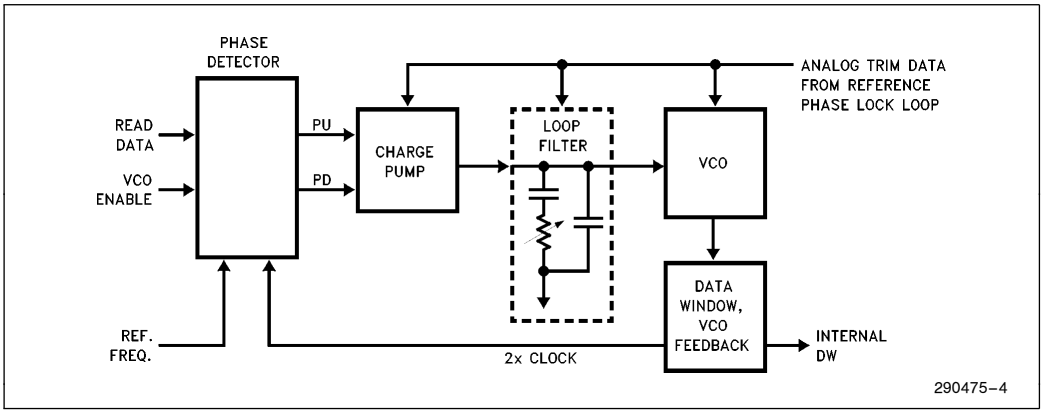


Figure 3-2. Data PLL

Figure 3-2 shows the data PLL. The reference PLL has control over the loop gain by its influence on the charge pump and the VCO. In addition the reference PLL controls the loop filter time constant. As a result the closed loop transfer function of the data PLL is controlled, and immune to the first order, to environmental factors and process variation.

Systems with analog PLLs are often very sensitive to noise. In the design of this data separator many steps were taken to avoid noise sensitivity problems. The analog section of the chip has a separate VSS pin (AVSS) which should be connected externally to a noise free ground. This provides a clean basis for VSS referenced signals. In addition many analog circuit features were employed to make the overall system as insensitive to noise as possible.

3.2.1 JITTER TOLERANCE

The jitter immunity of the system is dominated by the data PLL's response to phase impulses. This is measured as a percentage of the theoretical data window by dividing the maximum readable bit shift by a ¼ bit cell distance. For instance, if the maximum allowable bit shift is 300 ns for a 500 Kbps data stream, the jitter tolerance is 60%.

3.2.2 LOCKTIME (tLOCK)

The lock, or settling time of the data PLL is designed to be 64 bit times (8 sync bytes). The value assumes that the sync field jitter is 5% the bit cell or less. This level of jitter is realistic for a constant bit pattern. Intersymbol interference should be equal, thus nearly eliminating random bit shifting.

3.2.3 CAPTURE RANGE

Capture Range is the maximum frequency range over which the data separator will acquire phase lock with the incoming RDDATA signal. In a floppy disk environment, this frequency variation is composed of two components: drive motor speed error and ISV. Frequency is a factor which may determine the maximum level of the ISV (Instantaneous Speed Variation) component. In general, as frequency increases the allowed magnitude of the ISV component will decrease. When determining the capture range requirements, the designer should take the maximum amount of frequency error for the disk drive and double it to account for media switching between drives.

3.3 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. The shifting of bits is a known phenomena of magnetic media and is dependent upon the disk media AND the floppy drive.

The 82078 monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late (or not at all) relative to the surrounding bits. Figure 3-3 is a block diagram of the internal circuit.

The top block is a 13-bit shift register with the no delay tap being in the center. This allows 6 levels of early and late shifting with respect to nominal. The shift register is clocked at the main clock rate (24 MHz). The output is fed into 2 multiplexors one for early and one for late. A final stage of multiplexors combines the early, late and normal data stream back into one which is the WRDATA output.

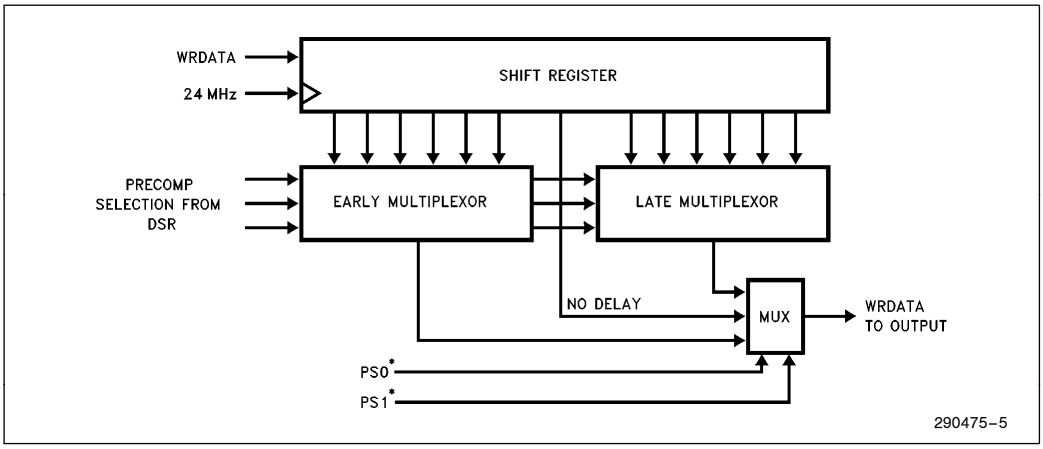


Figure 3-3. Precompensation Block Diagram

4.0 POWER MANAGEMENT FEATURES

The 82078 contains power management features that makes it ideal for design of portable personal computers. In addition to all of the power management features the 82078SL also operates at 3.3V. These features can be classified into power management of the part and that of the internal oscillator. The powerdown of the part is done independently of the internal oscillator in the 82078.

4.1 Power Management Scheme

The 82078 supports two powerdown modes, direct powerdown and automatic powerdown. Direct powerdown refers to direct action by the software to powerdown without dependence on external factors. Automatic powerdown results from 82078's monitoring of the current conditions according to a previously programmed mode. Any hardware reset disables the automatic POWERDOWN command, however, software resets have no effect on the command. The 82078 also supports powerdown of its internal crystal oscillator independent of the powerdown modes described above. By setting bit 5 (PDOSC) in the DSR register, the internal oscillator is turned off. This bit has sole control of the oscillator powerdown, allowing the internal clock to be turned off when an external oscillator is used.

4.2 3.3V Support for Portable Platforms

The portable market share of the personal computing market has increased significantly. To improve power conservation on portable platforms, designs are migrating from 5.0V to 3.3V. Intel's 82078SL allows designers to incorporate 3.3V floppy disk controller support in their systems. The 82078SL has a SEL3V# pin to allow selection of either 5.0V or 3.3V operation. In order to support the slower migration of floppy drives to 3.3V and allow system vendors to use standard 5.0V floppy drive inventory, the 82078SL accommodates a 5.0V tolerant floppy drive interface. This is achieved by changing the floppy drive's interface power supply, VCCF between 5.0V and 3.3V supplies. The 82078SL's 3.3V D.C. specification conforms to the JEDEC standard that describes the operating voltage levels for Integrated Circuits operating at 3.3V $\pm$0.3V. The 82077SL also maintains compatibility to 5.0V A.C. specifications.

4.3 Oscillator Power Management

The 82078 supports a built-in crystal oscillator that can be programmed to be either powered down or active, independent of the power state of the chip. This capability is implemented by the PDOSC bit in the DSR. When PDOSC is set low, the internal oscillator is on, it is off when the bit is high. Note, a DSR powerdown does not turn off the oscillator.

When the external oscillator is used, power can be saved by turning off the internal oscillator. If the internal oscillator is used, the oscillator may be powered up (even when the rest of the chip is powered off) allowing the chip to wake up quickly and in a stable state. It is recommended to keep the internal oscillator on even when in the powerdown state. The main reason for this is that the recovery time of the oscillator during wake up may take tens of milliseconds under the worst case, which may create problems with any sensitive application software. In a typical application the internal oscillator should be on unless the system goes into a power saving or standby mode (such a mode request would be made by a system time out or by a user). In this case, the system software would take over and must turn on the oscillator sufficiently ahead of awakening the part.

In the case of the external oscillators, the power up characteristics are similar. If the external source remains active during the time the 82078 is powered down, then the recovery time effect is minimized. The PD pin can be used to turn off the external source. While the PD pin is active, the 82078 does not require a clock source. However, when the PD pin is inactive, the clocking source, once it starts oscillating, must be completely stable to ensure that the 82078 operates properly.

4.4 Part Power Management

This section deals with the power management of the rest of the chip excluding the oscillator. This section explains powerdown modes and wake up modes.

4.4.1 DIRECT POWERDOWN

Direct powerdown is conducted via the POWERDOWN bit in the DSR register (bit 6). Programming this bit high will powerdown 82078. All status is lost if this type of powerdown mode is used. The part can exit powerdown from this mode via any hardware or software reset. This type of powerdown overrides the automatic powerdown. When the part is in automatic powerdown and the DSR powerdown is issued, the previous status of the part is lost and the 82078 resets to its default values.

4.4.2 AUTO POWERDOWN

Automatic powerdown is conducted via a ''Powerdown Mode'' command. There are four conditions required before the part will enter powerdown. All these conditions must be true for the part to initiate the powerdown sequence. These conditions follow:

1. The motor enable pins FDME[0:3] must be inactive.
2. The part must be idle; this is indicated by MSR = 80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupt).
3. The head unload timer (HUT, explained in the SPECIFY command) must have expired.
4. The auto powerdown timer must have timed out.

The command can be used to enable powerdown by setting the AUTO PD bit in the command to high. The command also provides a capability of programming a minimum power up time via the MIN DLY bit in the command. The minimum power up time refers to a minimum amount of time the part will remain powered up after being awakened or reset. An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down provided all the remaining conditions are met. Any software reset will reinitialize the timer. Changing of data rate extends the auto powerdown timer by up to 10 ms, but only if the data rate is changed during the countdown.

Disabling the auto powerdown mode cancels the timers and holds the 82078 out of auto powerdown.

The IDLE pin can be masked via the IDLEMSK bit in Status Register B (Enhanced AT/EISA). When in PS/2 mode, the PS/2 STAT bit in the Powerdown Command can be set to enable PD and IDLE bits in the DIR register (bits 5 and 6) and IDLEMSK (bit 4) can be enabled.

4.4.3 WAKE UP MODES

This section describes the conditions for awakening the part from both direct and automatic powerdown. Power conservation or extension of battery life is the main reason power management is required. This means that the 82078 must be kept in powerdown state as long as possible and should be powered up as late as possible without compromising software transparency.

To keep the part in powerdown mode as late as possible implies that the part should wake up as fast as possible. However, some amount of time is required for the part to exit powerdown state and prepare the internal microcontroller to accept commands. Application software is very sensitive to such a delay and in order to maintain software transparency, the recovery time of the wake up process must be carefully controlled by the system software.

4.4.3.1 Wake Up from DSR Powerdown

If the 82078 enters the powerdown through the DSR powerdown bit, it must be reset to exit. Any form of software or hardware reset will serve, although DSR is recommended. No other register access will awaken the part, including writing to the DOR's motor enable (FDME[0:3]) bits.

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened by a software reset, the auto powerdown command (including the minimum delay timer) will once again become effective as previously programmed. If the part is awakened via a hardware reset, the auto powerdown is disabled.

After reset, the part will go through a normal sequence. The drive status will be initialized. The FIFO mode will be set to default mode on a hardware reset or on a software reset if the LOCK command has not blocked it. Finally, after a delay, the polling interrupt will be issued.

4.4.3.2 Wake Up from Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the 82078 resumes operation as though it was never in powerdown. Besides activating the RESET pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part).
2. A read from the MSR register.
3. A read or write to the FIFO register.

Any of these actions will wake up the part. Once awake, 82078 will reinitiate the auto powerdown timer for 10 ms or 0.5 sec. (depending on the MIN DLY bit the auto powerdown command). When operating at 2 Mbps, the time is halved to 5 ms or 0.25 sec. depending on the MIN DLY bit. The part will powerdown again when all the auto powerdown conditions are satisfied.

4.5 Register Behavior

The register descriptions and their values in the powerdown state are listed in the Microprocessor Interface section. Table 4-1 reiterates the AT and PS/2 (including model 30) configuration registers available. It also shows the type of access permitted. In order to maintain software transparency, access to all the registers must be maintained. As Table 4-1 shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Table 4-1. 82078 Register Behavior

Address	Available Registers	Access	
	PC-AT	PS/2 (Model 30)	Permitted
Access to these registers DOES NOT wake up the part			
000	—	SRA	R
001	SRB (EREG EN = 1)	SRB	R/W
010	DOR*	DOR*	R/W
011	TDR	TDR	R/W
100	DSR*	DSR*	W
110	—	—	—
111	DIR	DIR	R
111	CCR	CCR	W
Access to these registers wake up the part			
100	MSR	MSR	R
101	FIFO	FIFO	R/W

*Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (either via DOR or DSR reset bits) will wake up the part.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in Section 2.1. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed. None of the extended registers effect the behavior of the powerdown mode.

4.6 Pin Behavior

The 82078 is specifically designed for the portable PC systems in which the power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of 82078 can be divided into two major categories; system interface and floppy disk drive interface. The floppy disk drive pins are disabled such that no power will be drawn through the 82078 as a result of any voltage applied to the pin within the 82078's power supply range. The floppy disk drive interface pins are configurable by the FDI TRI bit in the auto powerdown command. When the bit is set the output pins of the floppy disk drive retain their original state. All other pins are either disabled or unchanged as depicted in Table 4-4. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

4.6.1 SYSTEM INTERFACE PINS

Table 4-2 gives the state of the system interface pins in the powerdown state. Pins unaffected by powerdown are labeled ''UC''. Input pins are ''DISABLED'' to prevent them from causing currents internal to the 82078 when they have indeterminate input values.

Table 4-2. System Interface Pins

System Pins	State In Powerdown	System Pins	State In Powerdown
Input Pins		**Output Pins**	
CS#	UC	DRQ	UC (Low)
RD#	UC	INT	UC (Low)
WR#	UC	PD	HIGH
A[0:2]	UC	IDLE	High (Auto PD) Low (DSR PD)
DB[0:7]	UC	DB[0:7]	UC
RESET	UC		
IDENTn	UC		
DACK#	Disabled		
TC	Disabled		
X[1:2]	Programmable		

Two pins which can be used to indicate the status of the part are IDLE and PD. Table 4-3 shows how these pins reflect the 82078 status.

Table 4-3. 82078 Status Pins

PD	IDLE	MSR	Part Status
1	1	80H	Auto Powerdown
1	0	RQM = 1; MSR[6:0] = X	DSR Powerdown
0	1	80H	Idle
0	0	—	Busy

The IDLE pin indicates when the part is idle state and can be powered down. It is a combination of MSR equalling 80H, the head being unloaded and the INT pin being low. As shown in the table the IDLE pin will be low when the part is in DSR powerdown state. The PD pin is active whenever the part is in the powerdown state. It is active for either mode of powerdown. The PD pin can be used to turn off an external oscillator of other floppy disk drive interface hardware.

4.6.2 FDD INTERFACE PINS

The FDD interface ''input'' pins during powerdown are disabled or unchanged as shown in Table 4-4. The floppy disk drive ''output'' pins are programmable by the FDI TRI bit in the auto powerdown command. Setting of the FDI TRI bit in the auto powerdown command results in the interface retaining its normal state. When this bit is low (default state) all output pins in the FDD interface to the floppy disk drive itself are tri-stated. Pins used for local logic control or part programming are unaffected. Table 4-4 depicts the state of the floppy disk interface pins in the powerdown state (FDI TRI is low).

Table 4-4. 82078 FDD Interface Pins

FDD Pins	State In Powerdown	FDD Pins	State in Powerdown
Input Pins		**Output Pins (FDI TRI = 0)**	
RDDATA	Disabled	FDME[0:3]#	Tristated
WP	Disabled	FDS[0:3]#	Tristated
TRK0	Disabled	DIR#	Tristated
INDX#	Disabled	STEP#	Tristated
DRV2#	Disabled	WRDATA#	Tristated
DSKCHG#	Disabled	WE#	Tristated
		HDSEL#	Tristated
		DRVDEN[0:1]#	Tristated

5.0 CONTROLLER PHASES

For simplicity, command handling in the 82078 can be divided into three phases: Command, Execution and Result. Each phase is described in the following sections.

When there is no command in progress, the 82078 can be in idle, drive polling or powerdown state.

5.1 Command Phase

After a reset, the 82078 enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the 82078 before the command phase is complete (Please refer to Section 6.0 for the command descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the 82078, the host must examine the RQM and DIO bits of the Main Status Register. RQM, DIO must be equal to ''1'' and ''0'' respectively before command bytes may be written. RQM is set false by the 82078 after each write cycle until the received byte is processed. The 82078 asserts RQM again to request each parameter byte of the command, unless an illegal command condition is detected. After the last parameter byte is received, RQM remains ''0'', and the 82078 automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to retain compatibility with the 8272A, and to provide for the proper handling of the ''Invalid Command'' condition.

5.2 Execution Phase

All data transfers to or from the 82078 occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the SPECIFY command.

Each data byte is transferred by an INT or DRQ depending on the DMA mode. The CONFIGURE command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, (threshold) is defined as the number of bytes available to the 82078 when service is requested from the host, and ranges from 1 to 16. The parameter FIFOTHR which the user programs is one less, and ranges from 0 to 15.

A low threshold value (i.e., 2) results in longer periods of time between service requests, but requires faster servicing of the request, for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a ''fast'' system.

A high value of threshold (i.e., 12) is used with a ''sluggish'' system by affording a long latency period after a service request, but results in more frequent service requests.

5.2.1 NON-DMA MODE, TRANSFERS FROM THE FIFO TO THE HOST

The INT pin and RQM bits in the Main Status Register are activated when the FIFO contains 16 (or set threshold) bytes, or the last bytes of a full sector transfer have been placed in the FIFO. The INT pin can be used for interrupt driven systems and RQM can be used for polled sytems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO, then 82078 deactivates the INT pin and RQM bit.

5.2.2 NON-DMA MODE, TRANSFERS FROM THE HOST TO THE FIFO

The INT pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The INT pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has (threshold) bytes remaining in the FIFO. The INT pin will also be deactivated if TC and DACK# both go inactive. The 82078 enters the result phase after the last byte is taken by the 82078 from the FIFO (i.e., FIFO empty condition).

5.2.3 DMA MODE, TRANSFERS FROM THE FIFO TO THE HOST

The 82078 activates the DRQ pin when the FIFO contains 16 (or set threshold) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The 82078 will deactivate the DRQ pin when the FIFO becomes empty. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of RD#, on the last byte, if no edge is present on DACK#). Note that DACK# and TC must overlap for at least 50 ns for proper functionality.

5.2.4 DMA MODE, TRANSFERS FROM THE HOST TO THE FIFO

The 82078 activates the DRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the DACK# and WR# pins and placing data in the FIFO. DRQ remains active until the FIFO becomes full. DRQ is again set true when the FIFO has (threshold) bytes remaining in the FIFO. The 82078 will also deactivate the DRQ pin when TC becomes true (qualified by DACK# by overlapping by 50 ns), indicating that no more data is required. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of WR# of the last byte, if no edge is present on DACK#).

5.2.5 DATA TRANSFER TERMINATION

The 82078 supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multisector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the 82078 will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return ''abnormal termination'' result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the 82078, the internal sector count will be complete when 82078 reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the 82078 to read the last 16 bytes from the FIFO. The host must tolerate this delay.

5.3 Result Phase

The generation of INT determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the 82078 before the result phase is complete. (Refer to Section 6.0 on command descriptions.) These bytes of data must be read out for another command to start.

RQM and DIO must both equal ''1'' before the result bytes may be read from the FIFO. After all the result bytes have been read, the RQM and DIO bits switch to ''1'' and ''0'' respectively, and the CB bit is cleared. This indicates that the 82078 is ready to accept the next command.

6.0 COMMAND SET/DESCRIPTIONS

Commands can be written whenever the 82078 is in the command phase. Each command has a unique set of needed parameters and status results. The 82078 checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it was invalid, the next time the RQM bit in the MSR register is a ''1'' the DIO and CB bits will also be ''1'', indicating the FIFO must be read. A result byte of 80H will be read out of the FIFO, indicating an invalid command was issued. After reading the result byte from the FIFO the 82078 will return to the command phase. Table 6-1 is a summary of the Command set.

Table 6-1. 82078 Command Set

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
READ DATA										
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer between the FDD and System
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				Sector ID Information after Command Execution
	R					H				
	R					R				
	R					N				
READ DELETED DATA										
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer between the FDD and System
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				Sector ID Information after Command Execution
	R					H				
	R					R				
	R					N				
WRITE DATA										
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer between the FDD and System
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				Sector ID Information after Command Execution
	R					H				
	R					R				
	R					N				

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
WRITE DELETED DATA										
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer between the FDD and System
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information after Command Execution
	R					R				
	R					N				
READ TRACK										
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data Transfer between the FDD and System. FDC Reads All Sectors from Index Hole to EOT
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information after Command Execution
	R					R				
	R					N				
VERIFY										
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W					C				Sector ID Information prior to Command Execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL/SC				
Execution										Data Transfer between the FDD and System
Result	R					ST 0				Status Information after Command Execution
	R					ST 1				
	R					ST 2				
	R					C				
	R					H				Sector ID Information after Command Execution
	R					R				
	R					N				
VERSION										
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
FORMAT TRACK										
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				N					Bytes/Sector
	W				SC					Sectors/Cylinder
	W				GPL					Gap3
	W				D					Filler Byte
Execution For Each Sector Repeat:	W				C					Input Sector Parameters
	W				H					
	W				R					
	W				N					
										82078 Formats an Entire Cylinder
Result	R				ST 0					Status Information after Command Execution
	R				ST 1					
	R				ST 2					
	R				Undefined					
	R				Undefined					
	R				Undefined					
	R				Undefined					
SCAN EQUAL										
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information prior to Command Execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared between the FDD and Main-System
Result	R				ST 0					Status Information after Command Execution
	R				ST 1					
	R				ST 2					
	R				C					
	R				H					Sector ID Information after Command Execution
	R				R					
	R				N					

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
SCAN LOW OR EQUAL										
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information
	W				H					Prior to Command
	W				R					Execution
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared Between the FDD and Main-System
Result	R				ST 0					Status Information
	R				ST 1					After Command
	R				ST 2					Execution
	R				C					
	R				H					Sector ID Information
	R				R					After Command
	R				N					Execution
SCAN HIGH OR EQUAL										
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID Information
	W				H					Prior to Command
	W				R					Execution
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data Compared Between the FDD and Main-System
Result	R				ST 0					Status Information
	R				ST 1					After Command
	R				ST 2					Execution
	R				C					
	R				H					Sector ID Information
	R				R					After Command
	R				N					Execution

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	Enhanced Controller
Execution										Head Retracted to Track 0 Interrupt
SENSE INTERRUPT STATUS										
Command	W	0	0	0	1	0	0	0	0	Command Codes
Result	R				ST 0					Status Information at the End of each Seek Operation
	R				PVN					
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT					HUT			
	W	HLT							ND	
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R				ST 3					Status Information about FDD
DRIVE SPECIFICATION COMMAND										
Command	W	1	0	0	0	1	1	1	0	Command Codes
Phase	W	0	FD1	FD0	PTS	DRT1	DRT0	DT1	DT0	
	:	:	:	:	:	:	:	:	:	0–4 bytes issued
	W	DN	NRP	0	0	0	0	0	0	
Result	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 0
Phase	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 1
	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 2
	R	0	0	0	PTS	DRT1	DRT0	DT1	DT0	Drive 3
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				NCN					
Execution										Head is Positioned over Proper Cylinder on Diskette
CONFIGURE										
Command	W	CLK48	0	0	1	0	0	1	1	Command Code
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL		FIFOTHR			
	W				PRETRK					
RELATIVE SEEK										
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				RCN					

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
DUMPREG										
Command Execution	W	0	0	0	0	1	1	1	0	*Note Registers Placed in FIFO
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT					HUT			
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	D_3	D_2	D_1	D_0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL		FIFOTHR			
	R	PRETRK								
READ ID										
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The First Correct ID Information on the Cylinder is Stored in Data Register
Result	R	ST 0								Status Information after Command Execution
	R	ST 1								
	R	ST 2								
	R	C								
	R	H								Disk Status after the Command has Completed
	R	R								
	R	N								
PERPENDICULAR MODE										
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	D_3	D_2	D_1	D0	GAP	WGATE	
LOCK										
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	
PART ID										
Command	W	0	0	0	1	1	0	0	0	Command Code
Result	R	0	0	0		STEPPING			1	Part ID Number
POWERDOWN MODE										
Command	W	0	0	0	1	0	1	1	1	Command Code
	W	0	0	EREG EN	X	PS2 STAT	FDI TRI	MIN DLY	AUTO PD	
Result	R	0	0	EREG EN	X	PS2 STAT	FDI TRI	MIN DLY	AUTO PD	
OPTION										
Command	W	0	0	1	1	0	0	1	1	Command Code
	W	RSVD							ISO	

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
					SAVE					
Command Phase	W	0	0	1	0	1	1	1	0	Command Code
Result Phase	R	CLK 48	SEL 3V#	PD OSC	PC2	PC1	PC0	DRATE1	DRATE0	Save Info to Reprogram the FDC
	R	0	0	0	0	0	0	0	ISO	
	R				PCN-Drive 0					
	R				PCN-Drive 1					
	R				PCN-Drive 2					
	R				PCN-Drive 3					
	R		SRT					HUT		
	R				HLT				ND	
	R				SC/EOT					
	R	LOCK	0	D_3	D_2	D_1	D_0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL			FIFOTHR		
	R				PRETRK					
	R	0	0	EREG EN	RSVD	PS2 STAT	FDI TRI	MIN DLY	AUTO PD	
	R				DISK/STATUS					
	R				RSVD					
	R				RSVD					
					RESTORE					
Command Phase	W	0	1	0	0	1	1	1	0	Command Code
Result	W	CLK48	SEL 3V#	0	PC2	PC1	PC0	DRATE1	DRATE0	Restore Original Register Status
	W	0	0	0	0	0	0	0	ISO	
	W				PCN-Drive 0					
	W				PCN-Drive 1					
	W				PCN-Drive 2					
	W				PCN-Drive 3					
	W		SRT					HUT		
	W				HLT				ND	
	W				SC/EOT					
	W	LOCK	0	D_3	D_2	D_1	D_0	GAP	WGATE	
	W	0	EIS	EFIFO	POLL			FIFOTHR		
	W				PRETRK					
	W	0	0	EREG EN	RSVD	PS2 STAT	FDI TRI	MIN DLY	AUTO PD	
	W				DISK/STATUS					
	W				RSVD					
	W				RSVD					

Table 6-1. 82078 Command Set (Continued)

Phase	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
FORMAT AND WRITE										
Command	W	1	MFM	1	0	1	1	0	1	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				N					
	W				SC					
	W				GPL					
	W				D					
Execution	W				C					Input
Repeated	W				H					Sector
for each	W				R					Parameters
Sector	W				N					
	W	Data Transfer of N Bytes								82078 Formats and Writes Entire Track
Result	R				ST 0					
Phase	R				ST 1					
	R				ST 2					
	R				Undefined					
	R				Undefined					
	R				Undefined					
	R				Undefined					
INVALID										
Command	W				Invalid Codes					Invalid Command Codes (NoOp — 82078 goes into Standby State)
Result	R				ST 0					ST 0 = 80H

PARAMETER ABBREVIATIONS

Symbol	Description
AUTO PD	Auto powerdown control. If this bit is 0, then the automatic powerdown is disabled. If it is set to 1, then the automatic powerdown is enabled.
C	Cylinder address. The currently selected cylinder address, 0 to 255.
CLK48	CLK48 = 1 indicates an external 48 MHz oscillator is being used. CLK48 = 0 indicates a 24 MHz clock.
D0, D1, D2, D3	Drive Select 0-3. Designates which drives are Perpendicular drives, a ''1'' indicating Perpendicular drive.
D	Data pattern. The pattern to be written in each sector data field during formatting.
DN	Done. This bit indicates that this is the last byte of the drive specification command. The 82078 checks to see if this bit is high or low. If it is low, it expects more bytes. DN = 0 82078 expects more subsequent bytes. DN = 1 Terminates the command phase and jumps to the results phase. An additional benefit is that by setting this bit high, a direct check of the current drive specifications can be done.
DIR	Direction control. If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.
DS0, DS1	Disk Drive Select.

DS1	DS0	
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

DTL	Special sector size. By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
DRATE1, DRATE0	Data rate values from the DSR register.
DRT0, DRT1	Data rate table select. These two bits select between the different data rate tables. The default is the conventional table. These also provide mapping of the data rates selected in the DSR and CCR. The mapped values are provided for read back by the system software are as shown in the DIR (in PS/2 Mode only). Table 6-2 shows this.
DT0, DT1	Drive density select type. These bits select the outputs on DRVDEN0 and DRVDEN1 based on mode of operation that was selected via the IDENT1 and IDENT0 pins. More information is available in the Design Applications section.

Table 6-2. Data Rate Select Table

		Bits in DSR/CCR			Bits returned via DIR (Only available in PS/2)		
DRT0	**DRT1**	**DRATE0**	**DRATE1**	**Data Rate**	**DRATE0**	**DRATE1**	**Operation**
0	0	1	1	1 Mbps	1	1	Default
		0	0	500 Kbps	0	0	
		1	0	300 Kbps	1	0	
		0	1	250 Kbps	0	1	
0	1	1	1	1 Mbps	1	1	2 Mbps Tape Drive
		0	0	500 Kbps	0	0	
		1	0	2 Mbps	1	1	
		0	1	250 Kbps	0	1	
1	0		——-RSVD——				RSVD
1	1	1	1	1 Mbps	1	1	Perpendicular mode FDDs
		0	0	500 Kbps	0	0	
		1	0	RSVD			
		0	1	250 Kbps	0	1	

EC — Enable Count. When this bit is ''1'' the ''DTL'' parameter of the Verify Command becomes SC (Number of sectors per track).

EFIFO — Enable FIFO. When this bit is 0, the FIFO is enabled. A ''1'' puts the 82078 in the 8272A compatible mode where the FIFO is disabled.

EIS — Enable implied seek. When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A ''0'' disables the implied seek.

EOT — End of track. The final sector number of the current track.

EREG EN — Enhanced Register Enable.

EREG EN = 1 In PS/2 mode the TDR register is extended. In AT/EISA mode, the TDR register is extended and SRB is made visible to the user.

EREG EN = 0 Standard AT/EISA and PS/2 registers are used.

FDI TRI — Floppy Drive Interface Tri-state: If this bit is 0, then the output pins of the floppy disk drive interface are tri-stated. This is also the default state. If it is set to 1, then the floppy disk drive interface remains unchanged.

FD0, FD1 — Floppy drive select. These two bits select which physical drive is being specified. The FDn corresponds to FDSn and FDMEn on the floppy drive interface. The drive is selected independent of the BOOTSELn bits. Please refer to Section 2.1.1 which explains the distinction between physical drives and their virtual mapping as defined by the BOOTSEL1 and BOOTSEL0 bits.

FD0	**FD1**	**Drive Slot**
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

GAP — Alters Gap 2 length when using Perpendicular Mode.

GPL — Gap length. The gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).

HDS — Head address. Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.

HLT — Head load time. The time interval that 82078 waits after loading the head and before initiating a read or write operation. Refer to the SPECIFY command for actual delays.

HUT — Head unload time. The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the SPECIFY command for actual delays.

ISO — ISO Format: If this bit is set high the ISO format is used for all data transfer commands. When this bit is set low the normal IBM system 34 and perpendicular is used. The default is ISO = 0.

Lock — Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be reset to their default values by a ''Software Reset'' (Reset made by setting the proper bit in the DSR or DOR registers).

MFM — MFM mode. A one selects the double density (MFM) mode. A zero is reserved.

MIN DLY — Minimum power up time control. This bit is active only if AUTO PD bit is enabled. Setting this bit to a 0, assigns a 10 ms minimum power up time and setting this bit to a 1, assigns a 0.5 sec. minimum power up time (unless 2 Mbps, then 5 ms to 0.25 sec.).

MT — Multi-track selector. When set, this flag selects the multi-track operating mode. In this mode, the 82078 treats a complete cylinder, under head 0 and 1, as a single track. The 82078 operates as if this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the 82078 finishes operating on the last sector under head 0.

N — Sector size code. This specifies the number of bytes in a sector. If this parameter is ''00'', then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the ''N'th'' power) times 128. All values up to ''07'' hex are allowable. ''07''h would equal a sector size of 16k. It is the users responsibility to not select combinations that are not possible with the drive.

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
—	—
07	16 Kbytes

NCN — New cylinder number. The desired cylinder number.

ND — Non-DMA mode flag. When set to 1, indicates that the 82078 is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the 82078 operates in DMA mode, interfacing to a DMA controller by means of the DRQ and DACK# signals.

NRP — No Results phase. When this bit is set high the result phase is skipped. When this bit is low the result phase will be generated.

OW — The bits denoted D0, D1, D2, and D3 of the PERPENDICULAR MODE command can only be overwritten when the OW bit is set to ''1''.

PCN — Present cylinder number. The current position of the head at the completion of SENSE INTERRUPT STATUS command.

PC2, PC1, PC0 — Precompensation values from the DSR register.

PDOSC — When this bit is set, the internal oscillator is turned off.

This may be done if using the external 48 MHz oscillator.

PS/2 STAT — PS/2 status. This bit is functional only in the PS/2 mode. In all other modes this bit will not have any effect. When set high this bit enables two bits (bits 5 and 6) in the DIR register to reflect the values of PD and IDLE respectively except when IDLEMSK (bit 4) is set. Default value is 0.

PTS — Precompensation table select. This bit selects whether to enable the precompensation value programmed in the DSR or not. In the default state, the value programmed in DSR will be used.

PTS = 0 DSR programmed precompensation delays.

PTS = 1 No precompensation delay is selected for the corresponding drive.

POLL — Polling disable. When set, the internal polling routine is disabled. When clear, polling is enabled.

PRETRK — Precompensation start track number. Programmable from track 00 to FFH.

R — Sector address. The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.

RCN — Relative cylinder number. Relative cylinder offset from present cylinder as used by the RELATIVE SEEK command.

SC — Number of sectors. The number of sectors to be initialized by the FORMAT command. The number of sectors to be verified during a Verify Command, when EC is set.

SEL3V# — SEL3V# = 1 indicates that the part is operating at 5.0V.

SEL3V# = 0 indicates that the part is operating at 3.3V.

SK — Skip flag. When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of READ DATA. If READ DELETED is executed, only sectors with a deleted address mark will be accessed. When set to ''0'', the sector is read or written the same as the read and write commands.

SRT — Step rate interval. The time interval between step pulses issued by the 82078. Programmable from 0.5 ms to 8 ms, in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.

ST0–3 — Status registers 0–3. Registers within the 82078 that store status information after a command has been executed. This status information is available to the host during the result phase after command execution.

STEPPING — These bits identify the stepping of the 82078.

WGATE — Write gate alters timing of WE, to allow for pre-erase loads in perpendicular drives.

6.1 Data Transfer Commands

All of the READ DATA, WRITE DATA and VERIFY type commands use the same parameter bytes and return the same results information. The only difference being the coding of bits 0–4 in the first byte.

An implied seek will be executed if the feature was enabled by the CONFIGURE command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a READ/WRITE DATA command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

6.1.1 READ DATA

A set of nine (9) bytes is required to place the 82078 into the Read Data Mode. After the READ DATA command has been issued, the 82078 loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the SPECIFY command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the 82078 reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one, and the data from the next logical sector is read and output via the FIFO. This continuous read function is called ''Multi-Sector Read Operation''. Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the 82078 stops sending data, but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector terminate the READ DATA Command.

N determines the number of bytes per sector (see Table 6-3). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the 82078 transfers the specified number of bytes to the host. For reads, it continues to read the entire 128 byte sector and checks for CRC errors. For writes it completes the 128 byte sector by filling in zeroes. If N is not set to 00 Hex, DTL should be set to FF Hex, and has no impact on the number of bytes transferred.

Table 6-3. Sector Sizes

N	Sector Size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
—	—
07	16 Kbytes

The amount of data which can be handled with a single command to the 82078 depends upon MT (multi-track) and N (Number of bytes/sector).

Table 6-4. Effects of MT and N Bits

MT	N	Max. Transfer Capacity	Final Sector Read from Disk
0	1	256 × 26 = 656	26 at side 0 or 1
1	1	256 × 52 = 13312	26 at side 1
0	2	512 × 15 = 7680	15 at side 0 or 1
1	2	512 × 30 = 15360	15 at side 1
0	3	1024 × 8 = 8192	8 at side 0 or 1
1	3	1024 × 16 = 16384	16 at side 1

The Multi-Track function (MT) allows the 82078 to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at the last sector of the same track at Side 1.

If the host terminates a read or write operation in the 82078, then the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 6-7. The termination must be normal.

At the completion of the READ DATA Command, the head is not unloaded until after the Head Unload Time Interval (specified in the SPECIFY command) has elapsed. If the host issues another command before the head unloads then the head settling time may be saved between subsequent reads.

If the 82078 detects a pulse on the INDX# pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the 82078 sets the IC code in Status Register 0 to ''01'' (Abnormal termination), and sets the ND bit in Status Register 1 to ''1'' indicating a sector not found, and terminates the READ DATA Command.

After reading the ID and Data Fields in each sector, the 82078 checks the CRC bytes. If a CRC error occurs in the ID or data field, the 82078 sets the IC code in Status Register 0 to ''01'' (Abnormal termination), sets the DE bit flag in Status Register 1 to ''1'', sets the DD bit in Status Register 2 to ''1'' if CRC is incorrect in the ID field, and terminates the READ DATA Command.

Table 6-5 describes the affect of the SK bit on the READ DATA command execution and results.

Table 6-5. Skip Bit vs READ DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	No	Normal Termination.
0	Deleted Data	Yes	Yes	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	Yes	No	Normal Termination.
1	Deleted Data	No	Yes	Normal Termination Sector Not Read (''Skipped'').

Except where noted in Table 6-5, the C or R value of the sector address is automatically incremented (see Table 6-7).

6.1.2 READ DELETED DATA

This command is the same as the READ DATA command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 6-6 describes the affect of the SK bit on the READ DELETED DATA command execution and results.

Table 6-6. Skip Bit vs READ DELETED DATA Command

SK Bit Value	Data Address Mark Type Encountered	Results		
		Sector Read?	CM Bit of ST2 Set?	Description of Results
0	Normal Data	Yes	Yes	Normal Termination.
0	Deleted Data	Yes	No	Address Not Incremented. Next Sector Not Searched For.
1	Normal Data	No	Yes	Normal Termination Sector Not Read (''Skipped'').
1	Deleted Data	Yes	No	Normal Termination.

Except where noted in Table 6-6 above, the C or R value of the sector address is automatically incremented (see Table 6-7).

6.1.3 READ TRACK

This command is similar to the READ DATA command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the INDX# pin, the 82078 starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the 82078 finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The 82078 compares the ID information read from each sector with the specified value in the command, and sets the ND flag of Status Register 1 to a ''1'' if there is no comparison.

Multi-track or skip operations are not allowed with this command. The MT and SK bits (Bits D7 and D5 of the first command byte respectively) should always be set to ''0''.

Table 6-7. Result Phase Table

MT	Head	Final Sector Transferred to Host	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	NC	01	NC
1	0	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R+1	NC
		Equal to EOT	C+1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

This command terminates when the EOT specified number of sectors have been read. If the 82078 does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the INDX# pin, then it sets the IC code in Status Register 0 to ''01'' (Abnormal termination), sets the MA bit in Status Register 1 to ''1'', and terminates the command.

6.1.4 WRITE DATA

After the WRITE DATA command has been issued, the 82078 loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the SPECIFY command), and begins reading ID Fields. When the sector address read from the diskette matches the sector address specified in the command, the 82078 reads the data from the host via the FIFO, and writes it to the sector's data field.

After writing data into the current sector, the 82078 computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in ''R'' is incremented by one, and the 82078 continues writing to the next data field. The 82078 continues this ''Multi-Sector Write Operation''. Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeroes.

The 82078 reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID Fields, it sets the IC code in Status Register 0 to ''01'' (Abnormal termination), sets the DE bit of Status Register 1 to ''1'', and terminates the WRITE DATA command.

The WRITE DATA command operates in much the same manner as the READ DATA command. The following items are the same. Please refer to the READ DATA Command for details:

- Transfer Capacity
- (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command.
- Definition of DTL when N = 0 and when N does not = 0.

6.1.5 WRITE DELETED DATA

This command is almost the same as the WRITE DATA command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

6.1.6 VERIFY

The VERIFY command is used to verify the data stored on a disk. This command acts exactly like a READ DATA command except that no data is transferred to the host. Data is read from the disk, CRC computed and checked against the previously stored value.

Because no data is transferred to the host, TC (pin 25) cannot be used to terminate this command. By setting the EC bit to ''1'' an implicit TC will be issued to the 82078. This implicit TC will occur when the SC value has decrement to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to ''0'' and the EOT value equal to the final sector to be checked. If EC is set to ''0'' DTL/SC should be programmed to 0FFH. Refer to Table 6-6 and Table 6-7 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to ''1''.

Table 6-8. Verify Command Result Phase Table

MT	EC	SC/EOT Value	Termination Result
0	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

NOTE:
If MT is set to ''1'' and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

6.1.7 FORMAT TRACK

The FORMAT command allows an entire track to be formatted. After a pulse from the INDX# pin is detected, the 82078 starts writing data on the disk including Gaps, Address Marks, ID Fields and Data Fields, per the IBM System 34 (MFM). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID Field for each sector is supplied by the host; that is, four data bytes per sector are needed by the 82078 for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the 82078 for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the 82078 encounters a pulse on the INDX# pin again and it terminates the command.

Table 6-9 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

Table 6-9. Typical PC-AT Values for Formatting

Drive Form	MEDIA	Sector Size	N	SC	GPL1	GPL2
5.25″	1.2M	512	02	0F	2A	50
	360K	512	02	09	2A	50
3.5″	2.88M	512	02	24	38	53
	1.44M	512	02	18	1B	54
	720K	512	02	09	1B	54

NOTE:
All values except Sector Size are in Hex.

Gap3 is programmable during reads, writes, and formats.

GPL1 = suggested Gap3 values in read and write commands to avoid splice point between data field and ID field of contiguous sections.

GPL2 = suggested Gap3 value in FORMAT TRACK command.

6.1.7.1 Format Fields

Table 6-10. System 34 Format Double Density

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM		DATA	CRC	GAP 3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE						22x 4E	12x 00	3x A1	FB F8				

Table 6-11. ISO Format

GAP 1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM		DATA	CRC	GAP 3	GAP 4b
32x 4E	12x 00	3x A1	FE						22x 4E	12x 00	3x A1	FB F8				

Table 6-12. Perpendicular Format

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP 2	SYNC	DATA AM		DATA	CRC	GAP 3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE						41x 4E	12x 00	3x A1	FB F8				

6.2 Control Commands

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete; READ ID, RECALIBRATE and SEEK. The other control commands do not generate an interrupt.

6.2.1 READ ID

The READ ID command is used to find the present position of the recording heads. The 82078 stores the values from the first ID Field it is able to read into its registers. If the 82078 does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the INDX# pin, it then sets the IC code in Status Register 0 to ''01'' (Abnormal termination), sets the MA bit in Status Register 1 to ''1'', and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the SENSE INTERRUPT STATUS command. Otherwise, valuable interrupt status information will be lost.

6.2.2 RECALIBRATE

This command causes the read/write head within the 82078 to retract to the track 0 position. The 82078 clears the contents of the PCN counter, and checks the status of the TRK0 pin from the FDD. As long as the TRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the TRK0 pin goes high, the SE bit in Status Register 0 is set to ''1'', and the command is terminated. If the TRK0 pin is still low after 79 step pulses have been issued, the 82078 sets the SE and the EC bits of Status Register 0 to ''1'', and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one RECALIBRATE command to return the head back to physical Track 0.

The RECALIBRATE command does not have a result phase. SENSE INTERRUPT STATUS command must be issued after the RECALIBRATE command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the 82078 is in the BUSY state, but during the execution phase it is in a NON BUSY state. At this time another RECALIBRATE command may be issued, and in this manner, parallel RECALIBRATE operations may be done on up to 4 drives at once.

Upon power up, the software must issue a RECALIBRATE command to properly initialize all drives and the controller.

6.2.3 DRIVE SPECIFICATION COMMAND

The 82078 uses two pins, DRVDEN0 and DRVDEN1 to select the density for modern drives. These signals inform the drive of the type of diskette in the drive. The Drive Specification command specifies the polarity of the DRVDEN0 and DRVDEN1 pins. It also enables or disables DSR programmed precompensation.

This command removes the need for a hardware workaround to accommodate differing specifications among drives. By programming this command during BIOS's POST routine, the floppy disk controller will internally configure the correct values for DRVDEN0 and DRVDEN1 with corresponding precompensation value and data rate table enabled for the particular type of drive.

This command is protected from software resets. After executing the DRIVE SPEC command, subsequent software resets will not clear the programmed parameters. Only another DRIVE SPEC command or H/W reset can reset it to default values. The 6 LSBs of the last byte of this command are reserved for future use.

The DRATE0 and DRATE1 are values as programmed in the DSR register. The DENSEL is high for high data rates (1 Mbps and 500 Kbps) and low for low data rates (300 Kbps and 250 Kbps).

Table 6-13 describes the drives that are supported with the DT0, DT1 bits of the Drive Specification command:

Table 6-13. Drive Support via the Drive Specification Command

DRVDENn Polarities for AT/EISA Mode (IDENT0, IDENT1 = 11)

DT0	DT1	Data Rate	DRVDEN0	DRVDEN1
0*	0*	1 Mbps 500 Kbps 300 Kbps 250 Kbps	1 1 0 0	1 0 1 0
0	1	1 Mbps 500 Kbps 300 Kbps 250 Kbps	1 0 0 1	1 0 1 0
1	0	1 Mbps 500 Kbps 300 Kbps 250 Kbps	0 0 1 1	1 0 1 0
1	1	1 Mbps 500 Kbps 300 Kbps 250 Kbps	1 0 1 0	1 0 0 1

(*) Denotes the default setting

DRVDEN Polarities for PS/2, Model 30 Mode (IDENT0, IDENT1 = 0X)

DT0	DT1	Data Rate	DRVDEN0	DRVDEN1
0*	0*	1 Mbps 500 Kbps 300 Kbps 250 Kbps	1 0 1 0	1 0 0 1
0	1	1 Mbps 500 Kbps 300 Kbps 250 Kbps	1 1 0 0	1 0 1 0
1	0	1 Mbps 500 Kbps 300 Kbps 250 Kbps	0 0 1 1	1 0 1 0
1	1	1 Mbps 500 Kbps 300 Kbps 250 Kbps	1 0 0 1	1 0 1 0

(*) Denotes the default setting

6.2.4 SEEK

The read/write head within the drive is moved from track to track under the control of the SEEK Command. The 82078 compares the PCN which is the current head position with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in), and issues step pulses.

PCN > NCN: Direction signal to drive set to "0" (step out), and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN, then the SE bit in Status Register 0 is set to "1", and the command is terminated.

During the command phase of the seek or recalibrate operation, the 82078 is in the BUSY state, but during the execution phase it is in the NON BUSY state.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1. SEEK command; Step to the proper track
2. SENSE INTERRUPT STATUS command; Terminate the Seek command
3. READ ID. Verify head is on proper track
4. Issue READ/WRITE command.

The SEEK command does not have a result phase. Therefore, it is highly recommended that the SENSE INTERRUPT STATUS Command be issued after the SEEK command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return a "0". When exiting DSR POWERDOWN mode, the 82078 clears the PCN value and the status information to zero. Prior to issuing the DSR POWERDOWN command, it is highly recommended that the user service all pending interrupts through the SENSE INTERRUPT STATUS command.

6.2.5 SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6-9 shows the status of bits SH and SN under various conditions of SCAN.

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector has been encountered.

When either the STP (contiguous sectors STP = 01, or alternate sectors STP = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 13 μs. If an Overrun occurs the FDC terminates the command.

Table 6-13. Scan Status Codes

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \not> D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} \not< D_{Processor}$

6.2.6 SENSE INTERRUPT STATUS

An interrupt signal on INT pin is generated by the 82078 for one of the following reasons:

1. Upon entering the Result Phase of:
   a. READ DATA Command
   b. READ TRACK Command
   c. READ ID Command
   d. READ DELETED DATA Command
   e. WRITE DATA Command
   f. FORMAT TRACK Command
   g. WRITE DELETED DATA Command
   h. VERIFY Command
2. End of SEEK, RELATIVE SEEK or RECALIBRATE Command
3. 82078 requires a data transfer during the execution phase in the non-DMA Mode

The SENSE INTERRUPT STATUS command resets the interrupt signal and via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt. If a SENSE INTERRUPT STATUS command is issued when no active interrupt condition is present, the status register ST0 will return a value of 80H (invalid command).

Table 6-14. Interrupt Identification

SE	IC	Interrupt Due To
0	11	Polling
1	00	Normal Termination of SEEK or RECALIBRATE command
1	01	Abnormal Termination of SEEK or RECALIBRATE command

The SEEK, RELATIVE SEEK and the RECALIBRATE commands have no result phase. SENSE INTERRUPT STATUS command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a SENSE INTERRUPT STATUS is not issued, the drive will continue to be BUSY and may effect the operation of the next command.

6.2.7 SENSE DRIVE STATUS

SENSE DRIVE STATUS obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. STATUS REGISTER 3 contains the drive status information.

6.2.8 SPECIFY

The SPECIFY command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between the command phase to the execution phase of a read/write data command. The Head Unload Time (HUT) timer starts at the end of the execution phase to the beginning of the result phase of a read/write command. The values change with the data rate speed selection and are documented in Table 6-15.

Table 6-15. Drive Control Delays (ms)

	HUT				SRT			
	1M	500K	300K	250K	1M	500K	300K	250K
0	128	256	426	512	8.0	16	26.7	32
1	8	16	26.7	32	7.5	15	25	30
—	—	—	—	—	—	—	—	—
A	80	160	267	320	3.0	6.0	10.2	12
B	88	176	294	352	2.5	5.0	8.35	10
C	96	192	320	384	2.0	4.0	6.68	8
D	104	208	346	416	1.5	3.0	5.01	6
E	112	224	373	448	1.0	2.0	3.33	4
F	120	240	400	480	0.5	1.0	1.67	2

HLT				
	1M	500K	300K	250K
00	128	256	426	512
01	1	2	3.3	4
02	2	4	6.7	8
—	—	—	—	—
7E	126	252	420	504
7F	127	254	423	508

The choice of DMA or NON-DMA operations is made by the ND bit. When this bit is ''1'', the NON-DMA mode is selected, and when ND is ''0'', the DMA mode is selected. In DMA mode, data transfers are signalled by the DRQ pin. Non-DMA mode uses the RQM bit and the INT pin to signal data transfers.

6.2.9 CONFIGURE

Issue the configure command to enable features like the programmable FIFO and set the beginning track for pre-compensation. A CONFIGURE command need not be issued if the default values of the 82078 meet the system requirements. The CLK48 bit allows the 82078 to connect to a 48 MHz oscillator, this can reduce board space if there is a 48 MHz signal already available on the system.

CONFIGURE DEFAULT VALUES:

EIS — No Implied Seeks
EFIFO — FIFO Disabled
POLL — Polling Enabled
FIFOTHR — FIFO Threshold Set to 1 Byte
PRETRK — Pre-Compensation Set to Track 0

EIS—Enable implied seek. When set to ''1'', the 82078 will perform a SEEK operation before executing a read or write command. Defaults to no implied seek.

EFIFO—A ''1'' puts the FIFO into the 8272A compatible mode where the FIFO is disabled. This means data transfers are asked for on a byte by byte basis. Defaults to ''1'', FIFO disabled. The threshold defaults to one.

POLL—Disable polling of the drives. Defaults to ''0'', polling enabled. When enabled, a single interrupt is generated after a RESET. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR—The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 byte to 16 bytes. Defaults to one byte. A ''00'' selects one byte, ''0F'' selects 16 bytes.

PRETRK—Pre-compensation start track number. Programmable from track 0 to 255. Defaults to track 0. A ''00'' selects track 0, ''FF'' selects 255.

CLK48—Default is ''0'', external clock is assumed to be 24 MHz. If a 48 MHz external oscillator is used the bit must be set high. Note that the 82078 does not support a 48 MHz crystal, only an external oscillator. Note, this must be enabled first during the initialization routine of the POST if a 48 MHz oscillator is used.

6.2.10 VERSION

The VERSION command checks to see if the controller is an enhanced type (82077, 82077AA, 82077SL) or the older type (8272A/765A). A value of 90H is returned as the result byte, defining an enhanced FDD controller is in use. No interrupts are generated.

6.2.11 RELATIVE SEEK

The command is coded the same as for SEEK, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control.

DIR	Action
0	Step Head Out
1	Step Head In

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The RELATIVE SEEK command differs from the SEEK command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The SEEK command is good for drives that support a maximum of 256 tracks. RELATIVE SEEKs cannot be overlapped with other RELATIVE SEEKs. Only one RELATIVE SEEK can be active at a time. Bit 4 of Status Register 0 (EC) will be set if RELATIVE SEEK attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks and that the host needs to read track 300 and the head is on any track (0–255). If a SEEK

command was issued, the head would stop at track 255. If a RELATIVE SEEK command was issued, the 82078 would move the head the specified number of tracks, regardless of the internal cylinder position register (but would increment the register). If the head had been on track 40 (D), the maximum track that the 82078 could position the head on using RELATIVE SEEK, would be 296 (D), the initial track, + 256 (D). The maximum count that the head can be moved with a single RELATIVE SEEK command is 256 (D).

The internal register, PCN, would overflow as the cylinder number crossed track 255 and would contain 40 (D). The resulting PCN value is thus (NCN + PCN) mod 256. Functionally, the 82078 starts counting from 0 again as the track number goes above 255(D). It is the users responsibility to compensate 82078 functions (precompensation track number) when accessing tracks greater than 255. The 82078 does not keep track that it is working in an ''extended track area'' (greater than 255). Any command issued would use the current PCN value except for the RECALIBRATE command which only looks for the TRACK0 signal. RECALIBRATE would return an error if the head was farther than 79 due to its limitation of issuing a maximum 80 step pulses. The user simply needs to issue a second RECALIBRATE command. The SEEK command and implied seeks will function correctly within the 44 (D) track (299–255) area of the ''extended track area''. It is the users responsibility not to issue a new track position that would exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0–255) of tracks, a RELATIVE SEEK would be issued to cross the track 255 boundary.

A RELATIVE SEEK can be used instead of the normal SEEK but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a READ ID command to ensure that the head is physically on the track that software assumes it to be. Different 82078 commands will return different cylinder results which may be difficult to keep track of with software without the READ ID command.

6.2.12 DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. The command returns pertinent information regarding the internal status of the 82078. This can be used to verify the values initialized in the 82078.

6.2.13 PERPENDICULAR MODE COMMAND

6.2.13.1 About Perpendicular Recording Mode

An added capability of the 82078 is the ability to interface directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method by orienting the magnetic bits vertically. This scheme packs in more data bits for the same area.

6.2.13.2 The Perpendicular Mode Command

The PERPENDICULAR MODE Command allows the system designers to designate specific drives as

Table 6-16. Effects of WGATE and GAP Bits

GAP	WGATE	MODE	VCO Low Time after Index Pulse	Length of Gap2 Format Field	Portion of Gap2 Written by Write Data Operation	Gap2 VCO Low Time for Read Operations
0	0	Conventional Mode	33 Bytes	22 Bytes	0 Bytes	24 Bytes
0	1	Perpendicular Mode (500 Kbps Data Rate)	33 Bytes	22 Bytes	19 Bytes	24 Bytes
1	0	Reserved (Conventional)	33 Bytes	22 Bytes	0 Bytes	24 Bytes
1	1	Perpendicular Mode (1 Mbps Data Rate)	18 Bytes	41 Bytes	38 Bytes	43 Bytes

NOTE:
When either GAP or WGATE bit is set, the current value of precompensation in the DSR is used.

Perpendicular recording drives. Data transfers between Conventional and Perpendicular drives are allowed without having to issue PERPENDICULAR MODE commands between the accesses of the two different drives, nor having to change write pre-compensation values.

With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 6-16 describes the effects of the WGATE and GAP bits for the PERPENDICULAR MODE command.

When both GAP and WGATE equal ''0'' the PERPENDICULAR MODE command will have the following effect on the 82078: 1) If any of the new bits D0, D1, D2, and D3 are programmed to ''1'' the corresponding drive will automatically be programmed for Perpendicular mode (i.e.: GAP2 being written during a write operation, the programmed Data Rate will determine the length of GAP2), and data will be written with 0 ns write pre-compensation. 2) any of the new bits (D0–D3) that are programmed for ''0'' the designated drive will be programmed for Conventional Mode and data will be written with the currently programmed write pre-compensation value. 3) Bits D0, D1, D2, and D3 can only be over written when the OW bit is written as a ''1''. The status of these bits can be determined by interpreting the eighth result byte of the DUMPREG Command. (Note: if either the GAP or WGATE bit is a ''1'', then bits D0–D3 are ignored.)

''Software'' and ''Hardware'' RESET will have the following effects on the enhanced PERPENDICULAR MODE command:

1. ''Software'' RESETs (Reset via DOR or DSR registers) will only clear GAP and WGATE bits to ''0'', D3, D2, D1, and D0 will retain their previously programmed values.
2. ''Hardware'' RESETs (Reset via pin 32) will clear all bits (GAP, WGATE, D0, D1, D2, and D3) to ''0'' (All Drives Conventional Mode).

6.2.14 POWERDOWN MODE COMMAND

The POWERDOWN MODE command allows the automatic power management and enables the enhanced registers (EREG EN) of the 82078. The use of the command can extend the battery life in portable PC applications. To enable auto powerdown the command may be issued during the BIOS power on self test (POST).

This command includes the ability to configure the 82078 into the enhanced AT/EISA and PS/2 mode. In the enhanced PS/2 and Model 30 modes, this makes the PD and IDLE pin status visible in the DIR register. In the enhanced AT/EISA modes, this command extends the SRB and TDR register. These extended registers accommodate bits that give more information about floppy drive interface, allow for boot drive selection, and identify the values of the PD and IDLE status.

As soon as the command is enabled, a 10 ms or a 0.5 sec. (5 ms or 0.25 with 2Mbps tape mode) minimum powerup timer is initiated depending on whether the MIN DLY bit is set to 0 or 1. This timer is one of the required conditions that has to be satisfied before the part will enter auto powerdown. Any software reset will reinitialize the timer. The timer countdown is also extended by up to 10 ms if the data rate is changed during the timer's countdown. Without this timer 82078 would have been put to sleep immediately after 82078 is idle. The minimum delay gives software a chance to interact with 82078 without incurring an additional overhead due to recovery time.

The command also allows the output pins of floppy disk drive interface to be tri-stated or left unaltered during auto powerdown. This is done by the FDI TRI bit. In the default condition (FDI TRI = 0) the output pins of the floppy disk drive are tri-stated. Setting this bit leaves the interface unchanged from the normal state.

The results phase returns the values programmed for MIN DLY, FDI TRI and AUTO PD. The auto powerdown mode is disabled by a hardware reset. Software results have no effect on the POWERDOWN MODE command parameters.

6.2.15 PART ID COMMAND

This command can be used to identify the floppy disk controller as an enhanced controller. The first stepping of both versions of the 64 pin 82078 will yield 0x01 in the result phase of this command. Any future enhancements on these parts will be denoted by the 5 LSBs (0x01 to 0x1F).

6.2.16 OPTION COMMAND

The standard IBM format includes an index address field consisting of 80 bytes of GAP 4a, 12 bytes of the sync field, four bytes identifying the IAM and 50 bytes of GAP 1. Under the ISO format most of this preamble is not used. The ISO format allows only 32 bytes of GAP 1 after the index mark. The ISO bit in this command allows the 82078 to configure the data transfer commands to recognize this format. The MSBs in this command are reserved for any other enhancements made available to the user in the future.

6.2.17 SAVE COMMAND

The first byte corresponds to the values programmed in the DSR with the exception of CLK48. The DRATE1, DRATE0 used here are unmapped. The second byte is used for configuring the bits from the OPTION command. All future enhancements to the OPTION command will be reflected in this byte as well. The next nine result bytes are explained in the Parameter Abbreviations section after the command summary. The 13th byte is the value associated with the auto powerdown command. The disk status is used internally by 82078. There are two reserved bytes at the end of this command for future use.

This command is similar to the DUMPREG command but it additionally allows the user to read back the precompensation values as well as the programmed data rate. It also allows the user to read the values programmed in the auto powerdown command. The precompensation values will be returned as programmed in the DSR register. This command is used in conjunction with the Restore command should prove very useful for SMM power management. This command reserves the last two bytes for future enhancements.

6.2.18 RESTORE COMMAND

Using Restore with the Save command, allows the SMM power management to restore the 82078 to its original state after a system powerdown. It also serves as a succinct way to provide most of the initialization requirements normally handled by the system. The sequence of initializing the 82078 after a reset occurred and assuming a Save command was issued follows:

- Issue the Drive Spec command (if the design utilizes this command)
- Issue the Restore command (pass the 16 bytes retrieved previously during SAVE)

The Restore command will program the data rate and precompensation value via the DSR. It then restores the values normally programmed through the Configure, Specify, and Perpendicular commands. It also enables the previously selected values for the AUTO Powerdown command. The PCN values are set restored to their previous values and the user is responsible for issuing the seek and recalibrate commands to restore the head to the proper location. There are some drives that do not recalibrate in which case the Restore command will restore the previous state completely. The PDOSC bit is retrievable using the Save command, however, the system designer must set it correctly. The software must allow at least 20 μs to execute the Restore command. When using the BOOTSEL bits in the TDR, the user must restore or reinitialize these bits to their proper values.

6.2.19 FORMAT AND WRITE COMMAND

The format and write command is capable of simultaneously formatting and writing data to the diskette. It is essentially the same as the normal format command. With the exception that included in the execution for each sector is not only the C, H, R, and N but also the data transfer of N bytes. The D value is ignored. This command formats the entire track. High speed floppy diskette duplication can be done fast and efficiently with this command. The user can format the diskette and put data on it in a single pass. This is very useful for software duplication applications by reducing the time required to format and copy diskettes.

6.2.20 LOCK

The LOCK command is included to protect a system with long DMA latencies against older application software packages that can disable the 82078's FIFO.

NOTE:
This command should only be used by the system's FDC routines, and ISVs (Independent Software Vendors) should refrain from using it. If an ISV's application calls for having the 82078 FIFO disabled a CONFIGURE Command should be used to toggle the EFIFO (Enable FIFO) bit. ISV can determine the value of the LOCK bit by interpreting the eighth result byte of an DUMPREG Command.

The LOCK command defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to a ''1'' all subsequent ''software'' RESETs by the DOR and DSR registers will not change the previously set parameter values in the CONFIGURE command. When the LOCK bit is set to a ''0'' 'software'' RESETs by the DOR or DSR registers will return these parameters to their default values. All ''hardware'' Resets will set the LOCK bit to a ''0'' value, and will return EFIFO, FIFOTHR, and PRETRK to their default values. A Status byte is returned immediately after issuing the command byte. This Status byte reflects the value of the Lock bit set by the command byte.

NOTE:
No interrupts are generated at the end of this command.

7.0 STATUS REGISTER ENCODING

The contents of these registers are available only through a command sequence.

7.1 Status Register 0

Bit No.	Symbol	Name	Description
7, 6	IC	Interrupt Code	00—Normal termination of command. The specified command was properly executed and completed without error. 01—Abnormal termination of command. Command execution was started, but was not successfully completed. 10—Invalid command. The requested command could not be executed. 11—Abnormal termination caused by Polling.
5	SE	Seek End	The 82078 completed a SEEK or RECALIBRATE command, or a READ or WRITE with implied seek command.
4	EC	Equipment Check	The TRK0 pin failed to become a ‘‘1’’ after: 1. 80 step pulses in the RECALIBRATE command. 2. The RELATIVE SEEK command causes the 82078 to step outward beyond Track 0.
3	—	—	Unused. This bit is always ‘‘0’’.
2	H	Head Address	The current head address.
1, 0	DS1, 0	Drive Select	The current selected drive.

7.2 Status Register 1

Bit No.	Symbol	Name	Description
7	EN	End of Cylinder	The 82078 tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data Command.
6	—	—	Unused. This bit is always ‘‘0’’.
5	DE	Data Error	The 82078 detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the 82078 does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3	—	—	Unused. This bit is always ‘‘0’’.
2	ND	No Data	Any one of the following: 1. READ DATA, READ DELETED DATA command, the 82078 did not find the specified sector. 2. READ ID command, the 82078 cannot read the ID field without an error. 3. READ TRACK command, the 82078 cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a ‘‘1’’ while the 82078 is executing a WRITE DATA, WRITE DELETED DATA, or FORMAT TRACK command.
0	MA	Missing Address Mark	Any one of the following: 1. The 82078 did not detect an ID address mark at the specified track after encountering the index pulse from the INDX# pin twice. 2. The 82078 cannot detect a data address mark or a deleted data address mark on the specified track.

7.3 Status Register 2

Bit No.	Symbol	Name	Description
7	—	—	Unused. This bit is always ‘‘0’’.
6	CM	Control Mark	Any one of the following: 1. READ DATA command, the 82078 encounters a deleted data address mark. 2. READ DELETED DATA command, the 82078 encountered a data address mark.
5	DD	Data Error in Data Field	The 82078 detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82078.
3	—	—	Unused. This bit is always ‘‘0’’.
2	—	—	Unused. This bit is always ‘‘0’’.
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the 82078 and is equal to FF hex which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The 82078 cannot detect a data address mark or a deleted data address mark.

7.4 Status Register 3

Bit No.	Symbol	Name	Description
7	—	—	Unused. This bit is always ‘‘0’’.
6	WP	Write Protected	Indicates the status of the WP pin.
5	—	—	Unused. This bit is always ‘‘1’’.
4	T0	TRACK 0	Indicates the status of the TRK0 pin.
3	—	—	Unused. This bit is always ‘‘1’’.
2	HD	Head Address	Indicates the status of the HDSEL pin.
1, 0	DS1, 0	Drive Select	Indicates the status of the DS1, DS0 pins.

8.0 COMPATIBILITY

The 82078 was designed with software compatibility in mind. It is a fully backwards compatible solution with the older generation 8272A and NEC765A/B disk controllers. The 82078 also implements on-board registers for compatibility with the Personal System/2s as well as PC/AT and PC/XT floppy disk controller subsystems. The 82078 is fully compatible with Intel's 386/486SL Microprocessor Superset. Upon reset, the 82078 samples IDENT0 and IDENT1 to determine PS/2, PC/AT or PS/2 Model 30 mode.

8.1 PS/2 vs AT vs Model 30 Mode

The 82078 operates in three different modes: PS/2, PC/AT, and Model 30. The 82078 is placed into the proper mode of operations upon Hardware RESET with the appropriate settings of the IDENT0 and IDENT1 pins.

8.2 Compatibility with the FIFO

The FIFO of the 82078 is designed to be transparent to non-FIFO disk controller software developed on the older generation 8272A standard. Operation of the 82078 FIFO can be broken down into two tiers of compatibility. For first tier compatibility, the FIFO is left in the default disabled condition upon a ''Hardware'' reset. In this mode the FIFO operates in a byte mode and provides complete compability with non-FIFO based software. For second tier compatibility, the FIFO is enabled via the CONFIGURE command. When the FIFO is enabled, it will temporarily enter a byte mode during the command and result phase of disk controller operation. This allows for compatible operation when interrogating the Main Status Register (MSR) for the purpose of transferring a byte at a time to or from the disk controller. For normal disk controller applications, the system designer can still take advantage of the FIFO for time critical data transfers during the execution phase and not create any conflicts with non-FIFO software during the command or result phase.

In some instances, use of the FIFO in any form has conflicted with certain specialized software. An example of a compatibility conflict using the FIFO is with software that monitors the progress of a data transfer during the execution phase. If the software assumed the disk controller was operating in a single byte mode and counted the number of bytes transferred to or from the disk controller to trigger some time dependent event on the disk media (i.e., head position over a specific data field), the same software will not have an identical time relationship if the FIFO is enabled. This is because the FIFO allows data to be queued up, and then burst transferred across the host bus. To accommodate software of this type, it is recommended that the FIFO be disabled.

8.3 Drive Polling

The 82078 supports the polling mode of the older generation 8272A. This mode is enabled upon a reset and can be disabled via the CONFIGURE command. This mode is supported for the sole purpose of providing backward compatibility with software that expects its presence.

The intended purpose of drive polling dates back to 8″ drives as a means to monitor any change in status for each disk drive present in the system. Each of the drives is selected for a period of time and its READY signal sampled. After a delay, the next drive is selected. Since the 82078 does not support READY in this capacity (internally tied true), the polling sequence is only simulated and does not affect the drive select lines (DS0–DS3) when it is active. If enabled, it occurs whenever the 82078 is waiting for a command or during SEEKs and RECALIBRATEs (but not IMPLIED SEEKs). Each drive is assumed to be not ready after a reset and a ''ready'' value for each drive is saved in an internal register as the simulated drive is polled. An interrupt will be generated on the first polling loop because of the initial ''not ready'' status. This interrupt must be followed with a SENSE INTERRUPT STATUS command from the host to clear the interrupt condition for each of the four logical drives.

9.0 Programming Guidelines

Programming the 82078 is identical to any other 8272A compatible disk controller with the exception of some additional commands. For the new designer, it is useful to provide some guidelines on how to program the 82078. A typical disk operation involves more than issuing a command and waiting for the results. The control of the floppy disk drive is a low level operation that requires software intervention at different stages. New commands and features have been added to the 82078 to reduce the complexity of this software interface.

9.1 Command and Result Phase Handshaking

Before a command or parameter byte can be issued to the 82078, the Main Status Register (MSR) must be interrogated for a ready status and proper FIFO direction. A typical floppy controller device driver should contain a subroutine for sending command or

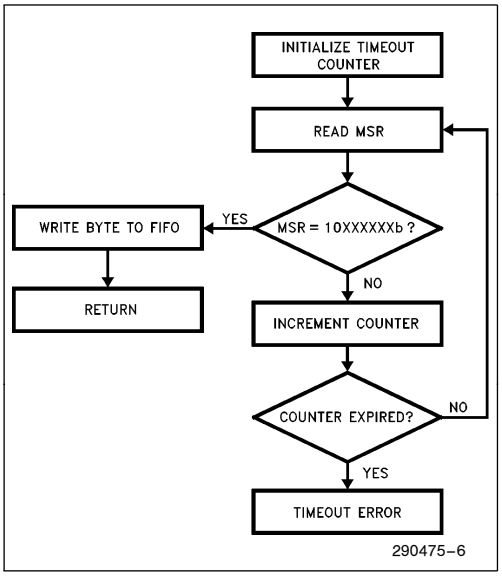


Figure 9-1. Send__Byte Routine

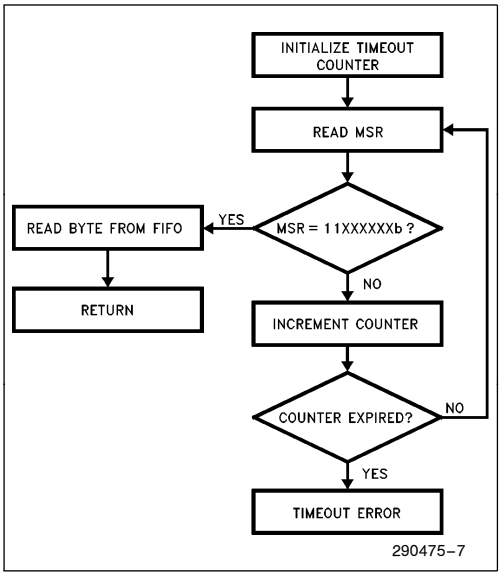


Figure 9-2. Get__Byte Routine

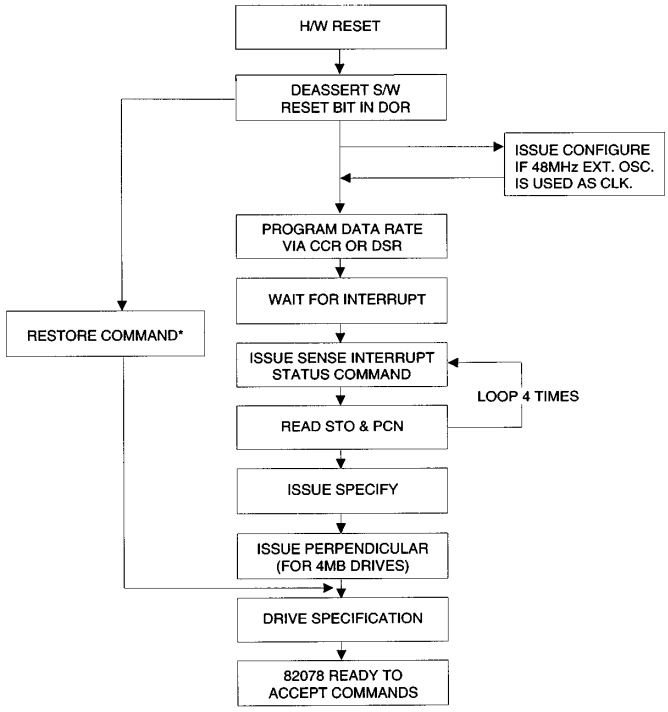
parameter bytes. For this discussion, the routine will be called ''Send__byte'' with the flowchart shown in Figure 9-1.

The routine loops until RQM is 1 and DIO is 0 indicating a ready status and FIFO direction is inward. If this condition is true, the 82078 is ready to accept a command or parameter byte. A timeout counter is used to insure software response within a reasonable amount of time in case of no response by the 82078. As a note, the programmer must be careful how the maximum delay is chosen to avoid unnecessary timeouts. For example, if a new command is issued when the 82078 is in the middle of a polling routine, the MSR will not indicate a ready status for the next parameter byte until the polling sequence completes the loop. This could cause a delay between the first and second bytes of up to 250 μs (@ 250 Kbps). If polling is disabled, this maximum delay is 175 μs. There should also be enough timeout margin to accommodate a shift of the software to a higher speed system. A timeout value that results in satisfactory operation on a 16 MHz CPU might fail when the software is moved to a system with a 25 MHz CPU. A recommended solution is to derive the timeout counter from a system hardware counter that is fixed in frequency from CPU clock to CPU clock.

For reading result bytes from the 82078, a similar routine is used. Figure 9-2 illustrates the flowchart for the routine ''Get__byte''. The MSR is polled until RQM is 1 and DIO is 1, which indicates a ready status and outward FIFO direction. At this point, the host can read a byte from the FIFO. As in the Send__byte routine, a timeout counter should be incorporated in case of a disk controller lock-up condition. For example, if a disk was not inserted into the disk drive at the time of a read operation, the controller would fail to receive the index pulse and lock-up since the index pulses are required for termination of the execution phase.

9.2 Initialization

Initializing the 82078 involves setting up the appropriate configuration after a reset. Parameters set by the SPECIFY command are undefined after a system reset and will need to be reinitialized. CONFIGURE command parameters default to a known state after a system reset but will need to be reinitialized if the system requirements are different from the default settings. This can be accomplished in two ways, either issue the individual commands, or issue the Restore command (assuming the Save command was issued). The Restore command is a succinct way to initialize the 82078, this is the preferable method if the system power management powers the 82078 on and off frequently. The flowchart for the recommended initialization sequence of the 82078 is shown in Figure 9-3.



*Sense Interrupt Status may be required if Restore CMD is not issued within 250 μs of trailing edge of H/W reset (@1 Mbps).

Figure 9-3. Initialization Flowchart

Following a reset of the 82078, the Configuration Control Register (CCR) should be reinitialized for the appropriate data rate. An external reset via the RESET pin will cause the data rate and write precompensation values to default to 250 Kbps (10b) and 125 ns (000b) respectively. Since the 125 ns write precompensation value is optimal for the 5 ¼″ and 3 ½″ disk drive environment, most applications will not require the value to be changed in the initialization sequence. As a note, a software reset issued via the DOR or DSR will not affect the data rate or write precompensation values. But it is recommended as a safe programming practice to always program the data rate after a reset, regardless of the type.

Since polling is enabled after a reset of the 82078, four SENSE INTERRUPT STATUS commands need to be issued afterwards to clear the status flags for each drive. The flowchart in Figure 9-3 illustrates how the software clears each of the four interrupt status flags internally queued by the 82078. It should be noted that although four SENSE INTERRUPT STATUS commands are issued, the INT pin is only active until the first SENSE INTERRUPT STATUS command is executed.

As a note, if the CONFIGURE command is issued within 250 μs of the trailing edge of reset (@1 Mbps), the polling mode of the 82078 can be disabled before the polling initiated interrupt occurs. Since polling stops when the 82078 enters the command phase, it is only time critical up to the first byte of the CONFIGURE command. If disabled in time, the system software no longer needs to issue the four SENSE INTERRUPT STATUS commands to clear the internal interrupt flags normally caused by polling.

The CONFIGURE command should also be issued if the system requirements are different from the default settings. For example, the CONFIGURE command can be used to enable the FIFO, set the threshold, and enable Implied Seeks.

The non-DMA mode flag, step rate (SRT), head load (HLT), and head unload times (HUT) programmed by the SPECIFY command do not default to a known state after a reset. This behavior is consistent with the 8272A and has been preserved here for compatibility. Thus, it is necessary to always issue a SPECIFY command in the initialization routine.

9.3 Recalibrates and Seeks

Commands that position the disk head are different from the typical READ/WRITE/FORMAT command in the sense that there is no result phase. Once a RECALIBRATE, SEEK, or RELATIVE SEEK command has been issued, the 82078 will return a ready status in the Main Status Register (MSR) and perform the head positioning operation as a background task. When the seek is complete, the 82078 will assert the INT signal to request service. A SENSE INTERRUPT STATUS command should then be asserted to clear the interrupt and read the status of the operation. Since the drive and motor enable signals are directly controlled through the Digital Output Register (DOR) on the 82078, a write to the DOR will need to precede the RECALIBRATE or SEEK command if the drive and motor is not already enabled. Figure 9-4 shows the flow chart for this operation.

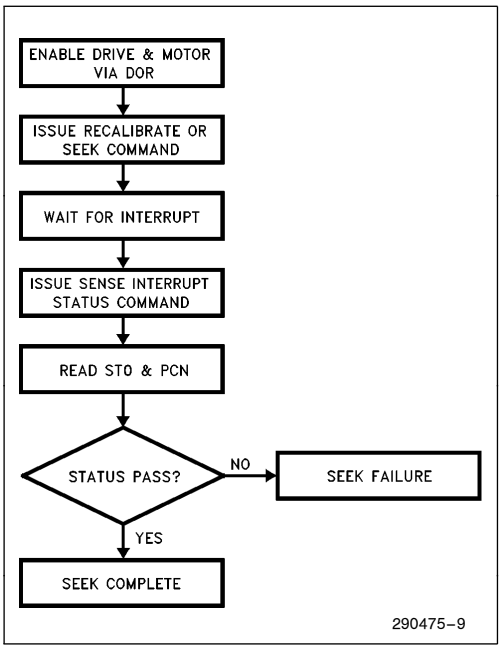


Figure 9-4. Recalibrate and Seek Operations

9.4 Read/Write Data Operations

A read or write data operation requires several steps to complete successfully. The motor needs to be turned on, the head positioned to the correct cylinder, the DMA controller initialized, the read or write command initiated, and an error recovery scheme implemented. The flowchart in Figure 9-5 highlights a recommended algorithm for performing a read or write data operation.

Before data can be transferred to or from the diskette, the disk drive motor must be brought up to speed. For most 3½″ disk drives, the spin-up time is 300 ms, while the 5¼″ drive usually requires about 500 ms due to the increased moment of inertia associated with the larger diameter diskette.

One technique for minimizing the motor spin-up delay in the read data case is to begin the read operation immediately after the motor is turned on. When the motor is not initially up to speed, the internal data separator will fail to lock onto the incoming data stream and report a failure in the status registers. The read operation is then repeated until successful status is obtained. There is no risk of a data integrity problem since the data field is CRC validated. But, it is not recommended to use this technique for the write data operation even though it requires successful reading of the ID field before the write takes place. The data separator performance of the 82078 is such that locking to the data stream could take place while the motor speed variation is still significant. This could result in errors when an attempt is made to read the disk media by other disk controllers that have a narrower incoming data stream frequency bandwidth.

After the motor has been turned on, the matching data rate for the media inserted into the disk drive should then be programmed to the 82078 via the Configuration Control Register (CCR). The 82078 is designed to allow a different data rate to be programmed arbitrarily without disrupting the integrity of the device. In some applications, it is required to automatically determine the recorded data rate of the inserted media. One technique for doing this is to perform a READ ID operation at each available data rate until a successful status is returned in the result phase.

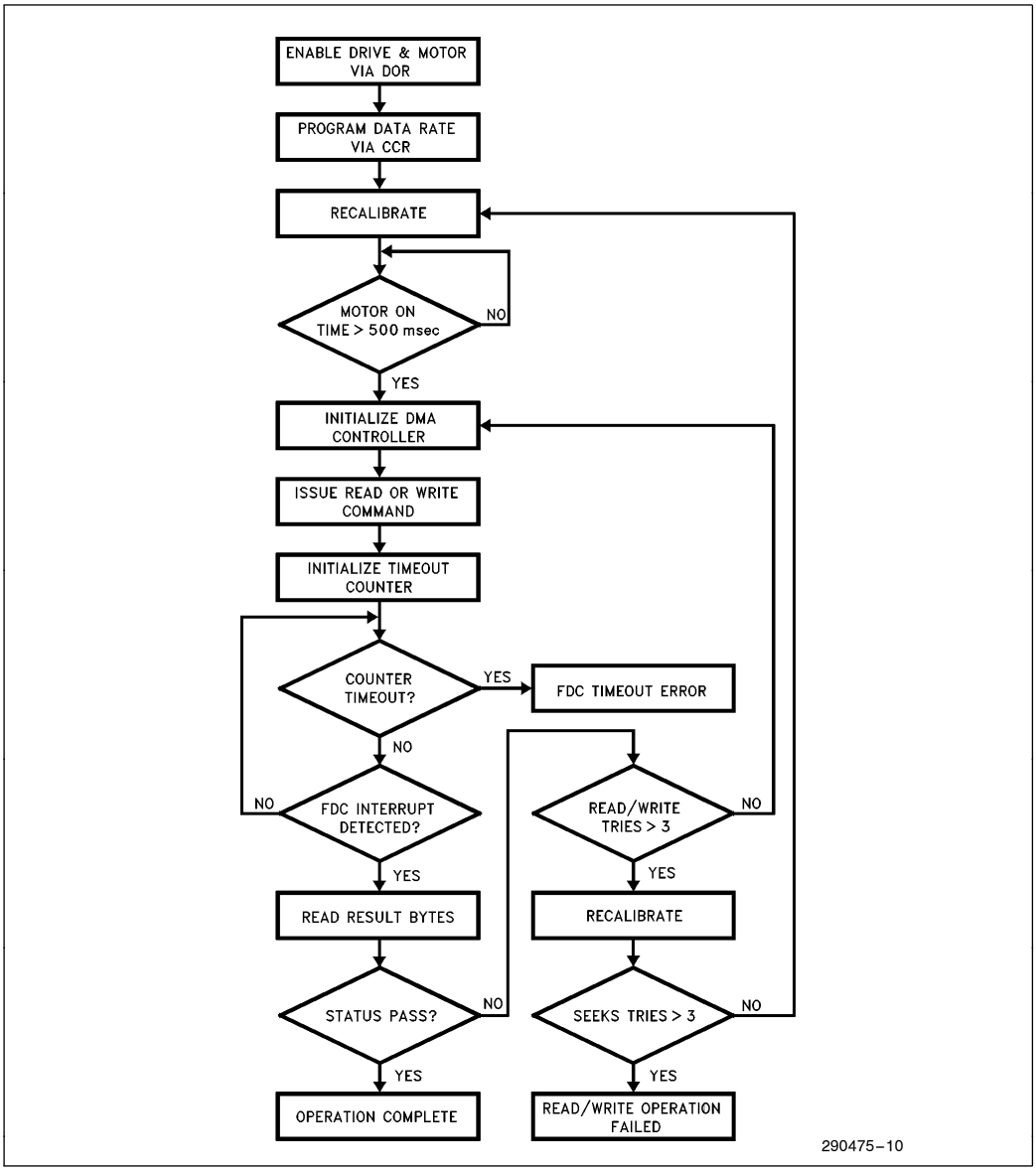


Figure 9-5. Read/Write Operation

If implied seeks are not enabled, the disk drive head must be positioned over the correct cylinder by executing a SEEK command. After the seek is complete, a head settling time needs to be asserted before the read or write operation begins. For most drives, this delay should be a minimum of 15 ms. When using implied seeks, the minimum head settling time can be enforced by the head load time (HLT) parameter designated in the SPECIFY command. For example, a HLT value of 8 will yield an effective head settling time of 16 ms for a programmed data rate of 500 Kbps. Of course if the head is already positioned over the correct cylinder, the head settling time does not need to be enforced.

The DMA controller is then initialized for the data transfer and the read or write command is executed. Typically the DMA controller will assert Terminal Count (TC) when the data transfer is complete. The 82078 will then complete the current data transfer and assert the INT signal signifying it has entered the result phase. The result phase can also be entered by the 82078 if an error is encountered or the last sector number equals the End of Track (EOT) parameter.

Based on the algorithm in Figure 9-5, if an error is encountered after reading the result bytes, two more retries are performed by reinitializing the DMA controller and re-issuing the read or write data command. A persisting failure could indicate the seek operation did not achieve proper alignment between the head and the track. The disk head should then be recalibrated and the seek repeated for a maximum of two more tries. Unsuccessful operation after this point should be reported as a disk failure to the operating system.

9.5 Formatting

The disk formatting procedure involves positioning the head on each track and creating a fixed format field used for organizing the data fields. The flowchart in Figure 9-6 highlights the typical format procedure.

After the motor has been turned on and the correct data rate programmed, the disk head is recalibrated to track 0. The disk is then allowed to come up to speed via a 500 ms delay. It is important the disk speed has stabilized before the actual formatting to avoid any data rate frequency variations. Since the format fields contain critical information used by the data separator of the disk controller for synchronization purposes, frequency stability of the data stream is imperative for media interchangeability among different systems.

The ID field data created on the disk during the format process is provided by the DMA controller during the execution phase. The DMA controller is initialized to send the C, H, R and N values for each sector ID field. For example, to format cylinder 7, on head 1, with 9 sectors, and a sector size of 2 (512 bytes), the DMA controller should be programmed to transfer 36 bytes (9 sectors $\times$ 4 bytes per sector) with the following data field: 7,1,1,2, 7,1,2,2, 7,1,3,2, ... 7,1,9,2. Since the values provided to the 82078 during the execution phase of the format command are directly recorded as the ID fields on the disk, the data contents can be arbitrary. Some forms of copy protection have been implemented by taking advantage of this capability.

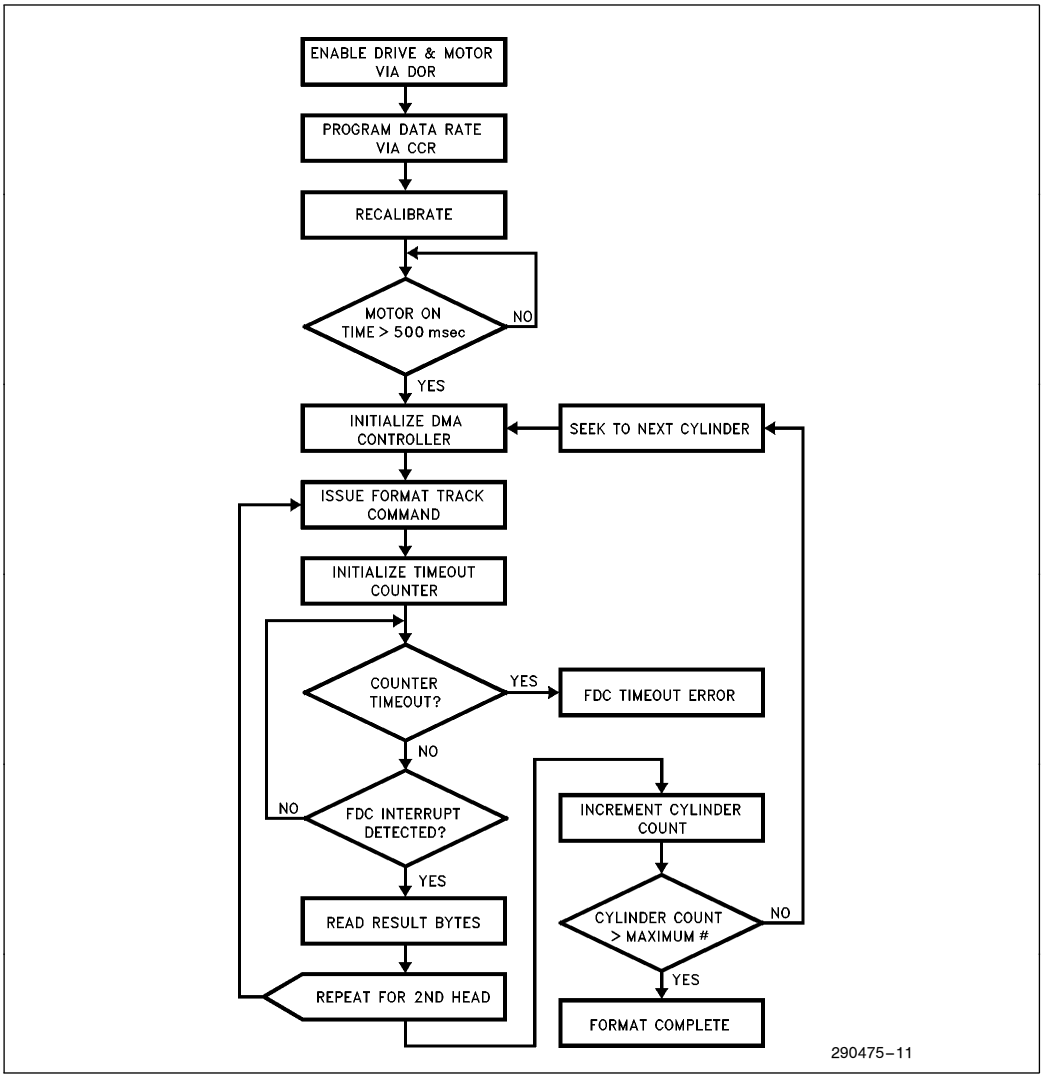


Figure 9-6. Formatting

After each head for a cylinder has been formatted, a seek operation to the next cylinder is performed and the format process is repeated. Since the FORMAT TRACK command does not have implied seek capability, the SEEK command must be used. Also, as discussed in Section 9.2, the head settling time needs to be adhered to after each seek operation.

9.6 Save and Restore

The Save and Restore commands were developed for portable systems that use zero-volt powerdown to conserve power. These systems turn off the V_{CC} to most of the system and retain the system status in a specific location. In older floppy controller designs, in order for system designers to retrieve the floppy controller status, a lot of separate commands and register reads were required. The Save command stores the key status information in a single command, the Restore command restores this information with a single command. These commands can be integrated into the SMM module that is responsible for zero-volt powerdown.

The sequence of initializing the 82078 after a reset occurred and assuming a Save command was issued follows:

- Issue the Drive Spec command (if the design utilizes this command)
- Issue the Restore command

The Restore command programs the data rate and precompensation value via the DSR. It then restores the values normally programmed through the Configure, Specify, and Perpendicular commands. It also enables the previously selected values for the AUTO Powerdown command. The command then restores the PCN values to its previous values. The user is responsible for issuing the seek and recalibrate commands to restore the head to the proper location. There are some drives that do not recalibrate in which case the Restore command will restore the previous state completely. The PDOSC bit is retrievable using the Save command, however it is up to the system designer to set it correctly. The software must allow at least 20 μs to execute the Restore command. When using the BOOTSEL bits in the TDR, the user must restore or reinitialize these bits to their proper values.

9.7 Verifies

In some applications, the sector data needs to be verified immediately after each write operation. One verify technique reinitializes the DMA controller to perform a read transfer or verify transfer (DACK# is asserted but not RD#) immediately after each write operation. Issue a read command to the disk controller and the resulting status indicates if the CRC validated the previously written data. This technique has the drawback of requiring additional software intervention by having to reprogram the DMA controller between each sector write operation. The 82078 supports this verify technique but also provides a VERIFY command that does not require the use of the DMA controller.

To verify a write data transfer or format track operation using the VERIFY command, the software simply issues the command with the same format as a READ DATA command but without the support of the DMA controller. The 82078 will then perform a disk read operation without a host data transfer. The CRC will be calculated for each sector read and compared against the value stored on the disk. When the VERIFY command is complete, the status register reports detected CRC errors.

9.8 Powerdown State and Recovery

The two power management modes coupled with the internal oscillator power management forms an important consideration for programming the 82078. The recovery of 82078 and the time it takes to achieve complete recovery depends on how 82078 is powered down and how it is awakened. The following sections describe all the programming concerns and subtleties involved in using power management features of the 82078.

9.8.1 OSCILLATOR POWER MANAGEMENT

Section 4.1 covers the power management scheme involved in powering down of both an internal and an external oscillator. Both types of oscillators face drop out effects and require recovery times on the order of tens of milliseconds (this may be objectionable to some application software). This means that if the oscillator is powered down then it is imperative for the software to assure enough time for the oscillator to recover to a stable state. Oscillator power management must be controlled by the system software especially to maintain software transparency. In cases where the system goes into a standby mode (by user request or system time-out), the power management software can turn off the oscillator to conserve power. This can also be controlled in hardware using the Powerdown (PD) pin. Complete recovery from an oscillator powerdown state requires the software to turn on the oscillator sufficiently ahead of awakening the 82078.

9.8.2 PART POWER MANAGEMENT

The part powerdown and wake up modes are covered in Section 4.2 in detail. This section is meant to address the programming concerns for the part (excluding the oscillator) during these modes.

9.8.2.1 Powerdown Modes

For both types of powerdown modes—DSR powerdown and auto powerdown, if reset is used to exit the part from powerdown then the internal microcontroller will go through a standard sequence: register initialization followed after some delay by an interrupt.

Software transparency in auto powerdown mode is preserved by MSR retaining the value of 80H which indicates that the part is ready to receive a command. This feature allows the part to powerdown while maintaining its responsiveness to any application software.

The PD and IDLE status bits can be monitored via the Status Register B (SRB, enhanced AT/EISA mode) and in the Digital Input Register (DIR, PS/2 and Model 30). Since the IDLE pin stays high when the 82078 is in idle state, the IDLEMSK bit can be used to set the pin low again (as part of a power management routine).

9.8.2.2 Wake Up Modes

Wake up from DSR powerdown results in the part being internally reset and all present status being lost. During DSR powerdown the RQM bit in the MSR is set. A software or hardware reset will wake up the part.

The case for wake up from auto powerdown is different. The BIOS and application software are very sensitive to delays involved in writing the first command bytes to the 82078. Most programs have short error time-outs in these cases. Such programs would not tolerate any floppy disk controller that was unable to receive the first byte of a command at any time. The following describes how 82078 uniquely sustains its software transparency during wake up sequences.

Prior to writing a command to 82078, it is first necessary to read the MSR to ensure that the 82078 is ready (RQM bit must be set) to receive the command. When the part detects a MSR read, it assumes that another command will follow and begins the wake up process. While the part is waking up it does not change the state of the MSR (MSR = 80H) and is able to receive the command in the FIFO. At this point one of the two following scenarios can occur.

No other command is sent subsequent to the MSR read. The part wakes up and initializes the minimum power up timer. Upon the expiration of this timer the part is once again put in powerdown state.

Another command follows the MSR read. If the command is sent during the part's recovery from powerdown, the part remembers the command, clears the RQM bit (to prevent further bytes being written) and acts on the command once it is fully awake.

If the MSR was not checked prior to writing of a command, the part will proceed as stated above with the RQM bit cleared and the command byte held until the internal microcontroller is ready. Writing the motor enable bits in DOR active will initiate the wake up sequence with RQM set high, ready to receive any command.

As it is clear from the above discussion, the immediate access to the floppy disk controller for the first command byte is vital to software transparency. The recovery of the part from powerdown may involve a delay after the first command byte has been issued. However, all programs have tolerance for the delay after the first command byte is issued. In a powered up chip, it is possible for the microcontroller to be in its ''polling loop''. As a result the tolerance for this delay provides an excellent window for recovery of the part.

10.0 DESIGN APPLICATIONS

10.1 Operating the 82078SL in a 3.3V Design

The design for 3.3V is the same as for 5.0V with two exceptions: The SEL3V# pin must be held low to select 3.3V operation, and the VCCF pin can be either 3.3V or 5.0V (VCCF can only be 5.0V when SEL3V# is high). The VCCF pin allows the controller to be operated in mixed (3.3V/5.0V) mode. For example, if the system operates at 3.3V and the floppy disk drive operates at 5.0V, the 82078 can be configured to operate at 3.3V with 5.0V available to the drive interface. See Figure 10-1 for a schematic.

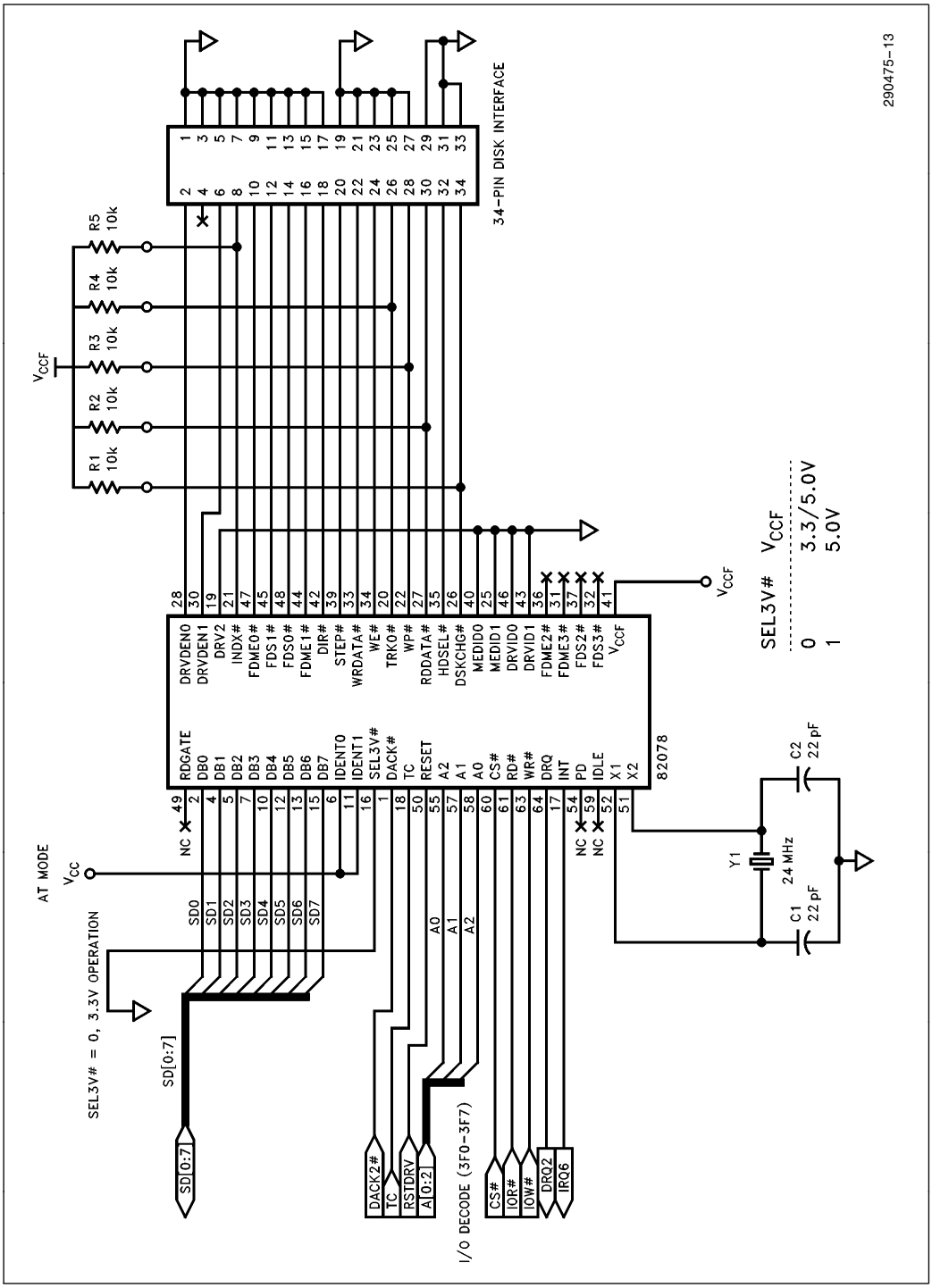


Figure 10-1. 82078SL 3.3V Design

10.2 Selectable Boot Drive

Generally a standard personal computer is configured with a 1.2 Mb 5.25″ disk drive and a 1.44 or 2.88 Mb 3.5″ disk drive. Usually the drive connects as ‘‘A:’’ and is the boot drive. At times the user may want to configure ‘‘B:’’ as the boot drive. Currently some BIOS’ use a special implementation in software to accomplish this. The 82078 now offers this capability more efficiently by configuring the boot drives.

The 82078 allows for virtual drive designations. This is a result of allowing multiplexing the boot drive select and motor enable lines. This is shown in the Figure 10-2.

The DRIVE SEL1 and the DRIVE SEL2 bits in the DOR register decode internally to generate the signals DSn. The MEn signals generate directly from the DOR register. The DSn and MEn signals get mapped to actual FDSn and FDMEn pins based on the BOOTSELn bits (selected in the TDR register). The exact mapping of BOOTSEL vs. the FDSn and FDMEn pins is shown in the following table.

BOOTSEL1	BOOTSEL0	Mapping:
0	0	DS0 → FDS0, ME0 → FDME0 DS1 → FDS1, ME1 → FDME1 DS2 → FDS2, ME2 → FDME2
0	1	DS0 → FDS1, ME0 → FDME1 DS1 → FDS0, ME1 → FDME0 DS2 → FDS2, ME2 → FDME2
1	0	DS0 → FDS2, ME0 → FDME2 DS1 → FDS1, ME1 → FDME1 DS2 → FDS0, ME2 → FDME0
1	1	Reserved

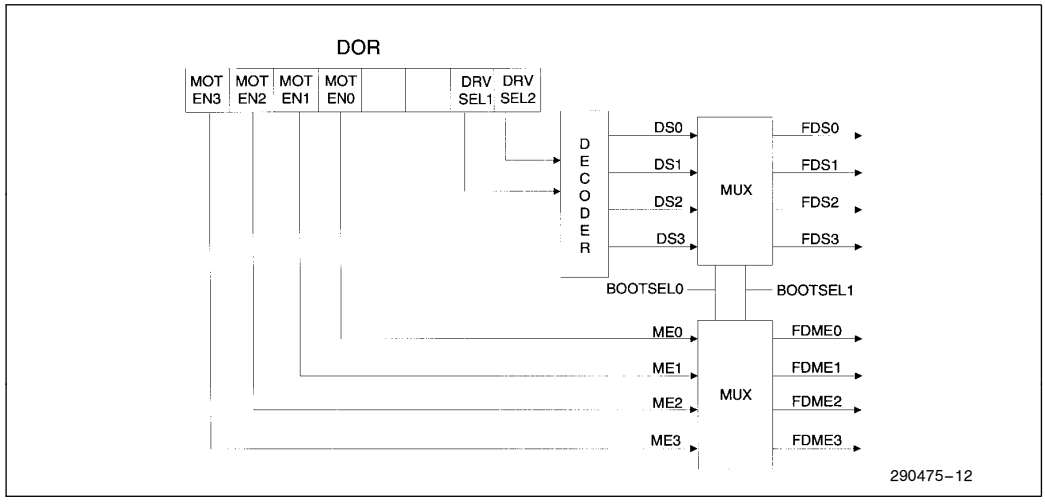


Figure 10-2. Virtual Drive Configuration

The BOOTSELn bits allow users to multiplex the output drive signals allowing different drives to be the boot drive. The DSn and MEn bits are considered virtual designations since the DSn and MEn signals get remapped to different corresponding physical FDSn and FDMEn pins. In other words, once the BOOTSELn bits are configured for a non-default selection, all future references made to the controller will be assumed as virtual designations. For example, if BOOTSEL1, BOOTSEL0 = 10 then DOR[1:0] = 00 refers to drive 2 and FDS2, FDME2 lines will be activated. Also, if TAPESEL[1:0] = 10, then tape mode is selected whenever FDS0, FDME0 are selected. Note, due to the virtual designations TAPESEL[1:0] = 00 would never enable tape mode due to boot drive restrictions.

10.3 How to Disable the Native Floppy Controller on the Motherboard

There are occasions when the floppy controller designed onto the motherboard of a system needs to be disabled in order to operate another floppy controller on the expansion bus. This can be done without changing the BIOS or remapping the address of the floppy controller (provided there is a jumper, or another way to disable the chip select on the native controller).

Upon reset, the DOR register in the 82078 is set to 00H. If the CS# is left enabled during the POST, the DOR is set to 0CH, this enables the DMA GATE# bit in the DOR. When this bit is set the 82078 treats a DACK# and a RD# or WR# as an internal chip select (CS#). Bus contention will occur between the native controller and the auxiliary controller if the DMA GATE# bit becomes active, even if the CS# signal is not present.

The proper way to disable the native floppy controller is to disable the CS# before the system is turned on. This will prevent the native controller from getting initialized. Another option is to map the native controller to a secondary address space, then disable the DMA GATE# via the DOR disabling the DMA GATE#. This assumes that the native controller is switchable to a secondary address space.

10.4 Replacing the 82077SL with a 82078 in a 5.0V Design

The 82078 easily replaces the 5.0V 82077SL with minimum design changes. With a few exceptions, most of the signals are named as they were in the 82077SL. Some pins were eliminated and other renamed to accommodate a reduced pin count and smaller package.

The connections to the AT bus are the same as the 82077SL with the following exceptions: MFM and IDENT have been replaced by IDENT1 and IDENT0. The PLL0 pin was removed. Configure the tape drive mode on the 82078 via the Tape Drive Register (TDR).

The Drive Interface on the 82078 is also similar to the 82077SL except as noted: DRVDEN0 and DRVDEN1 on the 82078 take the place of DENSEL, DRATE0, and DRATE1 on the 82077SL. The Drive Specification Command configures the polarity of these pins, thus selecting the density type of the drive. The Motor Enable pins (ME0-3) and the Drive Select pins (DS0-3) are renamed FDME(0-3) and FDS(0-3) respectively on the 82078. 10K pull-up resistors can be used on the disk interface. See Figure 10-3 for a schematic of the connection.

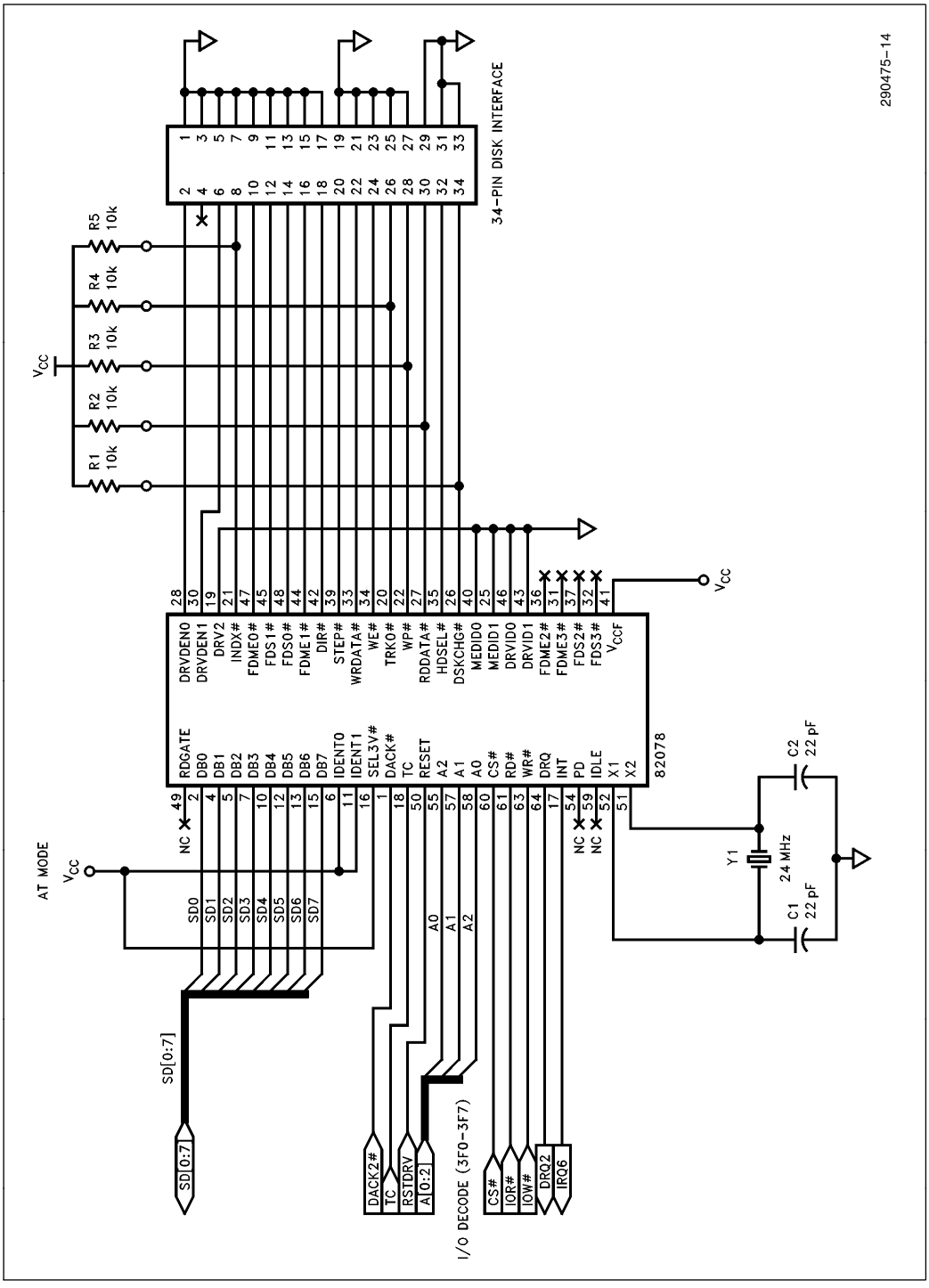


Figure 10-3. 82077SL Conversion to 82078-1

Pin Changes on the 64 Pin Part:

- INVERT# is removed
- 4 NC's (no connects) are removed
- MFM, IDENT pins on the 82077SL have been changed to IDENT1 and IDENT0 respectively.
- PLL0 pin, which allowed for H/W configuration of tape drive mode is no longer available. Tape mode can be configured via the TDR register.
- DENSEL, DRATE1, DRATE0 pins have been substituted by DRVDEN0, DRVDEN1. The Drive Specification command can be used to configure these pins for various requirements of drives available on the market.
- RDGATE has been added and can be used for diagnostics of the PLL.
- MEDID1, MEDID0 are new, they return media type information to the TDR register.
- DRVID1, DRVID0 return drive type information to the TDR register.
- SEL3V# selects between either 3.3V or 5V mode. Connecting the pin LOW selects 3.3V mode.
- 5 VSS pins, 2 VCC pins, 2 VSSP pins, 1 VCCF pin, and 1 AVCC and 1 AVSS pin.
- VCCF can be used to interface a 5.0V or a 3.3V drive to the 82078 (when SEL3V# is low).
- The Hardware RESET pulse width has changed from 170 times the oscillator period to 100 ns plus 25 times the oscillator period.

11.0 D.C. SPECIFICATIONS

11.1 Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Supply Voltage	−0.5V to +8.0V
Voltage on Any Input	GND −2V to 6.5V
Voltage on Any Output	GND −0.5V to V_{CC} +0.5V
Power Dissipation	1W

11.2 D.C. Characteristics T_A = 0°C to 70°C, V_{SS} = AV_{SS} = 0V

64 PIN D.C. CHARACTERISTICS

Symbol	Parameter	V_{CC} = +5V ±10%(7)			V_{CC} = 3.3V ± 0.3V		
		Min(V)	Max(V)	Test Conditions	Min(V)	Max(V)	Test Conditions
V_{ILC}	Input Low Voltage, X1	−0.5	0.8		−0.3	0.8	
V_{IHC}	Input High Voltage, X1	3.9	V_{CC} + 0.5		2.4	V_{CC} + 0.3	
V_{IL}	Input Low Voltage (all pins except X1)	−0.5	0.8		−0.3	0.8	
V_{IH}	Input High Voltage (all pins except X1)	2.0	V_{CC} + 0.5		2.0	V_{CC} + 0.3	
V_{OL}(8)	System Interface		0.45	I_{OL} = 12 mA		0.45	I_{OL} = 6 mA
	FDD Interface outputs		0.45	I_{OL} = 24 mA		0.45	I_{OL} = 12 mA
	Status Outputs (Note 6)		0.45	I_{OL} = 4 mA		0.45	I_{OL} = 4 mA
V_{OH}	All outputs	3.0		I_{OH} = −4.0 mA	2.4		I_{OH} = −2.0 mA
	All outputs	V_{CC} − 0.4		I_{OH} = −100 µA	V_{CC} − 0.2		I_{OH} = −100 µA

64 PIN D.C. CHARACTERISTICS (I_{CC})

Symbol	Parameter	V_{CC} = +5V ±10%(7)			V_{CC} = 3.3V ± 0.3V		
		Typ	Max(A)	Test Conditions	Typ	Max(A)	Test Conditions
I_{CC1}	1 Mbps Data Rate V_{IL} = V_{SS}, V_{IH} = V_{CC}	15.4 mA	25 mA	(Notes 1, 2, 5)	8.4 mA	16 mA	(Notes 1, 2)
I_{CC2}	1 Mbps Data Rate V_{IL} = 0.45V, V_{IH} = 2.4V	20.8 mA	30 mA	(Notes 1, 2, 5)	8.6 mA	16 mA	(Notes 1, 2)
I_{CC3}	500 Kbps Data Rate V_{IL} = V_{SS}, V_{IH} = V_{CC}	11.8 mA	20 mA	(Notes 1, 2)	6.2 mA	14 mA	(Notes 1, 2)
I_{CC4}	500 Kbps Data Rate V_{IL} = 0.45V, V_{IH} = 2.4V	17.6 mA	25 mA	(Notes 1, 2)	6.2 mA	14 mA	(Notes 1, 2)
I_{CCSB}	I_{CC} in Powerdown	0 µA	60 µA	(Notes 3, 4)	0 µA	60 µA	(Notes 3, 4)

64 PIN D.C. CHARACTERISTICS (I_{CC}) (Continued)

Symbol	Parameter	$V_{CC} = +5V \pm 10\%$(7)			$V_{CC} = 3.3V \pm 0.3V$		
		Typ	Max(A)	Test Conditions	Typ	Max(A)	Test Conditions
I_{IL}	Input Load Current (all input pins)		10 μA −10 μA	$V_{IN} = V_{CC}$ $V_{IN} = 0V$		10 μA −10 μA	$V_{IN} = V_{CC}$ $V_{IN} = 0V$
I_{OFL}	Data Bus Output Float Leakage		±10 μA	$0.45 < V_{OUT} < V_{CC}$		±10 μA ±10 μA	$0.45 < V_{OUT} < V_{CC}$

NOTES:
1. Only the data bus inputs may float.
2. Tested while reading a sync field of ''00''. Outputs not connected to D.C. loads.
3. $V_{IL} = V_{SS}$, $V_{IH} = V_{CC}$; Outputs not connected to D.C. loads.
4. Typical value with the oscillator off.
5. I_{CC} for 2 Mbps Data Rate: Max 40 mA (TTL), 35 mA (CMOS) at 5.5V, typical 29.2 mA (TTL) and 24.4 (CMOS).
6. Status outputs are PD, IDLE, and RDGATE.
7. V_{CC} and V_{CCF} for the 82078-1 is +5V ±5%.
8. V_{OL} change effective for both 44-pin and 64-pin package offerings.

64 PIN MIXED MODE D.C. CHARACTERISTICS

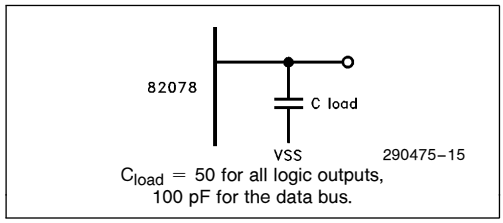
Symbol	Parameter	$V_{CC} = 3.3V \pm 0.3V$, $V_{CCF} = +5V \pm 10\%$(7)		
		Min(V)	Max(V)	Test Conditions
V_{ILC}	Input Low Voltage, X1	−0.3	0.8	
V_{IHC}	Input High Voltage, X1	2.4	$V_{CC} + 0.3$	
V_{IL}	Input Low Voltage (system pins except X1) (floppy drive interface pins)	−0.3 −0.5	0.8 0.8	
V_{IH}	Input High Voltage (system interface pins except X1) (floppy drive interface pins)	2.0 2.0	$V_{CC} + 0.3$ $V_{CC} + 0.5$	
V_{OL}	System Interface		0.4	$I_{OL} = 6$ mA
	FDD Interface outputs		0.4	$I_{OL} = 24$ mA
	Status Pins: IDLE, PD, RDGATE		0.4	$I_{OL} = 4$ mA
V_{OH}	All system outputs	2.4		$I_{OH} = -2.0$ mA
	All FDD interface outputs	3.0		$I_{OH} = -4.0$ mA
	All system outputs	$V_{CC} - 0.2$		$I_{OH} = -100$ μA
	All FDD interface outputs	$V_{CC} - 0.4$		$I_{OH} = -100$ μA

CAPACITANCE

C_{IN}	Input Capacitance	10	pF	F = 1 MHz, T_A = 25°C
C_{IN1}	Clock Input Capacitance	20	pF	Sampled, not 100% Tested
$C_{I/O}$	Input/Output Capacitance	20	pF	

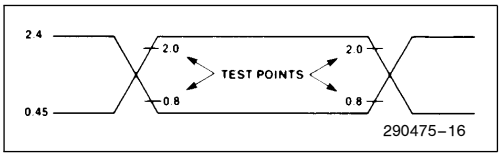
NOTE:
All pins except pins under test are tied to AC ground.

LOAD CIRCUIT

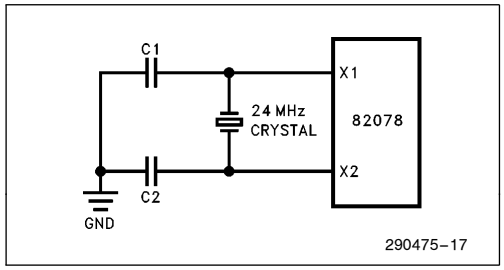


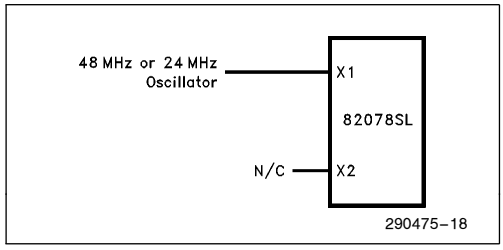
C_{load} = 50 for all logic outputs, 100 pF for the data bus.

A.C. TESTING INPUT, OUTPUT WAVEFORM



11.3 Oscillator





The 24 MHz clock can be supplied either by a crystal or a MOS level square wave. All internal timings are referenced to this clock or a scaled count which is data rate dependent.

The crystal oscillator must be allowed to run for 10 ms after V_{CC} has reached 4.5V or exiting the POWERDOWN mode to guarantee that it is stable.

Frequency:	24 MHz ±0.1%
Mode:	Parallel Resonant
	Fundamental Mode
Series Resistance:	Less than 40Ω
Shunt Capacitance:	Less than 5 pF

12.0 A.C. SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%(17), +3.3V ±0.3V, V_{SS} = AV_{SS} = 0V

Symbol	Parameter	Min	Max	Unit
CLOCK TIMINGS				
t1	Clock Rise Time		10	ns
	Clock Fall Time		10	ns
t2	Clock High Time(7)	16	26	ns
t3	Clock Low Time(7)	16	26	ns
t4	Clock Period	41.66	41.66	ns
t5	Internal Clock Period(3)			
HOST READ CYCLES				
t7	Address Setup to RD#	5		ns
t8	RD# Pulse Width	90		ns
t9	Address Hold from RD#	0		ns
t10	Data Valid from RD#(12)		80	ns
t11	Command Inactive	60		ns
t12	Output Float Delay		35	ns
t13	INT Delay from RD#(16)		t5 + 125	ns
t14	Data Hold from RD#	5		ns
HOST WRITE CYCLES				
t15	Address Setup to WR#	5		ns
t16	WR# Pulse Width	90		ns
t17	Address Hold from WR#	0		ns
t18	Command Inactive	60		ns
t19	Data Setup to WR#	70		ns
t20	Data Hold from WR#	0		ns
t21	INT Delay from WR#(16)		t5 + 125	ns
DMA CYCLES				
t22	DRQ Cycle Period(1)	6.5		µs
t23	DACK# to DRQ Inactive		75	ns
t23a	DRQ to DACK# Inactive	(Note 15)		ns
t24	RD# to DRQ Inactive(4)		100	ns
t25	DACK# Setup to RD#, WR#	5		ns
t26	DACK# Hold from RD#, WR#	0		ns
t27	DRQ to RD#, WR# Active(1)	0	6	µs
t28	Terminal Count Width(10)	50		ns
t29	TC to DRQ Inactive		150	ns
RESET				
t30	"Hardware" Reset Width(5)	1.13		µs
t30a	"Software" Reset Width(5)	(Note 11)		ns
t31	Reset to Control Inactive		2	µs

A.C. SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5V ±10%(17), +3.3V ±0.3V, V_{SS} = AV_{SS} = 0V (Continued)

Symbol	Parameter	Min	Max	Unit
WRITE DATA TIMING				
t32	Write Data Width(6)			ns
DRIVE CONTROL				
t35	DIR# Setup to STEP#(14)	1.0		µs
t36	DIR# Hold from STEP#	10		µs
t37	STEP# Active Time (High)	2.5		µs
t38	STEP# Cycle Time(2)			µs
t39	INDEX# Pulse Width	5		t5
t41	WE# to HDSEL# Change	(Note 13)		ms
READ DATA TIMING				
t40	Read Data Pulse Width	50		ns
t44	82078-1		2M	bits/sec
	82078SL		1M	bits/sec
t44	Data Rate Period = 1/f44			
tLOCK	Lockup Time		64	t44

NOTES:
1. This timing is for FIFO threshold = 1. When FIFO threshold is N bytes, the value should be multiplied by N and subtract 1.5 µs. The value shown is for 1 Mbps, scales linearly with data rate.
2. This value can range from 0.5 ms to 8.0 ms and is dependent upon data rate and the Specify command value.
3. Many timings are a function of the selected data rate. The nominal values for the internal clock period (t5) for the various data rates are:
   - 2 Mbps 1.5x oscillator period = 62.5 ns
   - 1 Mbps 3x oscillator period = 125 ns
   - 500 Kbps 6x oscillator period = 250 ns
   - 300 Kbps 10x oscillator period = 420 ns
   - 250 Kbps 12x oscillator period = 500 ns
4. If DACK# transitions before RD#, then this specification is ignored. If there is no transition on DACK#, then this becomes the DRQ inactive delay.
5. Reset requires a stable oscillator to meet the minimum active period.

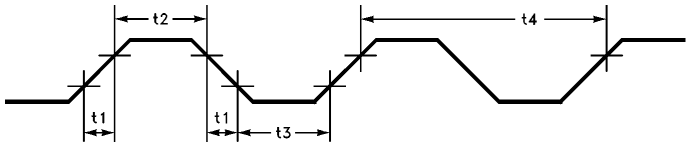
6. Based on the internal clock period (t5). For various data rates, the Write Data Width minimum values are:
   - 2 Mbps 2.5x oscillator period −50 ns = 75 ns
   - 1 Mbps 5x oscillator period −50 ns = 150 ns
   - 500 Kbps 10x oscillator period −50 ns = 360 ns
   - 300 Kbps 16x oscillator period −50 ns = 615 ns
   - 250 Kbps 19x oscillator period −50 ns = 740 ns
7. Test points for clock high time are 3.5V. Due to transitional times, clock high time max and clock low time max cannot be met simultaneously. Clock high time min and clock low time max can not be met simultaneously.
8. Based on internal clock period (t5).
9. Jitter tolerance is defined as:
   (Maximum bit shift from nominal position ÷ ¼ period of nominal data rate) × 100% is a measure of the allowable bit jitter that may be present and still be correctly detected. The data separator jitter tolerance is measured under dynamic conditions that jitters the bit stream according to a reverse precompensation algorithm.
10. TC width is defined as the time that both TC and DACK# are active. Note that TC and DACK# must overlap at least 50 ns.
11. The minimum reset active period for a software reset is dependent on the data rate, after the 82078 has been properly reset using the t30 spec. The minimum software reset period then becomes:
    - 2 Mbps 1.5 x t4 = 62.5 ns
    - 1 Mbps 3 x t4 = 125 ns
    - 500 Kbps 6 x t4 = 250 ns
    - 300 Kbps 10 x t4 = 420 ns
    - 250 Kbps 12 x t4 = 500 ns
12. Status Register's status bits which are not latched may be updated during a Host read operation.
13. The minimum MFM values for WE to HDSEL change (t41) for the various data rates are:
    - 2 Mbps 0.5 ms + [4 x GPL]
    - 1 Mbps 0.5 ms + [8 x GPL]
    - 500 Kbps 1.0 ms + [16 x GPL]
    - 300 Kbps 1.6 ms + [26.66 x GPL]
    - 250 Kbps 2.0 ms + [32 x GPL]

    GPL is the size of gap 3 defined in the sixth byte of a Write Command.
14. This timing is a function of the selected data rate as follows:
    - 2 Mbps 0.5 μs Min
    - 1 Mbps 1.0 μs Min
    - 500 Kbps 2.0 μs Min
    - 300 Kbps 3.3 μs Min
    - 250 Kbps 4.0 μs Min
15. This timing is a function of the internal clock period (t5) and is given as (⅔) t5. The values of t5 are shown in Note 3.
16. The timings t13 and t21 are specified for INT signal in the polling mode only. These timings in case of the result phase of the read and write commands are microcode dependent.

Part Specification	3.3V	5.0V	2 Mbps Data Rate
82078SL	X	X	
82078-1		X	X

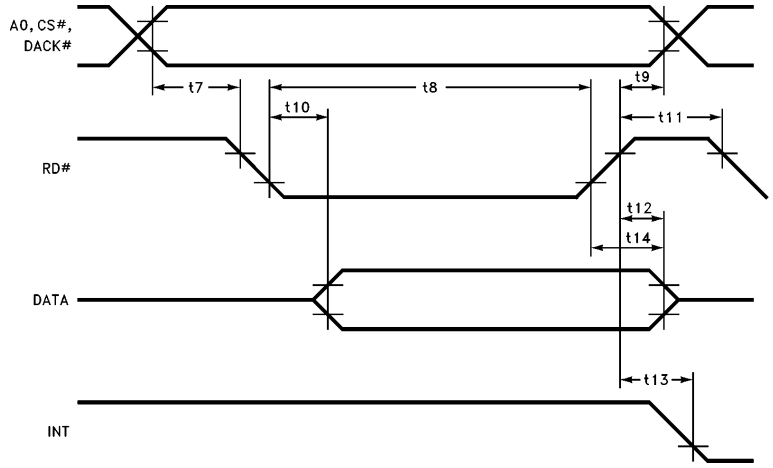
17. For 82078-1 only, V_{CC} and V_{CCF} requirements are +5V ±5%.

Clock Timings



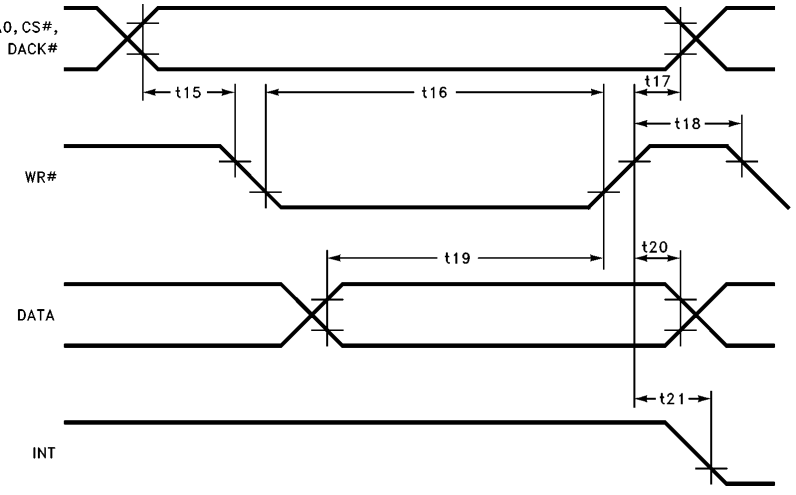
290475–19

Host Read Cycles



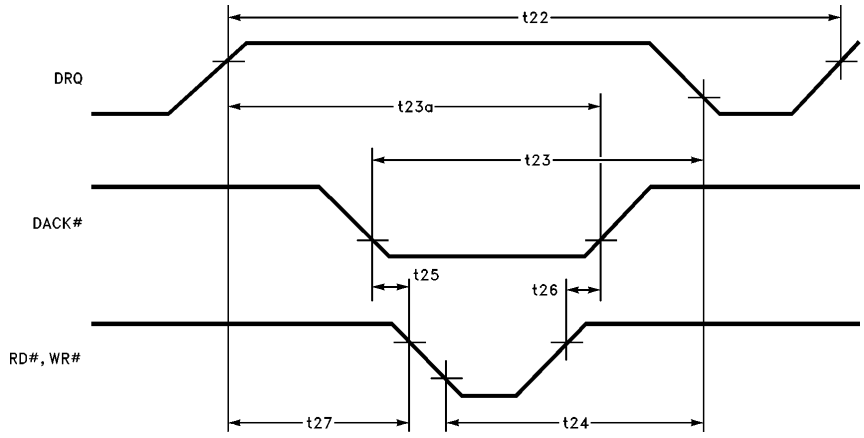
290475–20

Host Write Cycles



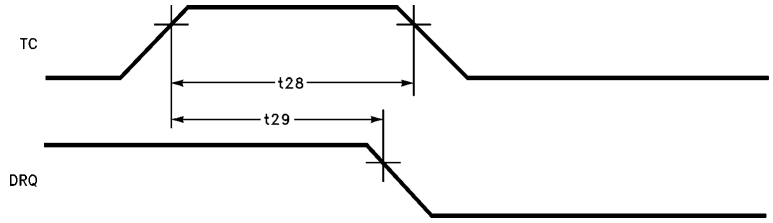
290475–21

DMA Cycles



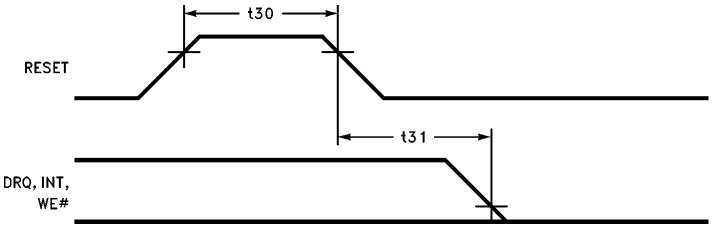
290475-22

Terminal Count



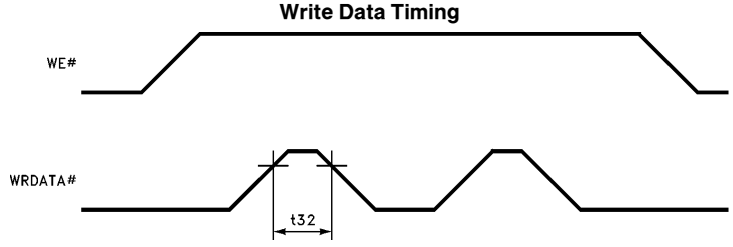
290475-23

Reset



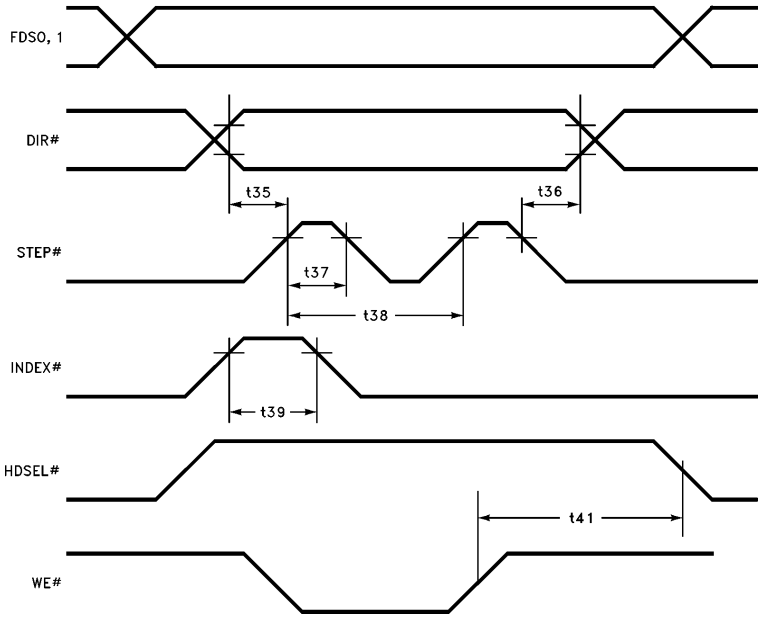
290475-24

Write Data Timing



290475–25

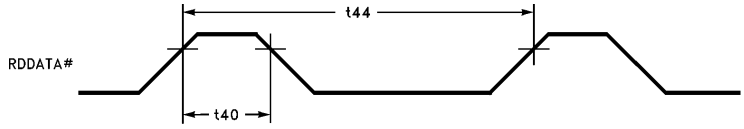
Drive Control



290475–26

NOTE:
For overlapped seeks, only one step pulse per drive selection is issued. Non-overlapped seeks will issue all programmed step pulses.

Internal PLL

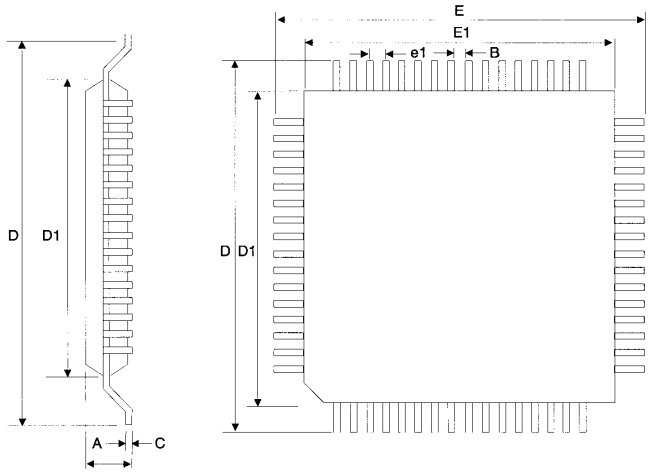


290475–27

12.1 Package Outline for the 64 QFP Part

The 82078 addresses the current need of the smaller and thinner packages, for the current market. The size of the part is becoming increasingly important in the portable computer market. The QFP part considerably reduces the real estate consumed. The package outline, with the appropriate dimensions is given below:

64-Lead Quad Flatpack Package



290475–28

Description	Symbol	64 QFP Package	
		Nominal (mm)	Tolerance (mm)
Overall Height	A	2.35	±0.20
Stand Off	A1	0.15	±0.10
Lead Width	B	0.30	±0.10
Lead Thickness	C	0.15	±0.05
Terminal	D	15.3	±0.40
Long Side	D1	12.0	±0.10
Terminal	E	15.3	±0.40
Short Side	E1	12.0	±0.10
Lead Spacing	e1	0.65	±0.12
Lead Count	N	64	

13.0 REVISION HISTORY FOR THE 82078 64 PIN

The following list represents the key differences between version 002 and version 003 of the 82078 64 pin data sheet.

Section 5.2.3	Redundant information removed.
Section 5.2.4	Redundant information removed.
Section 8.0	Description of IDENT0 and IDENT1 changed to clarify their function.
Section 11.2	New Vol specification added for status pins.
Table 6-2	Data in table reordered to be consistent.
AC Specifications	V_{CC} has changed for 82078-1 only.