56F827

Data Sheet

Preliminary Technical Data

56F800
16-bit Digital Signal Controllers

DSP56F827
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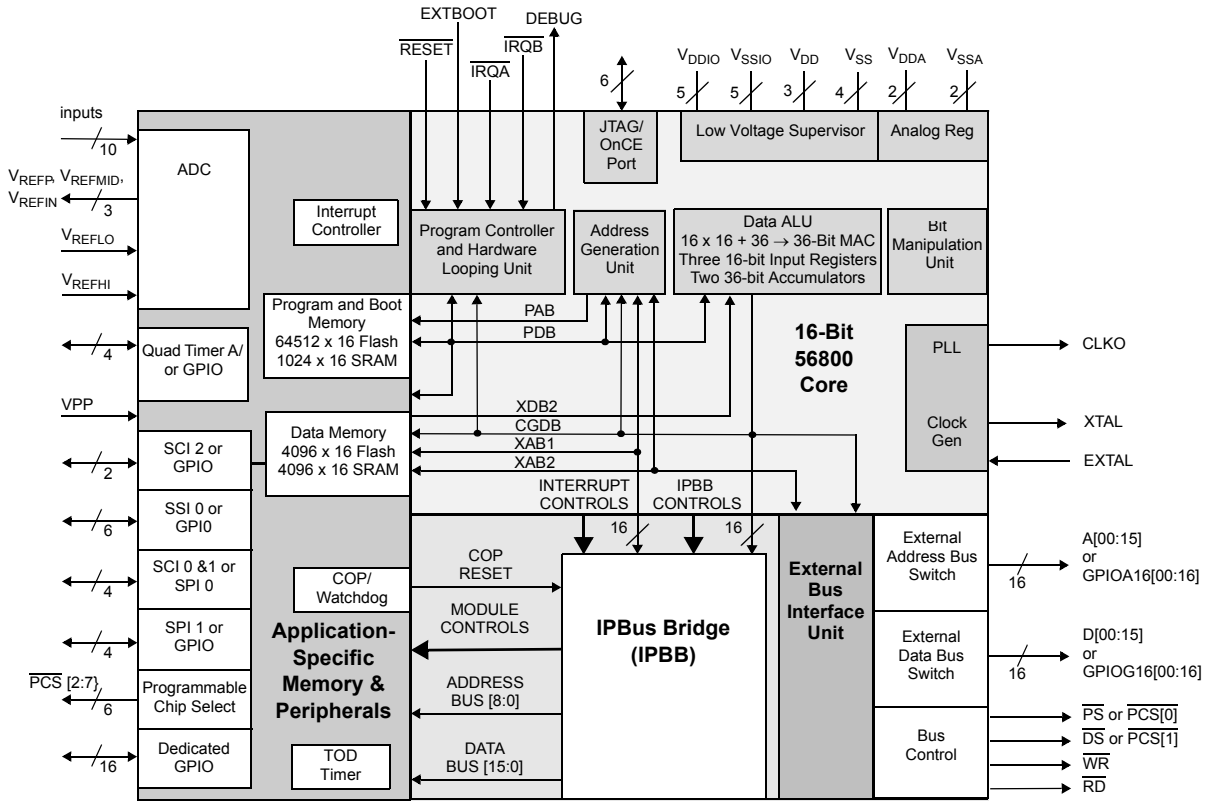
semiconductor

56F827 General Description

- Up to 40 MIPS at 80MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- 64K × 16-bit words (128KB) Program Flash
- 1K × 16-bit words (2KB) Program RAM
- 4K × 16-bit words (8KB) Data Flash
- 4K × 16-bit words (8KB) Data RAM
- Up to 64K × 16-bit words (128KB) external memory expansion each for Program and Data memory
- JTAG/OnCE™ for debugging
- General Purpose Quad Timer
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 8-channel Programmable Chip Select
- 10-channel, 12-bit ADC
- Synchronous Serial Interface (SSI)
- Serial Port Interface (SPI)
- Serial Communications Interface (SCI)
- Time-of-Day (TOD) Timer
- 128-pin LQFP Package
- 16-dedicated and 48 shared GPIO



56F827 Block Diagram

Part 1 Overview

1.1 56F827 Features

1.1.1 Processing Core

- Efficient 16-bit 56800 family processor engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique processor addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE Debug Programming Interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to Program and Data memory
- On-chip memory including a low-cost, high-volume Flash solution
  - 64K words of Program Flash
  - 1K words of Program RAM
  - 4K words of Data RAM
  - 4K words of Data Flash
- Off-chip memory expansion capabilities programmable for 0, 4, 8, or 12 wait states
  - As much as 64 K × 16 Data memory
  - As much as 64 K × 16 Program memory

1.1.3 Peripheral Circuits for 56F827

- One 10 channel, 12-bit, Analog-to-Digital Converter (ADC)
- One General Purpose Quad Timer totaling 4 pins
- One Serial Peripheral Interface with configurable four-pin port multiplexed with two Serial Communications Interfaces totalling 4 pins or 4 GPIO pins
- Three Serial Communication Interfaces with 2 pins each (or 6 additional GPIO pins)
- Two Serial Peripheral Interface with configurable four-pin port (or 4 additional GPIO pins)

- One Synchronous Serial Interface with 6 pins (or 6 additional GPIO pins)
- One 8-channel Programmable Chip Select
- Sixteen dedicated and forty eight multiplexed GPIO pins (64 total)
- Computer-Operating Properly (COP) Watchdog timer
- Two external interrupt pins
- External reset pin for hardware reset
- JTAG/On-Chip Emulation (OnCE™) for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Locked Loop-based frequency synthesizer for the core clock
- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- One Time of Day (TOD) Timer

1.1.4 Power Information

- Dual power supply, 3.3V and 2.5V
- Wait and Multiple Stop modes available

1.2 56F827 Description

The 56F827 is a member of the 56800 core-based family of controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution for general purpose applications. Because of its low cost, configuration flexibility, and compact program code, the 56F827 is well-suited for many applications. The 56F827 includes many peripherals that are especially useful for applications such as: noise suppression, ID tag readers, sonic/subsonic detectors, security access devices, remote metering, sonic alarms, and telephony.

The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C/C++ Compilers to enable rapid development of optimized control applications.

The 56F827 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56F827 also provides two external dedicated interrupt lines, and up to 64 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56F827 controller includes 64K words (16-bit) of Program Flash and 4K words of Data Flash (each programmable through the JTAG port) with 1K words of Program RAM and 4K words of Data RAM. It also supports program execution from external memory. The 56800 core is capable of accessing two data operands from the on-chip Data RAM per instruction cycle.

This controller also provides a full set of standard programmable peripherals that include one 10-input, 12-bit Analog-to-Digital Converters (ADC), one Synchronous Serial Interface (SSI), two Serial Peripheral Interfaces (SPI), three Serial Communications Interfaces (SCI). (Note: The second SPI is multiplexed with

the second and third SCIs, giving the option to select a second SPI or two additional SCIs.) This controller also provides one Programmable Chip Select (PCS), and one Quad Timer. The SCI, SSI, SPI, Quad Timer A, and select address and data lines can be used as General Purpose Input/Outputs (GPIOs) if those functions are not required.

1.3 Award-Winning Development Environment

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 2-1** are required for a complete description and proper design with the 56F827. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **www.freescale.com**.

Table 1-1 56F827 Chip Documentation

Topic	Description	Order Number
56800E Family Manual	Detailed description of the 56800 family architecture, and 16-bit core processor and the instruction set	56800EFM
DSP56F826/F827 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56F826 and 56F827	DSP56F826-827UM
56F827 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F827
56F827 Errata	Details any chip issues that might be present	DSP56F827E

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
“asserted”	A high true (active high) signal is high or a low true (active low) signal is low.
“deasserted”	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

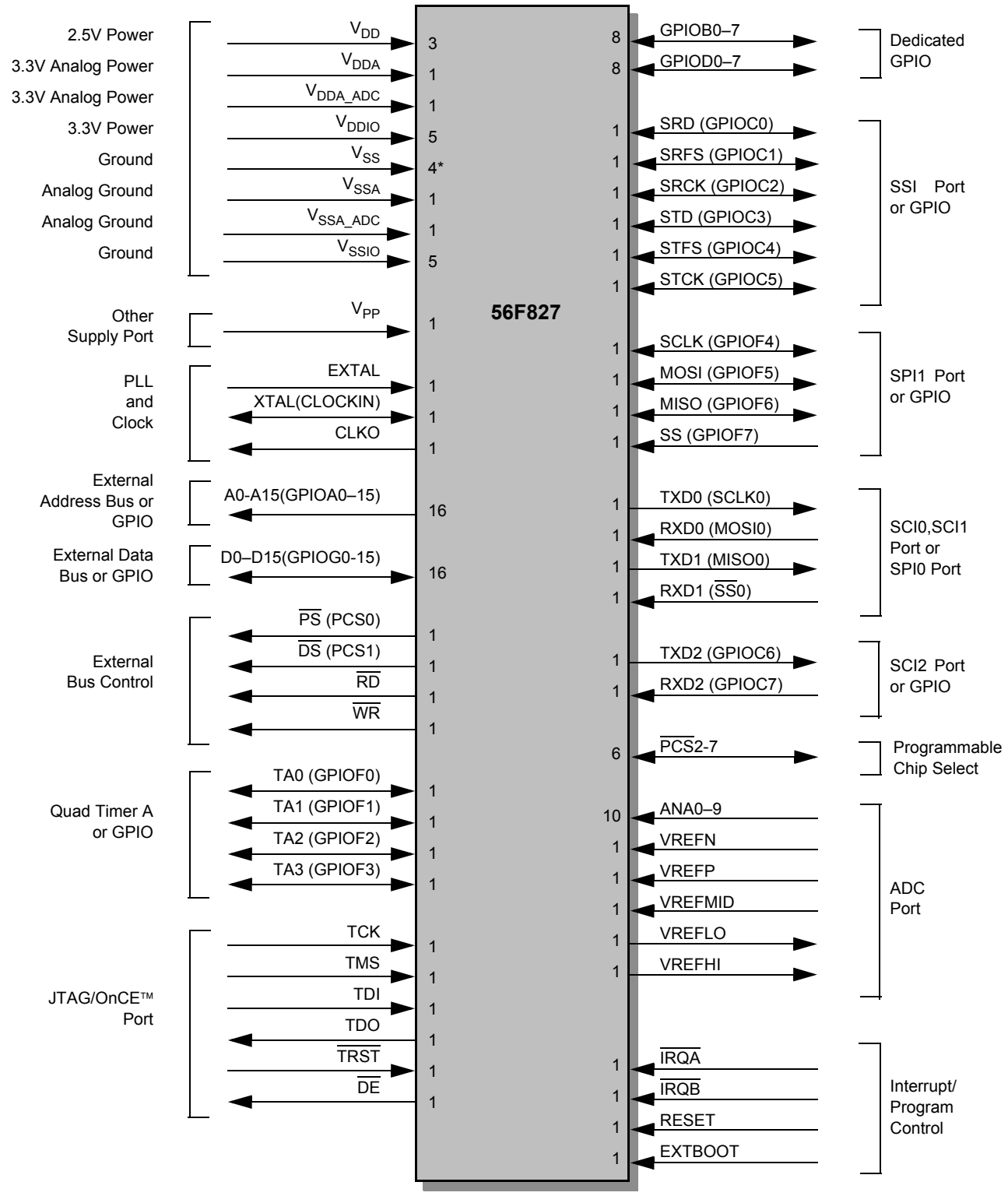
2.1 Introduction

The input and output signals of the 56F827 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. **Table 2-2** describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD}, V_{DDIO}, V_{DDA} or V_{DDA_ADC})	(3,5,1,1)
Ground (V_{SS}, V_{SSIO}, V_{SSA}, or V_{SSA_ADC})	(3,5,1,1)
V_{PP}	1
PLL and Clock	3
Address Bus[1]	16
Data Bus[1]	16
Bus Control	4
Quad Timer Module Ports[1]	4
JTAG/On-Chip Emulation (OnCE)	6
Dedicated General Purpose Input/Output	16
Synchronous Serial Interface (SSI) Port[1]	6
Serial Peripheral Interface (SPI) Port[1]	4
Serial Communications Interface1 (SCI0, SCI1) Port[2]	4
Serial Communications Interface2 (SCI2) Port[1]	2
Analog to Digital Converter (ADC)	15
Programmable Chip Select ($\overline{PCS}$)[3]	6
Interrupt and Program Control	5

1. Alternately, GPIO pins
2. Alternately, SPI pins
3. In addition, 2 Bus Control pins can be programmed as PCS[0-1].



*Includes TCS pin, which is reserved for factory use and is tied to VSS

Figure 2-1 56F827 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

2.2 Signals and Package Information

All inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are always enabled. Exceptions:

1. When a pin is owned by GPIO, then the pull-up may be disabled under software control.
2. TCK has a weak pull-down circuit always active.

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP

Signal Name	Pin No.	Type	Description
V_{DD}	116	V_{DD}	**Power**—These pins provide power to the internal structures of the chip, and are generally connected to a 2.5V supply.
V_{DD}	81	V_{DD}	
V_{DD}	19	V_{DD}	
V_{DDA}	62	V_{DDA}	**Analog Power**—This pin is a dedicated power pin for the analog portion of the chip and should be connected to a low-noise 3.3V supply.
V_{DDA_ADC}	69	V_{DDA}	**Analog Power**—This pin is a dedicated power pin for the analog portion of the ADC module and should be connected to a low-noise 3.3V supply.
V_{DDIO}	113	V_{DDIO}	**Power In/Out**—These pins provide power to the I/O structures of the chip, and are generally connected to a 3.3V supply.
V_{DDIO}	82	V_{DDIO}	
V_{DDIO}	56	V_{DDIO}	
V_{DDIO}	29	V_{DDIO}	
V_{DDIO}	4	V_{DDIO}	
V_{SS}	115	V_{SS}	**GND**—These pins provide grounding for the internal structures of the chip. All should be attached to V_{SS}.
V_{SS}	80	V_{SS}	
V_{SS}	20	V_{SS}	
V_{SSA}	61	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.
V_{SSA_ADC}	63	V_{SSA}	**Analog Ground**—This pin is a dedicated ground pin for the analog portion of the ADC module.
V_{SSIO}	114	V_{SSIO}	**GND In/Out**—These pins provide grounding for the I/O ring on the chip. All should be attached to V_{SS}.
V_{SSIO}	83	V_{SSIO}	
V_{SSIO}	58	V_{SSIO}	
V_{SSIO}	30	V_{SSIO}	
V_{SSIO}	5	V_{SSIO}	
TCS	43	Input/Output (Schmitt)	**TCS**—This pin is reserved for factory use. It must be tied to V_{SS} for normal use. In block diagrams, this pin is considered an additional V_{SS}.

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
V_{PP}	90	Input	**V_{PP}**—This pin should be left unconnected as an open circuit for normal functionality.
EXTAL	59	Input	**External Crystal Oscillator Input**—This input should be connected to a 4MHz external crystal or ceramic resonator. For more information, please refer to **Section 3.6**. This pin can also be connected to an external clock source. For more information, please refer to **Section 3.6.3**.
XTAL (CLOCKIN)	60	Output Input	**Crystal Oscillator Output**—This output connects the internal crystal oscillator output to an external crystal or ceramic resonator. If an external clock source over 4MHz is used, XTAL must be used as the input and EXTAL connected to V_{SS}. For more information, please refer to **Section 3.6.3.** **External Clock Input**—This input should be used when using an external clock or ceramic resonator.
CLKO	57	Output	**Clock Output**—This pin outputs a buffered clock signal. By programming the CLKO Select Register (CLKOSR), the user can select between outputting a version of the signal applied to XTAL and a version of the device master clock at the output of the PLL. The clock frequency on this pin can be disabled by programming the CLKO Select Register (CLKOSR).

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
A0 (GPIOA0)	21	Output Input/Output	**Address Bus**—A0–A15 specify the address for external Program or Data memory accesses. **Port A GPIO**—These 16 General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is Address Bus.
A1 (GPIOA1)	22		
A2 (GPIOA2)	23		
A3 (GPIOA3)	24		
A4 (GPIOA4)	25		
A5 (GPIOA5)	26		
A6 (GPIOA6)	27		
A7 (GPIOA7)	28		
A8 (GPIOA8)	31		
A9 (GPIOA9)	32		
A10 (GPIOA10)	33		
A11 (GPIOA11)	34		
A12 (GPIOA12)	35		
A13 (GPIOA13)	36		
A14 (GPIOA14)	37		
A15 (GPIOA15)	38		

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
D0 (GPIOG0)	125	Input/Output Input/Output	**Data Bus**—D0–D15 specify the data for external Program or Data memory accesses. D0-D15 are tri-stated when the external bus is inactive. **Port G GPIO**—These 16 General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is Address Bus.
D1 (GPIOG1)	126		
D2 (GPIOG2)	127		
D3 (GPIOG3)	128		
D4 (GPIOG4)	1		
D5 (GPIOG5)	2		
D6 (GPIOG6)	3		
D7 (GPIOG7)	6		
D8 (GPIOG8)	7		
D9 (GPIOG9)	8		
D10 (GPIOG10)	9		
D11 (GPIOG11)	10		
D12 (GPIOG12)	11		
D13 (GPIOG13)	12		
D14 (GPIOG14)	13		
D15 (GPIOG15)	14		
$\overline{PS}$ (PCS0)	18	Output	**Program Memory Select**—$\overline{PS}$ is asserted low for external program memory access. This pin can also be programmed as a programmable chip select.
$\overline{DS}$ (PCS1)	17	Output	**Data Memory Select**—$\overline{DS}$ is asserted low for external Data memory access. This pin can also be programmed as a programmable chip select.

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
$\overline{RD}$	15	Output	**Read Enable**—$\overline{RD}$ is asserted during external memory read cycles. When $\overline{RD}$ is asserted low, pins D0–D15 become inputs and an external device is enabled onto the device data bus. When $\overline{RD}$ is deasserted high, the external data is latched inside the device. When $\overline{RD}$ is asserted, it qualifies the A0–A15, $\overline{PS}$, and $\overline{DS}$ pins. $\overline{RD}$ can be connected directly to the $\overline{OE}$ pin of a Static RAM or ROM.
$\overline{WR}$	16	Output	**Write Enable**—$\overline{WR}$ is asserted during external memory write cycles. When $\overline{WR}$ is asserted low, pins D0–D15 become outputs and the device puts data on the bus. When $\overline{WR}$ is deasserted high, the external data is latched inside the external device. When $\overline{WR}$ is asserted, it qualifies the A0–A15, $\overline{PS}$, and $\overline{DS}$ pins. $\overline{WR}$ can be connected directly to the $\overline{WE}$ pin of a Static RAM.
TA0 (GPIOF0)	112	Input/Output Input/Output	**TA0–3**—Timer A Channels 0, 1, 2, and 3 **Port F GPIO**—These four General Purpose I/O (GPIO) pins can be individually programmed as input or output. After reset, the default state is Quad Timer.
TA1 (GPIOF1)	111		
TA2 (GPIOF2)	110		
TA3 (GPIOF3)	109		
TCK	44	Input (Schmitt)	**Test Clock Input**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
TMS	46	Input (Schmitt)	**Test Mode Select Input**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
TDI	48	Input (Schmitt)	**Test Data Input**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDO	47	Input/Output	**Test Data Output**—This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
$\overline{TRST}$	45	Input (Schmitt)	**Test Reset**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{TRST}$ should be asserted whenever $\overline{RESET}$ is asserted. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the JTAG/OnCE module. In this case, assert $\overline{RESET}$, but do not assert $\overline{TRST}$. $\overline{TRST}$ must always be asserted at power-up. **Note:** For normal operation, connect $\overline{TRST}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{TRST}$ may be tied to V_{SS} through a 1K resistor.
$\overline{DE}$	41	Output	**Debug Event**—$\overline{DE}$ provides a low pulse on recognized debug events.

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
GPIOB0	124	Input/Output	**Port B GPIO**—These eight dedicated General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is GPIO input.
GPIOB1	123		
GPIOB2	122		
GPIOB3	121		
GPIOB4	120		
GPIOB5	119		
GPIOB6	118		
GPIOB7	117		
GPIOD0	98	Input/ Output	**Port D GPIO**—These eight dedicated GPIO pins can be individually programmed as an input or output pins. After reset, the default state is GPIO input.
GPIOD1	97		
GPIOD2	96		
GPIOD3	95		
GPIOD4	94		
GPIOD5	93		
GPIOD6	92		
GPIOD7	91		
SRD (GPIOC0)	55	Input/Output Input/Output	**SSI Receive Data (SRD)—**This input pin receives serial data and transfers the data to the SSI Receive Shift Receiver. **Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
SRFS (GPIOC1)	54	Input/Output Input/Output	**SSI Serial Receive Frame Sync (SRFS)**—This bidirectional pin is used by the receive section of the SSI as frame sync I/O or flag I/O. The STFS can be used only by the receiver. It is used to synchronize data transfer and can be an input or an output. **Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
SRCK (GPIOC2)	53	Input/Output Input/Output	**SSI Serial Receive Clock (SRCK)—**This bidirectional pin provides the serial bit rate clock for the Receive section of the SSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode. **Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
STD	52	Output	**SSI Transmit Data (STD)**—This output pin transmits serial data from the SSI Transmitter Shift Register.
(GPIOC3)		Input/Output	**Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
STFS	51	Input	**SSI Serial Transmit Frame Sync (STFS)—**This bidirectional pin is used by the Transmit section of the SSI as frame sync I/O or flag I/O. The STFS can be used by both the transmitter and receiver in synchronous mode. It is used to synchronize data transfer and can be an input or output pin.
(GPIOC4)		Input/Output	**Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
STCK	50	Input/ Output	**SSI Serial Transmit Clock (STCK)**—This bidirectional pin provides the serial bit rate clock for the transmit section of the SSI. The clock signal can be continuous or gated. It can be used by both the transmitter and receiver in synchronous mode.
(GPIOC5)		Input/Output	**Port C GPIO**—This is a General Purpose I/O (GPIO) pin with the capability of being individually programmed as input or output. After reset, the default state is GPIO input.
SCLK	102	Input/Output	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
(GPIOF4)		Input/Output	**Port F GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is SCLK.
MOSI	101	Input/Output	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
(GPIOF5)		Input/Output	**Port F GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output.
MISO	100	Input/Output	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(GPIOF6)		Input/Output	**Port F GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is MISO.

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
$\overline{SS}$	99	Input/Output	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave.
(GPIOF7)		Input/Output	**Port F GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is $\overline{SS}$.
TXD0	108	Output	**Transmit Data (TXD0)**—transmit data output
(SCLK0)		Input/Output	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. After reset, the default state is SCI output.
RXD0	107	Input	**Receive Data (RXD0)**—receive data input
(MOSI0)		Input/Output	**SPI Master Out/Slave In**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
TXD1	106	Output	**Transmit Data (TXD1)**—transmit data output
(MISO0)		Input/Output	**SPI Master In/Slave Out**—This serial data pin is an output to a master device and an input from a slave device. The master device places data on the MOSI line one half-cycle before the clock edge the slave device uses to latch the data. After reset, the default state is SCI input.
RXD1	105	Input (Schmitt)	**Receive Data (RXD1)**— receive data input
($\overline{SS}$0)		Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave. After reset, the default state is SCI input.
TXD2	104	Output	**Transmit Data (TXD2)**—transmit data output
(GPIOC6)		Input/Output	**Port C GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is GPIO output.
RXD2	103	Input/Output	**Receive Data (RXD2)**— receive data input
(GPIOC7)		Input/Output	**Port C GPIO**—This General Purpose I/O (GPIO) pin can be individually programmed as input or output. After reset, the default state is GPIO input.

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
$\overline{\text{PCS}}$2	84	Input/Output	**Programmable Chip Select** - $\overline{\text{PCS}}$ 2-7 is asserted low for external peripheral chip select.
$\overline{\text{PCS}}$3	85	Input/Output	
$\overline{\text{PCS}}$4	86	Input/Output	
$\overline{\text{PCS}}$5	87	Input/Output	
$\overline{\text{PCS}}$6	88	Input/Output	
$\overline{\text{PCS}}$7	89	Input/Output	
ANA0	70	Input	**ANA0–9**—Analog inputs to ADC
ANA1	71	Input	
ANA2	72	Input	
ANA3	73	Input	
ANA4	74	Input	
ANA5	75	Input	
ANA6	76	Input	
ANA7	77	Input	
ANA8	78	Input	
ANA9	79	Input	
V_{REFN}	66	Input	**ADC Reference**—This pin is connected to the negative side of the ADC input range. This pin requires a 0.1μF ceramic capacitor to V_{SSA} and a start-up time of 25ms, prior to beginning conversions.
V_{REFP}	65	Input	**ADC Reference**—This pin is connected to the positive side of the ADC input range. This pin requires a 0.1μF ceramic capacitor to V_{SSA} and a start-up time of 25ms, prior to beginning conversions.
V_{REFMID}	68	Input	**ADC Reference**—This pin isconnected to the center of the ADC input range. This pin requires a 0.1μF ceramic capacitor to V_{SSA} and a start-up time of 25ms, prior to beginning conversions.
V_{REFLO}	64	Input	**ADC Reference**—These pins are Negative Reference for ADC and are generally connected to a V_{SSA}.
V_{REFHI}	67	Input	**ADC Reference**—These pins are Positive Reference for ADC and are generally connected to a 3.3V Analog (V_{DDA_ADC}) supply.
$\overline{\text{IRQA}}$	40	Input (Schmitt)	**External Interrupt Request A**—The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull-up resistor is required for wired-OR operation. If the processor is in the Stop state and $\overline{\text{IRQA}}$ is asserted, the processor will exit the Stop state.

Table 2-2 56F827 Signal and Package Information for the 128 Pin LQFP (Continued)

Signal Name	Pin No.	Type	Description
$\overline{\text{IRQB}}$	49	Input (Schmitt)	**External Interrupt Request B**—The $\overline{\text{IRQB}}$ input is an external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull-up resistor is required for wired-OR operation.
$\overline{\text{RESET}}$	42	Input (Schmitt)	**Reset**—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the external boot pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
EXTBOOT	39	Input (Schmitt)	**External Boot**—This input is tied to V_{DD} to force device to boot from off-chip memory. Otherwise, it is tied to V_{SS}.

Part 3 Specifications

3.1 General Characteristics

The 56F827 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term "5V-tolerant" refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels. A standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage. This 5V-tolerant capability, therefore, offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 3-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The 56F827 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 3-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	V_{DD}[1]	V_{SS} - 0.3	V_{SS} + 3.0	V
Supply voltage, IO Supply voltage, Analog Supply voltage, ADC	V_{DDIO}[2] V_{DDA}[2] V_{DDA_ADC}	V_{SSIO} - 0.3 V_{SSA} - 0.3 V_{SSA_ADC}-0.3	V_{SSIO} + 4.0 V_{SSA} + 4.0 V_{SSA_ADC}+0.3	V
Digital input voltages Analog input voltages (XTAL, EXTAL) Analog input voltages (ANA0-7, VREF)	V_{IN} V_{INA} V_{IN_ADC}	V_{SSIO} - 0.3 V_{SSA} - 0.3 V_{SSA_ADC}-0.3	V_{SSIO} + 5.5 V_{DDA} + 0.3 V_{SSA_ADC}+0.3	V
Voltage difference V_{DD} to V_{DD_IO}, V_{DDA}	ΔV_{DD}	- 0.3	0.3	V
Voltage difference V_{SS} to V_{SS_IO}, V_{SSA}	ΔV_{SS}	- 0.3	0.3	V
Current drain per pin excluding V_{DD}, V_{SS}, V_{DDA}, V_{SSA}, V_{DDIO}, V_{SSIO}	I	—	10	mA
Junction temperature	T_J	—	150	°C
Storage temperature range	T_{STG}	-55	150	°C

1. V_{DD} must not exceed V_{DDIO}
2. V_{DDIO} and V_{DDA} must not differ by more that 0.5V

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage, core	V_{DD}	2.5	2.5	2.75	V
Supply Voltage, IO and analog	V_{DDIO}, V_{DDA}	3.0	3.3	3.6	V
Voltage difference V_{DD} to V_{DD_IO}, V_{DDA}	ΔV_{DD}	-0.1	-	0.1	V
Voltage difference V_{SS} to V_{SS_IO}, V_{SSA}	ΔV_{SS}	-0.1	-	0.1	V
ADC reference voltage, positive	V_{REFHI}	2.7	—	V_{DD_ADC}	V
ADC reference voltage, negative	V_{REFLO}	V_{SSA}	—	V_{REFHI}	V
Ambient operating temperature	T_A	–40	—	85	°C

Table 3-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			128-pin LQFP		
Junction to ambient Natural convection		$R_{\theta JA}$	50.8	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	46.5	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	43.9	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	41.7	°C/W	1,2
Junction to case		$R_{\theta JC}$	13.9	°C/W	3
Junction to center of case		Ψ_{JT}	1.2	°C/W	4
I/O pin power dissipation		$P_{I/O}$	User Determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Junction to center of case		P_{DMAX}	(TJ - TA) /RθJA	W	7

Notes:

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$) was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p where s is the number of signal layers and p is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the "case" temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.
4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the "resistance" from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See Section 5.1 from more details on thermal design considerations.
7. TJ = Junction Temperature
   TA = Ambient Temperature

3.2 DC Electrical Characteristics

Table 3-4 DC Electrical Characteristics

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, $C_L \leq 50$pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	—	3.6	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	0	—	0.5	V
Input high voltage (Schmitt trigger inputs)[1]	V_{IHS}	2.2	—	5.5	V
Input low voltage (Schmitt trigger inputs)[2]	V_{ILS}	-0.3	—	0.8	V
Input high voltage (all other digital inputs)	V_{IH}	2.0	—	5.5	V
Input low voltage (all other digital inputs)	V_{IL}	-0.3	—	0.8	V
Input current high (pull-up/pull-down resistors disabled, V_{IN}=V_{DD})	I_{IH}	-1	—	1	μA
Input current low (pull-up/pull-down resistors disabled, V_{IN}=V_{SS})	I_{IL}	-1	—	1	μA
Input current high (with pull-up resistor, V_{IN}=V_{DD})	I_{IHPU}	-0	—	1	μA
Input current low (with pull-up resistor, V_{IN}=V_{SS})	I_{ILPU}	-210	—	-50	μA
Input current high (with pull-down resistor, V_{IN}=V_{DD})	I_{IHPD}	20	—	180	μA
Input current low (with pull-down resistor, V_{IN}=V_{SS})	I_{ILPD}	-1	—	1	μA
Nominal pull-up or pull-down resistor value	R_{PU}, R_{PD}		30		KΩ
Output tri-state current low	I_{OZL}	-10	—	10	μA
Output tri-state current high	I_{OZH}	-10	—	10	μA
Input current high (analog inputs, V_{IN}=V_{DDA})[2]	I_{IHA}	-15	—	15	μA
Input current low (analog inputs, V_{IN}=V_{SSA})[2]	I_{ILA}	-15	—	15	μA
Output High Voltage (at I_{OH})	V_{OH}	V_{DD} – 0.7	—	—	V
Output Low Voltage (at I_{OL})	V_{OL}	—	—	0.4	V
Output source current	I_{OH}	4	—	—	mA
Output sink current	I_{OL}	4	—	—	mA
PWM pin output source current[3]	I_{OHP}	10	—	—	mA

Table 3-4 DC Electrical Characteristics (Continued)

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, C_L ≤ 50pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Typ	Max	Unit
PWM pin output sink current[4]	I_{OLP}	16	—	—	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current	I_{DDT}[5]				
Run [6]		—	60	90	mA
Wait[7]		—	35	50	mA
Stop		—	6	15	mA
Low Voltage Interrupt, V_{DDIO} power supply[8]	V_{EIO}	2.4	2.7	3.0	V
Low Voltage Interrupt, V_{DD} power supply[9]	V_{EIC}	2.0	2.2	2.4	V
Power-on Reset[10]	V_{POR}	—	1.7	2.0	V

1. Schmitt Trigger inputs are: EXTBOOT, $\overline{IRQA}$, $\overline{IRQB}$, $\overline{RESET}$, TCS, TCK, $\overline{TRST}$, TMS, TDI, and RXD1.
2. Analog inputs are: ANA[0:7], XTAL and EXTAL. Specification assumes ADC is not sampling.
3. PWM pin output source current measured with 50% duty cycle.
4. PWM pin output sink current measured with 50% duty cycle.
5. I_{DDT} = I_{DD} + I_{DDA} (Total supply current for V_{DD} + V_{DDA})
6. Run (operating) I_{DD} measured using 4MHz clock source. All inputs 0.2V from rail; outputs unloaded. All ports configured as inputs; measured with all modules enabled.
7. Wait I_{DD} measured using external square wave clock source (f_{osc} = 4MHz) into XTAL; all inputs 0.2V from rail; no DC loads; less than 50pF on all outputs. C_L = 20pF on EXTAL; all ports configured as inputs; EXTAL capacitance linearly affects wait I_{DD}; measured with PLL enabled.
8. This low-voltage interrupt monitors the V_{DDIO} power supply. If V_{DDIO} drops below V_{EIO}, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when $V_{DDIO} \geq V_{EIO}$ (between the minimum specified V_{DDIO} and the point when the V_{EIO} interrupt is generated).
9. This low-voltage interrupt monitors the V_{DD} power supply. If V_{DDIO} drops below V_{EIC}, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when $V_{DD} \geq V_{EIC}$ (between the minimum specified V_{DD} and the point when the V_{EIC} interrupt is generated).
10. Power–on reset occurs whenever the V_{DD} power supply drops below V_{POR}. While power is ramping up, this signal remains active as long as V_{DD} is below V_{POR}, no matter how long the ramp-up rate is.

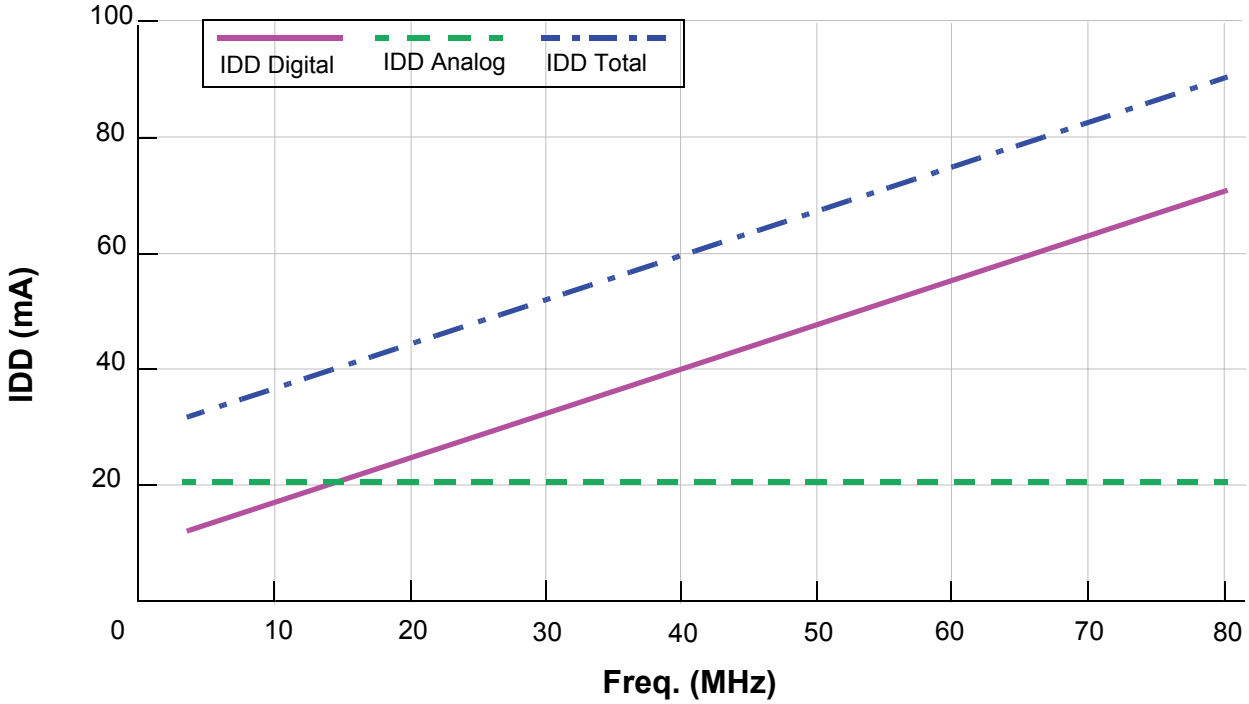
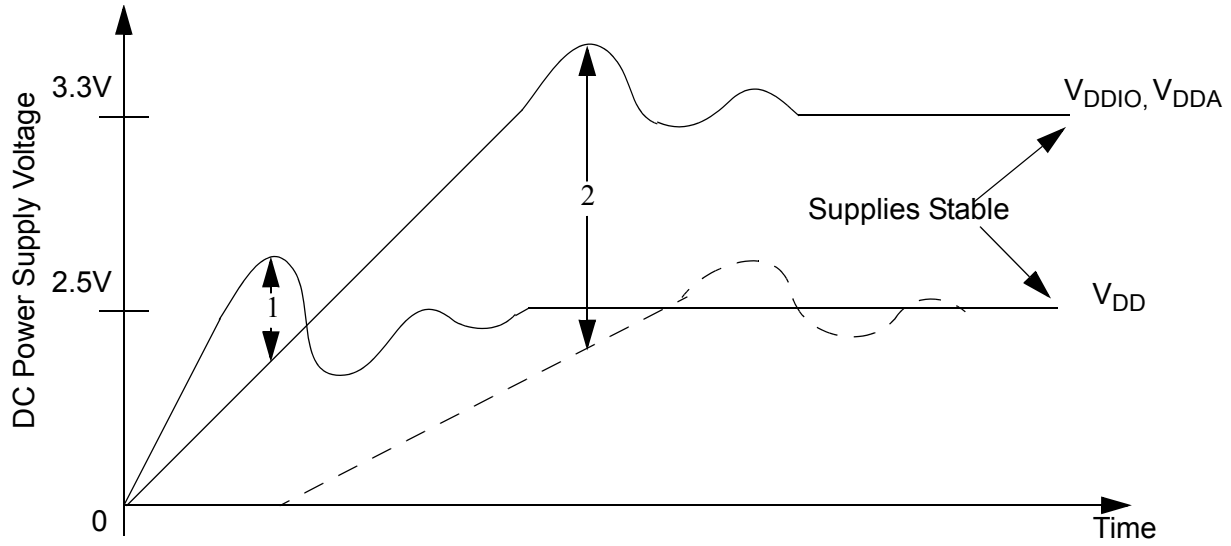


Figure 3-1 Maximum Run I_{DD} vs. Frequency (see Note 6. in Table 3-4)

3.3 Supply Voltage Sequencing and Separation Cautions

Figure 3-2 shows two situations to avoid in sequencing the V_{DD} and $V_{DDIO,}$ V_{DDA} supplies.



Notes: 1. V_{DD} rising before V_{DDIO}, V_{DDA}
2. V_{DDIO}, V_{DDA} rising much faster than V_{DD}

Figure 3-2 Supply Voltage Sequencing and Separation Cautions

V_{DD} should not be allowed to rise early (1). This is usually avoided by running the regulator for the V_{DD} supply (2.5V) from the voltage generated by the 3.3V V_{DDIO} supply, see **Figure 3-3**. This keeps V_{DD} from rising faster than V_{DDIO}.

V_{DD} should not rise so late that a large voltage difference is allowed between the two supplies (2). Typically, this situation is avoided by using external discrete diodes in series between supplies, as shown in **Figure 3-3**. The series diodes forward bias when the difference between V_{DDIO} and V_{DD} reaches approximately 1.4, causing V_{DD} to rise as V_{DDIO} ramps up. When the V_{DD} regulator begins proper operation, the difference between supplies will typically be 0.8V and conduction through the diode chain reduces to essentially leakage current. During supply sequencing, the following general relationship should be adhered to:
$V_{DDIO} \geq V_{DD} \geq (V_{DDIO} - 1.4V)$

In practice, V_{DDA} is typically connected directly to V_{DDIO} with some filtering.

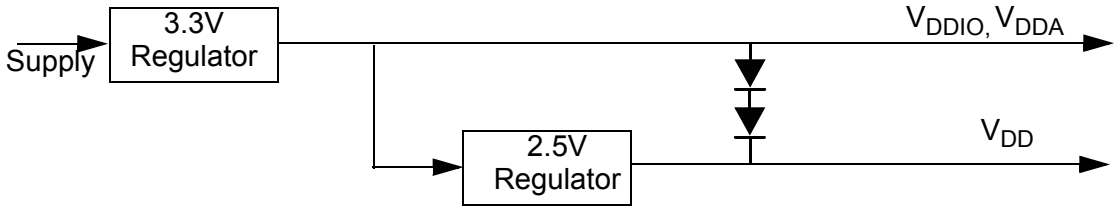
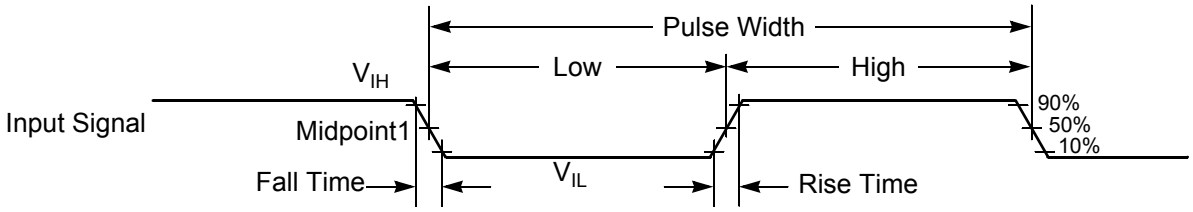


Figure 3-3 Example Circuit to Control Supply Sequencing

3.4 AC Electrical Characteristics

Timing waveforms in **Section 3.4** are tested using the V_{IL} and V_{IH} levels specified in the DC Characteristics table. In **Figure 3-4** the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 3-4 Input Signal Measurement References

Figure 3-5 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

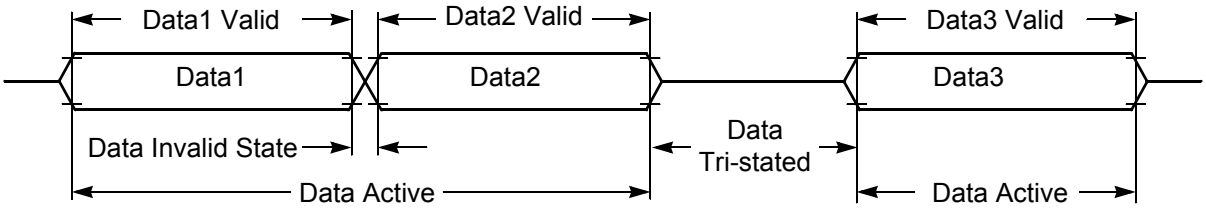


Figure 3-5 Signal States

3.5 Flash Memory Characteristics

Table 3-5 Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE = 0
2. Y address enable, YMUX is disabled when YE = 0
3. Sense amplifier enable
4. Output enable, tri-state Flash data out bus when OE = 0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 3-6 IFREN Truth Table

Mode	IFREN = 1	IFREN = 0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both block	Erase main memory block

Table 3-7 Flash Timing Parameters

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF

Characteristic	Symbol	Min	Typ	Max	Unit	Figure
Program time	T_{prog}*	20	–	–	us	Figure 3-6
Erase time	T_{erase}*	20	–	–	ms	Figure 3-7
Mass erase time	T_{me}*	100	–	–	ms	Figure 3-8
Endurance[1]	E_{CYC}	10,000	20,000	–	cycles	
Data Retention[1]	D_{RET}	10	30	–	years	
The following parameters should only be used in the Manual Word Programming Mode						
PROG/ERASE to NVSTR set up time	T_{nvs}*	–	5	–	us	Figure 3-6, Figure 3-7, Figure 3-8
NVSTR hold time	T_{nvh}*	–	5	–	us	Figure 3-6, Figure 3-7
NVSTR hold time (mass erase)	T_{nvh1}*	–	100	–	us	Figure 3-8
NVSTR to program set up time	T_{pgs}*	–	10	–	us	Figure 3-6,
Recovery time	T_{rcv}*	–	1	–	us	Figure 3-6, Figure 3-7,Figure 3-8
Cumulative program HV period[2]	T_{hv}	–	3	–	ms	Figure 3-6,
Program hold time[3]	T_{pgh}	–	–	–		Figure 3-6,
Address/data set up time[3]	T_{ads}	–	–	–		Figure 3-6,
Address/data hold time[3]	T_{adh}	–	–	–		Figure 3-6,

1. One cycle is equal to an erase program and read.
2. Thv is the cumulative high voltage programming time to the same row before next erase. The same address cannot be programmed twice before next erase.
3. Parameters are guaranteed by design in smart programming mode and must be one cycle or greater.

*The Flash interface unit provides registers for the control of these parameters.

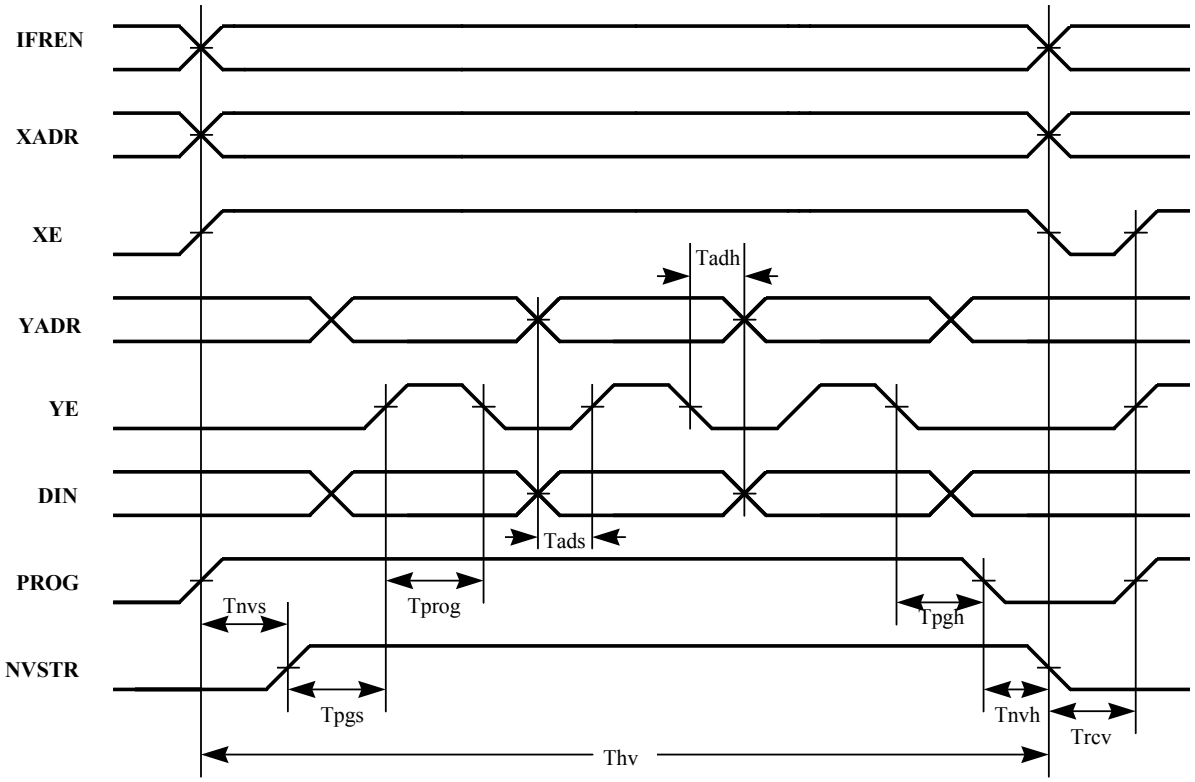


Figure 3-6 Flash Program Cycle

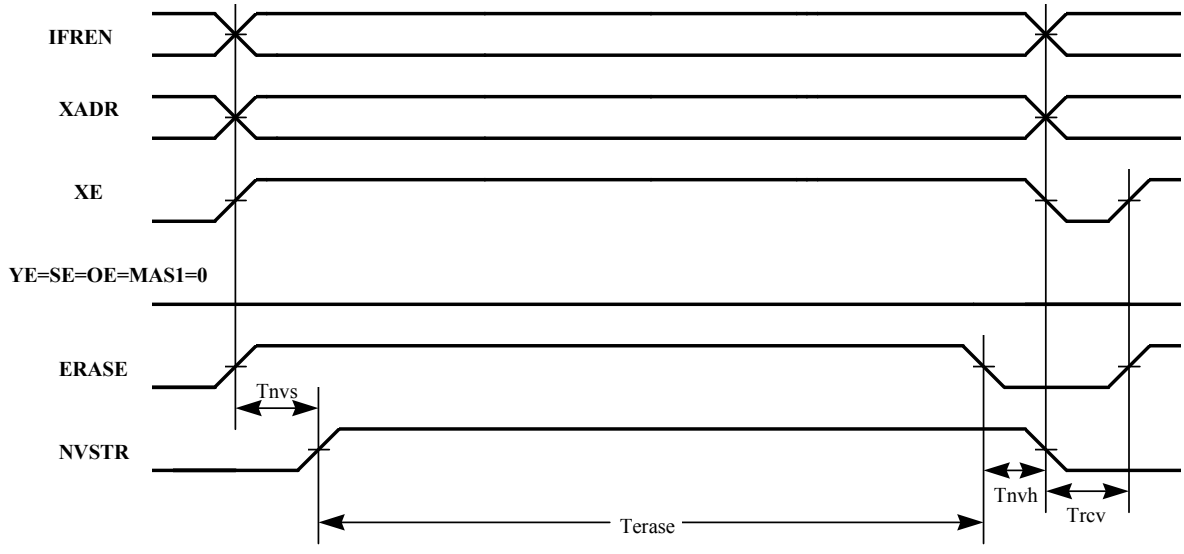


Figure 3-7 Flash Erase Cycle

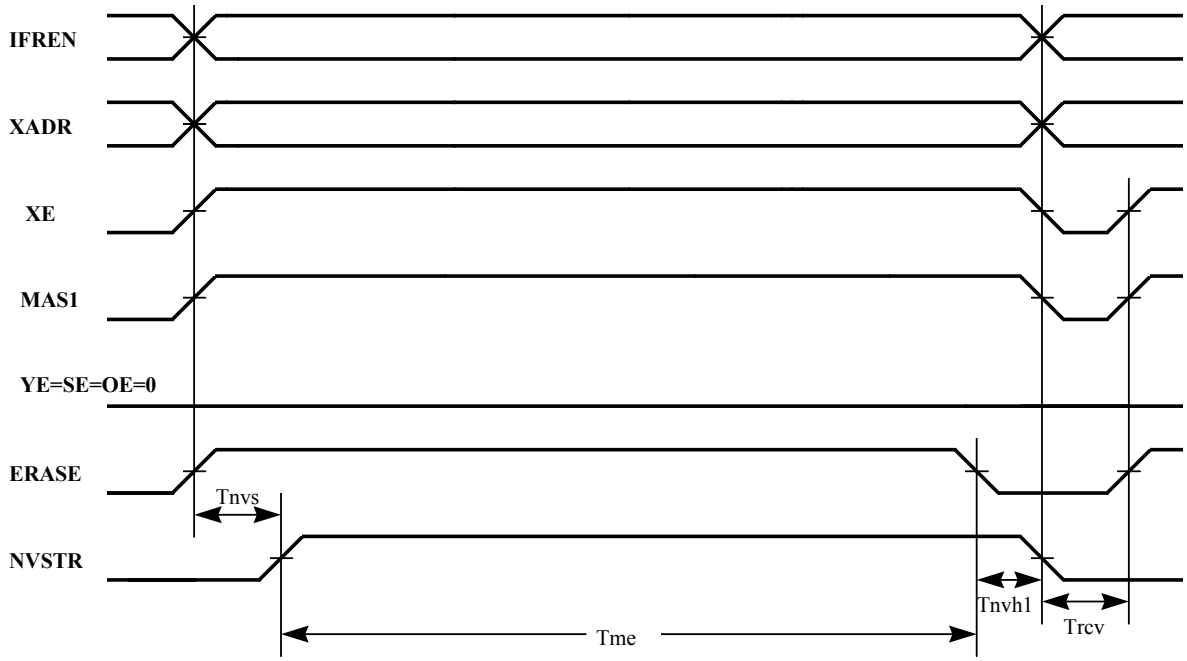


Figure 3-8 Flash Mass Erase Cycle

3.6 External Clock Operation

The 56F827 system clock can be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

3.6.1 Crystal Oscillator

The internal oscillator is also designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 3-8.** A recommended crystal oscillator circuit is shown in **Figure 3-9.** Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.The internal 56F82x oscillator circuitry is designed to have no external load capacitors present. As shown in **Figure 3-9,** no external load capacitors should be used.

The 56F80x components internally are modeled as a parallel resonant oscillator circuit to provide a capacitive load on each of the oscillator pins (XTAL and EXTAL) of 10pF to 13pF over temperature and process variations. Using a typical value of internal capacitance on these pins of 12pF and a value of 3pF

as a typical circuit board trace capacitance the parallel load capacitance presented to the crystal is 9pF as determined by the following equation:

$$CL = \frac{CL1 * CL2}{CL1 + CL2} + Cs = \frac{12 * 12}{12 + 12} + 3 = 6 + 3 = 9pF$$

This is the value load capacitance that should be used when selecting a crystal and determining the actual frequency of operation of the crystal oscillator circuit.

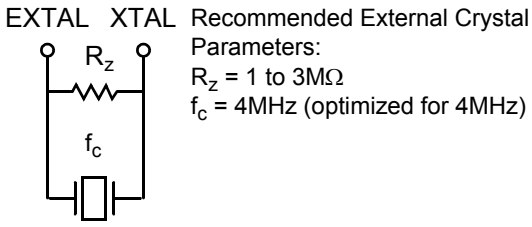


Figure 3-9 Connecting to a Crystal Oscillator Circuit

3.6.2 Ceramic Resonator

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. A typical ceramic resonator circuit is shown in **Figure 3-10**. The resonator and components should be mounted as close as possible to the EXTAL and XTAL pins. The internal 56F82x oscillator circuitry is designed to have no external load capacitors present. As shown in **Figure 3-9**, no external load capacitors should be used.

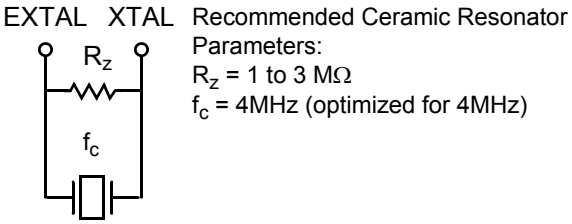


Figure 3-10 Connecting a Ceramic Resonator

Note: Freescale recommends only two terminal ceramic resonators vs. three terminal resonators (which contain an internal bypass capacitor to ground).

3.6.3 External Clock Source

The recommended method of connecting an external clock is given in **Figure 3-11**. The external clock source is connected to XTAL and the EXTAL pin is held $V_{DDA}/2$.

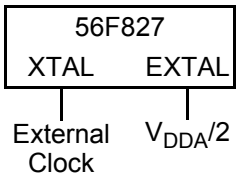


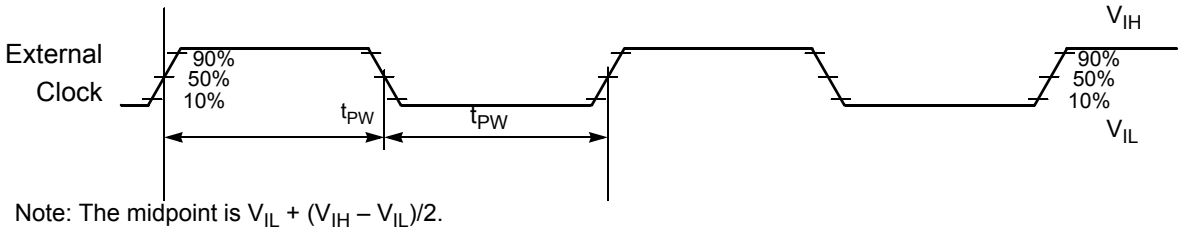
Figure 3-11 Connecting an External Clock Signal

Table 3-8 External Clock Operation Timing Requirements

Operating Conditions: $V_{SSIO}=V_{SS}=V_{SSA}=0V$, $V_{DDA}=V_{DDIO}=3.0–3.6V$, $V_{DD}=2.25–2.75V$, $T_A=–40°$ to $+85°C$, $C_L \le 50pF$, $f_{op}=80MHz$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	4	80[2]	MHz
Clock Pulse Width[3, 4]	t_{PW}	6.25	—	—	ns

1. See **Figure 3-11** for details on using the recommended connection of an external clock driver.
2. When using Time-of-Day (TOD), maximum external frequency is 6MHz.
3. The high or low pulse width must be no smaller than 6.25ns or the chip will not function.
4. Parameters listed are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 3-12 External Clock Timing

3.6.4 Phase Locked Loop Timing

Table 3-9 PLL Timing

Operating Conditions: $V_{SSIO}=V_{SS}=V_{SSA}=0V$, $V_{DDA}=V_{DDIO}=3.0–3.6V$, $V_{DD}=2.25–2.75V$, $T_A=–40°$ to $+85°C$, $C_L \le 50pF$, $f_{op}=80MHz$

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	2	4	6	MHz
PLL output frequency[2]	$f_{out}/2$	40	—	110	MHz
PLL stabilization time [3]-40° to +85°C	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 4MHz input crystal.
2. ZCLK may not exceed 80MHz. For additional information on ZCLK and $f_{out}/2$, please refer to the OCCS chapter in the User Manual. ZCLK = f_{op}
3. This is the minimum time required after the PLL set-up is changed to ensure reliable operation.

3.7 External Bus Asynchronous Timing

Table 3-10 External Bus Asynchronous Timing[1, 2]

Operating Conditions: $V_{SSIO}=V_{SS}=V_{SSA}=0V$, $V_{DDA}=V_{DDIO}=3.0–3.6V$, $V_{DD}=2.25–2.75V$, $T_A=–40°$ to $+85°C$, $C_L \le 50pF$, $f_{op}=80MHz$

Characteristic	Symbol	Min	Max	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	6.5	—	ns
$\overline{WR}$ Width Asserted Wait states = 0 Wait states > 0	t_{WR}	 7.5 (T*WS) + 7.5	 — —	 ns ns
$\overline{WR}$ Asserted to D0–D15 Out Valid	t_{WRD}	—	T + 4.2	ns
Data Out Hold Time from $\overline{WR}$ Deasserted	t_{DOH}	4.8	—	ns
Data Out Set Up Time to $\overline{WR}$ Deasserted Wait states = 0 Wait states > 0	t_{DOS}	 2.2 (T*WS) + 6.4	 — —	 ns ns
$\overline{RD}$ Deasserted to Address Not Valid	t_{RDA}	0	—	ns
Address Valid to $\overline{RD}$ Deasserted Wait states = 0 Wait states > 0	t_{ARDD}	 18.7 (T*WS) + 18.7	—	 ns ns

Table 3-10 External Bus Asynchronous Timing[1, 2] (Continued)

Operating Conditions: $V_{SSIO}=V_{SS} = V_{SSA} = 0V$, $V_{DDA} =V_{DDIO}=3.0–3.6V$, $V_{DD} = 2.25–2.75V$, $T_A = –40°$ to $+85°C$, $C_L \leq 50pF$, $f_{op} = 80MHz$

Characteristic	Symbol	Min	Max	Unit
Input Data Hold to $\overline{RD}$ Deasserted	t_{DRD}	0	—	ns
$\overline{RD}$ Assertion Width Wait states = 0 Wait states > 0	t_{RD}	 19 (T*WS) + 19	 — —	 ns ns
Address Valid to Output Data Valid Wait states = 0 Wait states > 0	t_{AD}	 — —	 1 (T*WS) + 1	 ns ns
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}	-4.4	—	ns
$\overline{RD}$ Asserted to Input Data Valid Wait states = 0 Wait states > 0	t_{RDD}	 — —	 2.4 (T*WS) + 2.4	 ns ns
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}	6.8	—	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}	0	—	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	14.1	—	ns
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}	12.8	—	ns

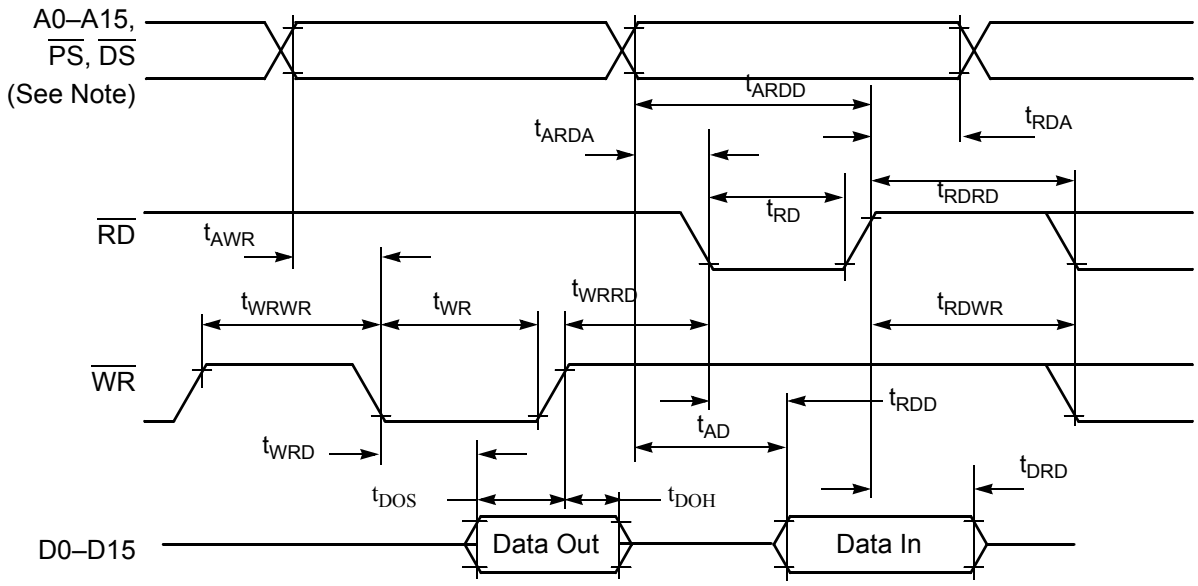
1. Timing is both wait state and frequency dependent. In the formulas listed, WS = the number of wait states and T = Clock Period. For 80MHz operation, T = 12.5ns.
2. Parameters listed are guaranteed by design.

To calculate the required access time for an external memory for any frequency < 80MHz, use this formula:

Top = Clock period @ desired operating frequency

WS = Number of wait states

Memory Access Time = (Top*WS) + (Top- 11.5)



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 3-13 External Bus Asynchronous Timing

3.8 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 3-11 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 5]

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, C_L ≤ 50pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	21	ns	Figure 3-14
Minimum $\overline{\text{RESET}}$ Assertion Duration[2] OMR Bit 6 = 0 OMR Bit 6 = 1	t_{RA}	 275,000T 128T	 — —	 ns ns	Figure 3-14
$\overline{\text{RESET}}$ Deassertion to First External Address Output	t_{RDA}	33T	34T	ns	Figure 3-14
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	Figure 3-15
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	15T	—	ns	Figure 3-16
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	16T	—	ns	Figure 3-16
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[3]	t_{IRI}	13T	—	ns	Figure 3-17
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[4]	t_{IW}	2T	—	ns	Figure 3-18
Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IF}	 — —	 275,000T 12T	 ns ns	Figure 3-18
Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Cause the Fetch of First $\overline{\text{IRQA}}$ Interrupt Instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IRQ}	 — —	 275,000T 12T	 ns ns	Figure 3-19
Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to First Interrupt Vector Address Out Valid (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{II}	 — —	 275,000T 12T	 ns ns	Figure 3-19

1. In the formulas, T = clock cycle. For an operating frequency of 80MHz, T = 12.5ns.
2. Circuit stabilization delay is required during reset when using an external clock or crystal oscillator in two cases:
   • After power-on reset
   • When recovering from Stop state
3. The minimum is specified for the duration of an edge-sensitive $\overline{\text{IRQA}}$ interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
4. The interrupt instruction fetch is visible on the pins only in Mode 3.
5. Parameters listed are guaranteed by design.

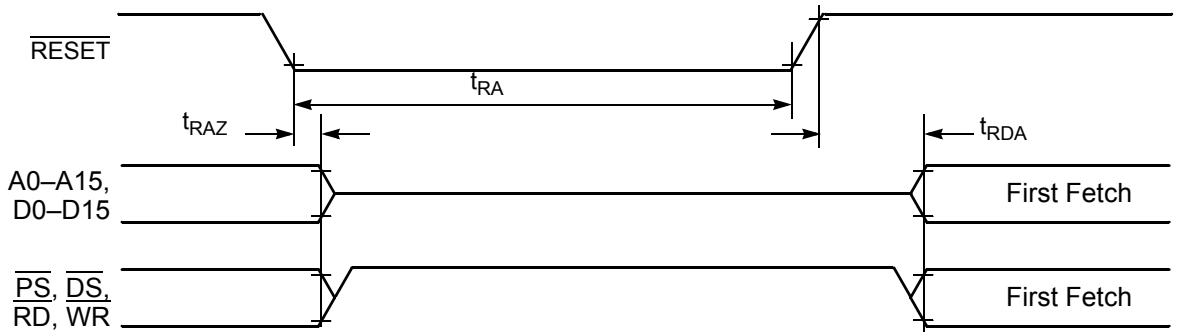


Figure 3-14 Asynchronous Reset Timing

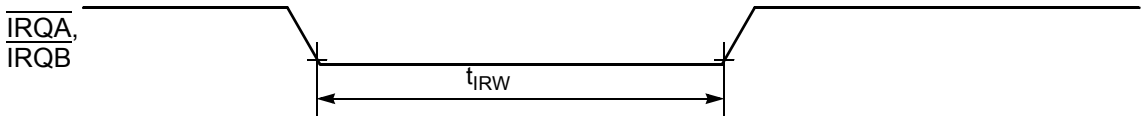
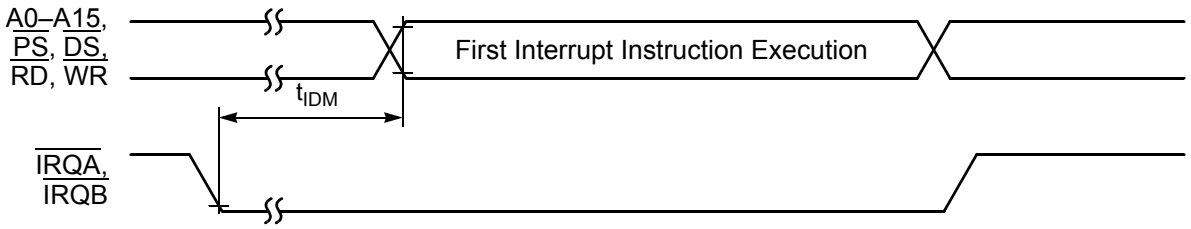
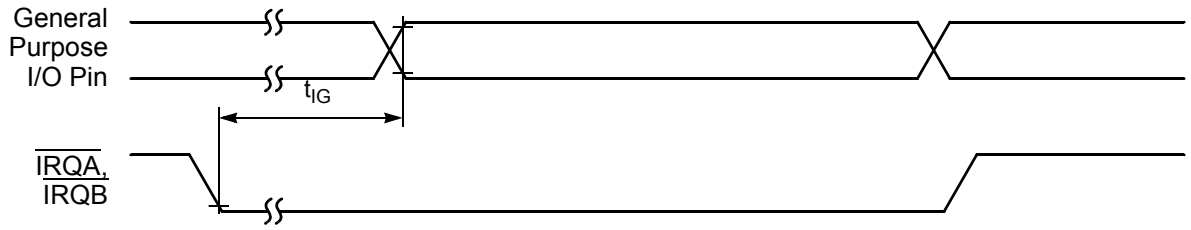


Figure 3-15 External Interrupt Timing (Negative-Edge-Sensitive)



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 3-16 External Level-Sensitive Interrupt Timing

Figure 3-17 Interrupt from Wait State Timing

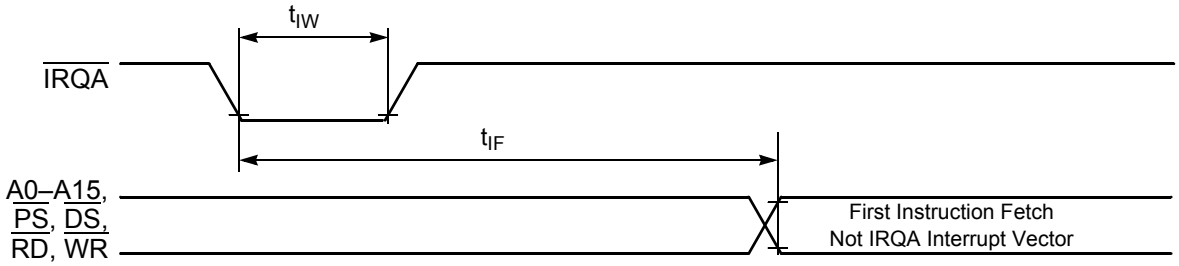


Figure 3-18 Recovery from Stop State Using Asynchronous Interrupt Timing

Figure 3-19 Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

3.9 Serial Peripheral Interface (SPI) Timing

Table 3-12 SPI Timing[1]

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, C_L ≤ 50pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 25	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure 3-23
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure 3-23
Clock (SCLK) high time Master Slave	t_{CH}	 24 12	 — —	ns ns	Figures 3-20, 3-21, 3-22, 3-23
Clock (SCLK) low time Master Slave	t_{CL}	 24.1 12	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Access time (time to data active from high-impedance state) Slave	t_A	 4.8	 15	 ns	Figure 3-23
Disable time (hold time to high-impedance state) Slave	t_D	 3.7	 15.2	 ns	Figure 3-23
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures 3-20, 3-21, 3-22, 3-23
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures 3-20, 3-21, 3-22, 3-23

1. Parameters listed are guaranteed by design.

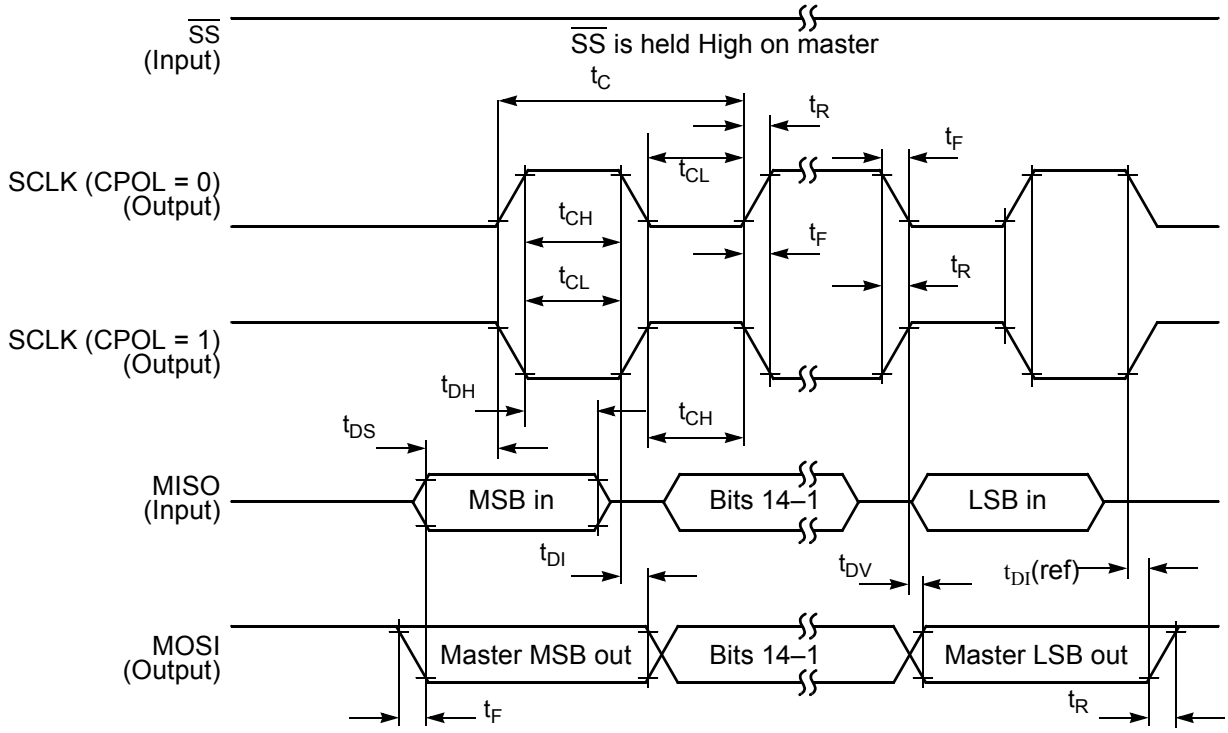


Figure 3-20 SPI Master Timing (CPHA = 0)

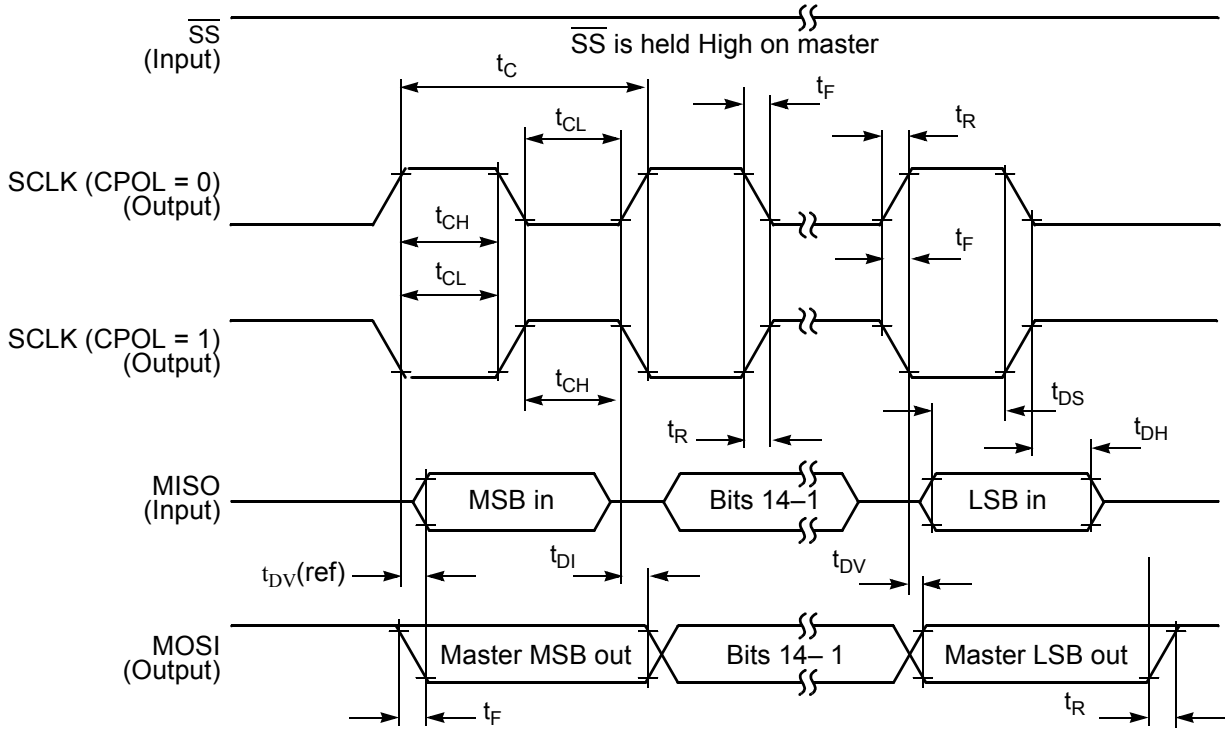


Figure 3-21 SPI Master Timing (CPHA = 1)

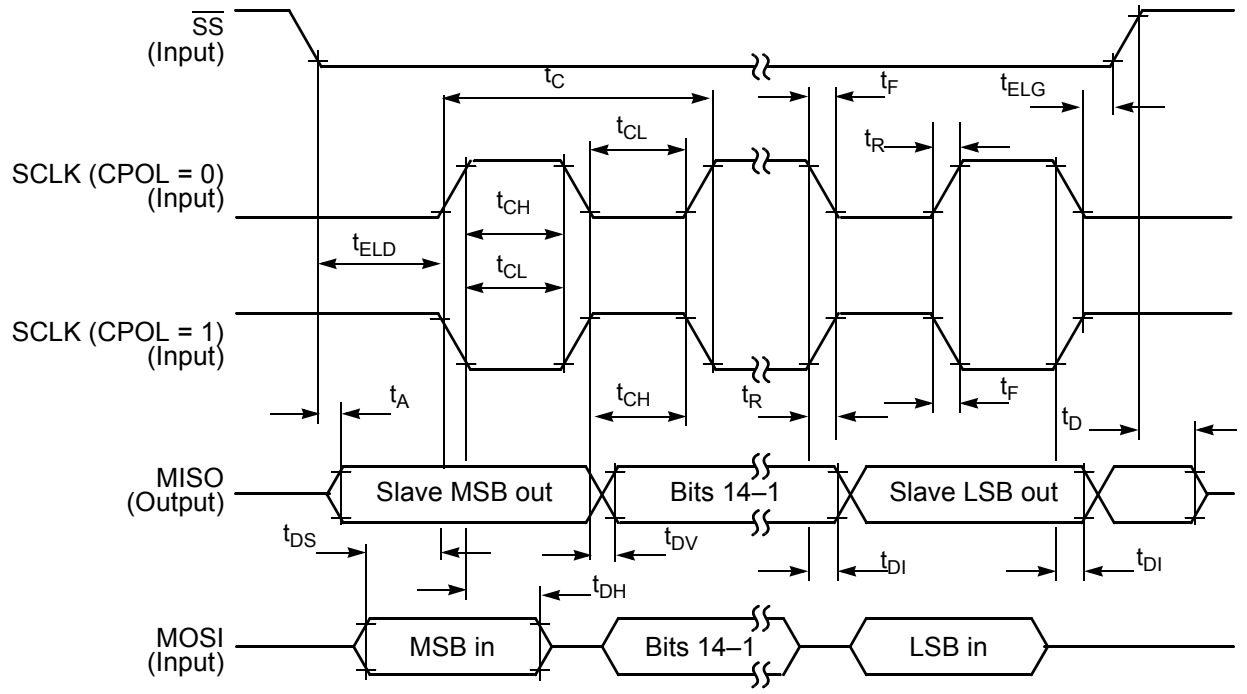


Figure 3-22 SPI Slave Timing (CPHA = 0)

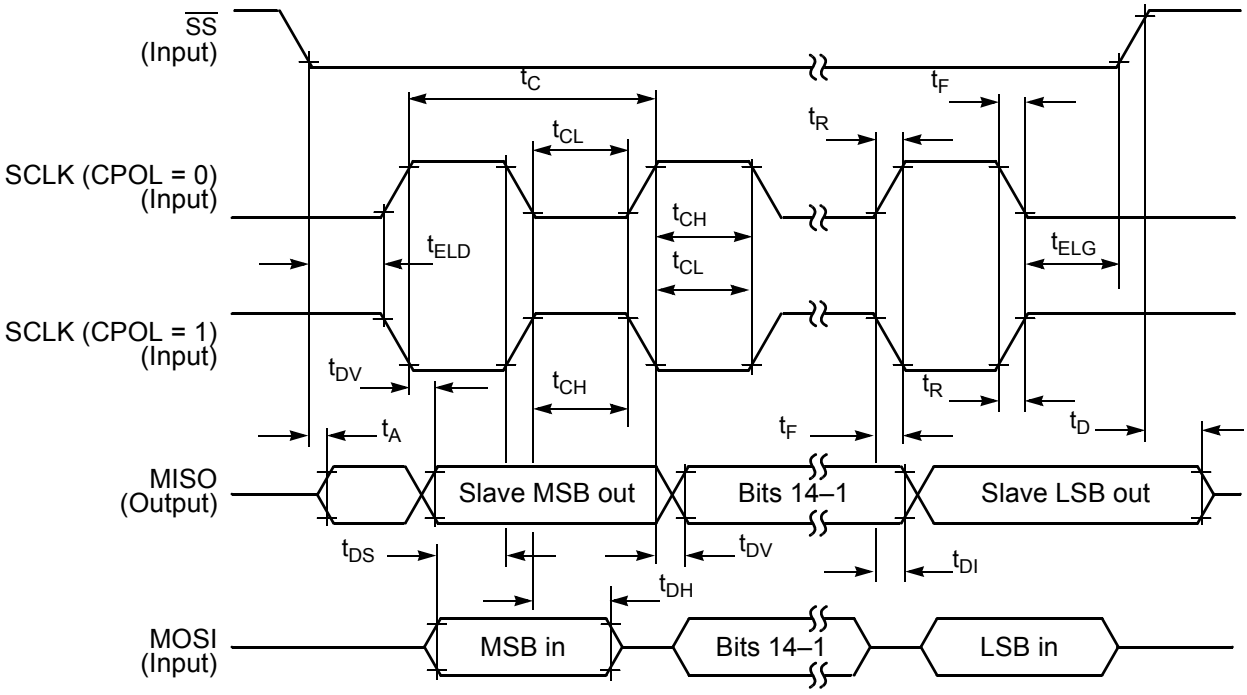


Figure 3-23 SPI Slave Timing (CPHA = 1)

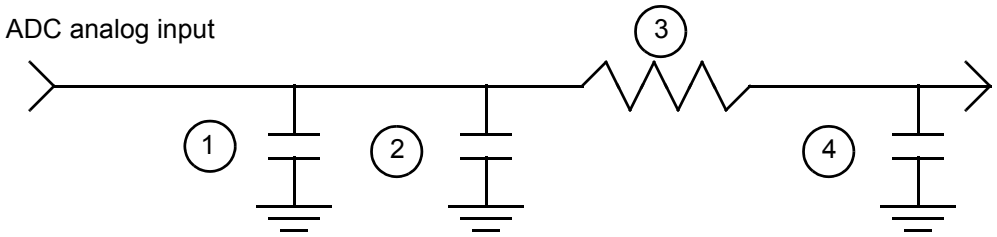
3.10 Analog-to-Digital Converter (ADC) Timing

Table 3-13 ADC Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
ADC Input voltage	V_{ADCIN}	0	—	V_{REFHI}[1]	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[2]	INL	—	+/- 1	+/- 3	LSB[3]
Differential Non-Linearity	DNL	—	+/- 0.4	+/- 1	LSB[3]
Monotonicity	GUARANTEED				
ADC internal clock[4]	f_{ADIC}	0.5	—	2.5	MHz
Conversion range	R_{AD}	V_{REFLO}	—	V_{REFHI}	V
Power-up time	t_{ADPU}	—	25	—	ms
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[5]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[5]
Input capacitance	C_{ADI}	—	5	—	pF[5]
Gain Error (transfer gain)[4]	E_{GAIN}	0.95	1.00	1.10	—
Offset Voltage[4]	V_{OFFSET}	-60	+15	+40	mV
Total Harmonic Distortion[4]	THD	57	66	—	dB
Effective Number of Bits[4]	ENOB	9.3	10.5	—	bit
Spurious Free Dynamic Range[4]	SFDR	58	70	—	dB
Signal-to-Noise plus Distortion[4]	SINAD	56	64	—	dB
ADC quiescent current	I_{ADC}	—	10	—	mA
ADC quiescent current (power down bit set high)	I_{ADCPD}	—	1	—	μA
V_{REF} quiescent current	I_{VREF}	—	1	—	mA
V_{REF} quiescent current (power down bit set high)	I_{VREFPD}	—	1	—	μA

1. V_{REF} must be equal to or less than V_{DDA} and must be greater than 2.7V. For optimal ADC performance, set V_{REF} to V_{DDA}-0.3V.

2. Measured in 10-90% range.
3. LSB = Least Significant Bit.
4. Guaranteed by characterization.
5. $t_{AIC} = 1/f_{ADIC}$



1. Parasitic capacitance due to package, pin to pin, and pin to package base coupling. (1.8pf)
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing. (2.04pf)
3. Equivalent resistance for the ESD isolation resistor and the channel select mux. (500 ohms)
4. Sampling capacitor at the sample and hold circuit. Capacitor 4 is normally disconnected from the input and is only connected to it at sampling time. (1pf)

Figure 3-24 Equivalent Analog Input Circuit

3.11 Synchronous Serial Interface (SSI) Timing

Table 3-14 SSI Master Mode[1] Switching Characteristics

Operating Conditions: $V_{SSIO}=V_{SS} = V_{SSA} = 0V$, $V_{DDA} =V_{DDIO}=3.0–3.6V$, $V_{DD} = 2.25–2.75V$, $T_A = –40°$ to $+85°C$, $C_L \leq 50pF$, $f_{op} = 80MHz$

Parameter	Symbol	Min	Typ	Max	Units
STCK frequency	fs	—	—	10[2]	MHz
STCK period[3]	t_{SCKW}	100	—	—	ns
STCK high time	t_{SCKH}	50[4]	—	—	ns
STCK low time	t_{SCKL}	50[4]	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from STCK high to STFS (bl) high - Master[5]	t_{TFSBHM}	0.1	—	0.5	ns
Delay from STCK high to STFS (wl) high - Master[5]	t_{TFSWHM}	0.1	—	0.5	ns
Delay from SRCK high to SRFS (bl) high - Master[5]	t_{RFSBHM}	0.6	—	1.3	ns
Delay from SRCK high to SRFS (wl) high - Master[5]	t_{RFSWHM}	0.6	—	1.3	ns
Delay from STCK high to STFS (bl) low - Master[5]	t_{TFSBLM}	-1.0	—	-0.1	ns

Table 3-14 SSI Master Mode[1] Switching Characteristics

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, $C_L \leq$ 50pF, f_{op} = 80MHz

Parameter	Symbol	Min	Typ	Max	Units
Delay from STCK high to STFS (wl) low - Master[5]	t_{TFSWLM}	-1.0	—	-0.1	ns
Delay from SRCK high to SRFS (bl) low - Master[5]	t_{RFSBLM}	-0.1	—	0	ns
Delay from SRCK high to SRFS (wl) low - Master[5]	t_{RFSWLM}	-0.1	—	0	ns
STCK high to STXD enable from high impedance - Master	t_{TXEM}	20	—	22	ns
STCK high to STXD valid - Master	t_{TXVM}	24	—	26	ns
STCK high to STXD not valid - Master	t_{TXNVM}	0.1	—	0.2	ns
STCK high to STXD high impedance - Master	t_{TXHIM}	24	—	25.5	ns
SRXD Setup time before SRCK low - Master	t_{SM}	4	—	—	ns
SRXD Hold time after SRCK low - Master	t_{HM}	4	—	—	ns
Synchronous Operation (in addition to standard internal clock parameters)					
SRXD Setup time before STCK low - Master	t_{TSM}	4	—	—	—
SRXD Hold time after STCK low - Master	t_{THM}	4	—	—	—

1. Master mode is internally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 40MHz / 4 = 10MHz for an 80MHz part.
3. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS in the tables and in the figures.
4. 50% duty cycle
5. bl = bit length; wl = word length

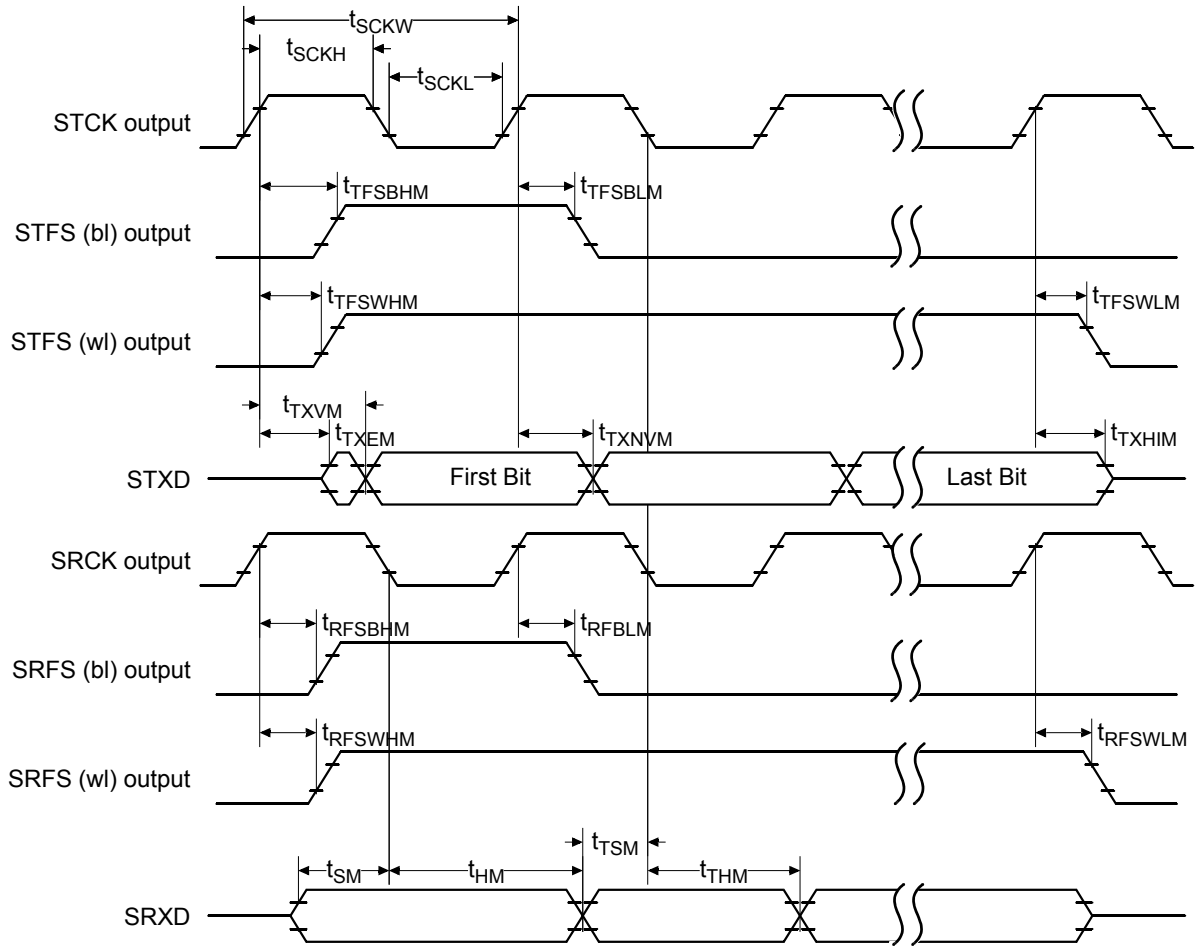


Figure 3-25 Master Mode Timing Diagram

Table 3-15 SSI Slave Mode[1] Switching Characteristics

Operating Conditions: $V_{SSIO}=V_{SS}=V_{SSA}=0V$, $V_{DDA}=V_{DDIO}=3.0–3.6V$, $V_{DD}=2.25–2.75V$, $T_A=–40°$ to $+85°C$, $C_L \le 50pF$, $f_{op}=80MHz$

Parameter	Symbol	Min	Typ	Max	Units
STCK frequency	fs	—	—	10[2]	MHz
STCK period[3]	t_{SCKW}	100	—	—	ns
STCK high time	t_{SCKH}	50[4]	—	—	ns
STCK low time	t_{SCKL}	50[4]	—	—	ns
Output clock rise/fall time	—	—	4	—	ns

Table 3-15 SSI Slave Mode[1] Switching Characteristics

Operating Conditions: $V_{SSIO}=V_{SS} = V_{SSA} = 0V$, $V_{DDA} =V_{DDIO}=3.0–3.6V$, $V_{DD} = 2.25–2.75V$, $T_A = –40°$ to $+85°C$, $C_L \leq 50pF$, $f_{op} = 80MHz$

Parameter	Symbol	Min	Typ	Max	Units
Delay from STCK high to STFS (bl) high - Slave[5]	t_{TFSBHS}	0.1	—	46	ns
Delay from STCK high to STFS (wl) high - Slave[5]	t_{TFSWHS}	0.1	—	46	ns
Delay from SRCK high to SRFS (bl) high - Slave[5]	t_{RFSBHS}	0.1	—	46	ns
Delay from SRCK high to SRFS (wl) high - Slave[5]	t_{RFSWHS}	0.1	—	46	ns
Delay from STCK high to STFS (bl) low - Slave[5]	t_{TFSBLS}	-1	—	—	ns
Delay from STCK high to STFS (wl) low - Slave[5]	t_{TFSWLS}	-1	—	—	ns
Delay from SRCK high to SRFS (bl) low - Slave[5]	t_{RFSBLS}	-46	—	—	ns
Delay from SRCK high to SRFS (wl) low - Slave[5]	t_{RFSWLS}	-46	—	—	ns
STCK high to STXD enable from high impedance - Slave	t_{TXES}	—	—	—	ns
STCK high to STXD valid - Slave	t_{TXVS}	1	—	25	ns
STFS high to STXD enable from high impedance (first bit) - Slave	t_{FTXES}	5.5	—	25	ns
STFS high to STXD valid (first bit) - Slave	t_{FTXVS}	6	—	27	ns
STCK high to STXD not valid - Slave	t_{TXNVS}	11	—	13	ns
STCK high to STXD high impedance - Slave	t_{TXHIS}	11	—	28.5	ns
SRXD Setup time before SRCK low - Slave	t_{SS}	4	—	—	ns
SRXD Hold time after SRCK low - Slave	t_{HS}	4	—	—	ns
Synchronous Operation (in addition to standard external clock parameters)					
SRXD Setup time before STCK low - Slave	t_{TSS}	4	—	—	—
SRXD Hold time after STCK low - Slave	t_{THS}	4	—	—	—

1. Slave mode is externally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 40MHz / 4 = 10MHz for an 80MHz part.
3. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS in the tables and in the figures.
4. 50% duty cycle
5. bl = bit length; wl = word length

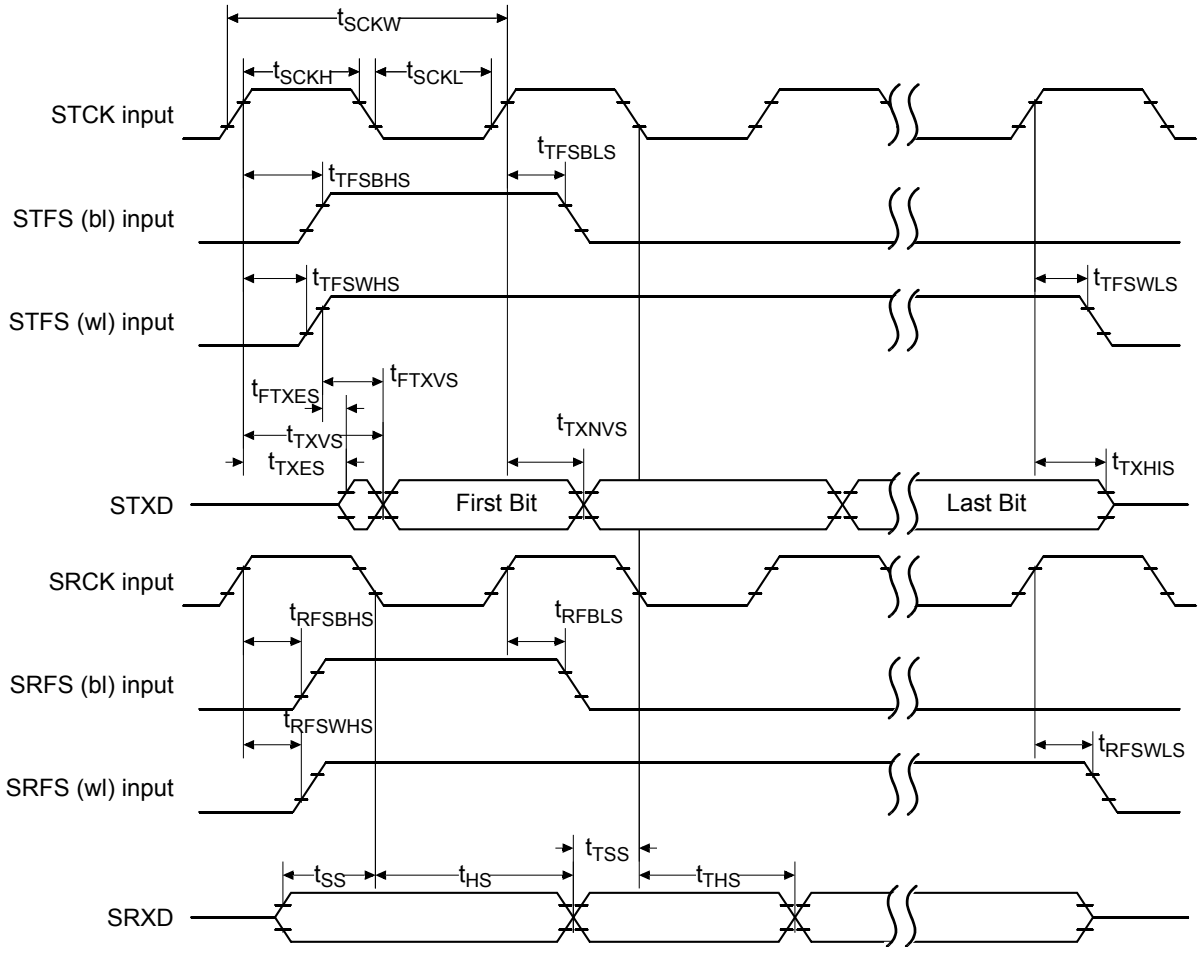


Figure 3-26 Slave Mode Clock Timing

3.12 Quad Timer Timing

Table 3-16 Timer Timing[1, 2]

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, $C_L \leq$ 50pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	4T+6	—	ns
Timer input high/low period	P_{INHL}	2T+3	—	ns
Timer output period	P_{OUT}	2T	—	ns
Timer output high/low period	P_{OUTHL}	1T	—	ns

1. In the formulas listed, T = clock cycle. For 80MHz operation, T = 12.5ns.
2. Parameters listed are guaranteed by design.

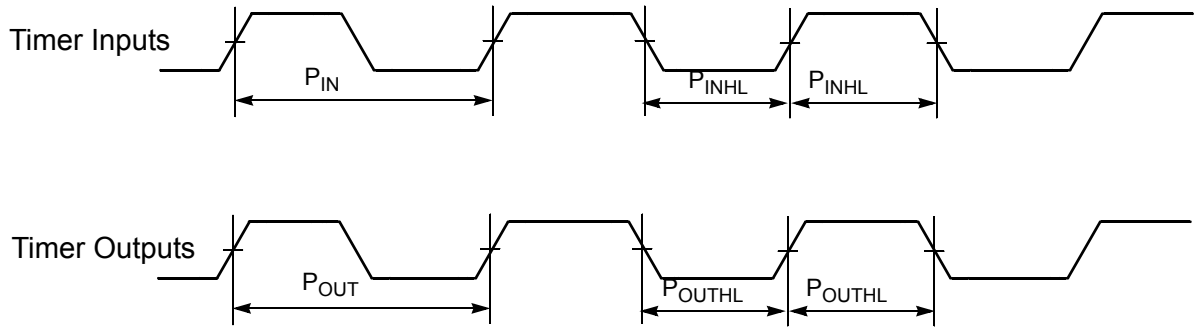


Figure 3-27 Quad Timer Timing

3.13 Serial Communication Interface (SCI) Timing

Table 3-17 SCI Timing[4]

Operating Conditions: V_{SSIO}=V_{SS} = V_{SSA} = 0V, V_{DDA} =V_{DDIO}=3.0–3.6V, V_{DD} = 2.25–2.75V, T_A = –40° to +85°C, C_L ≤ 50pF, f_{op} = 80MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	(f_{MAX}*2.5)/(80)	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

Figure 3-28 RXD Pulse Width

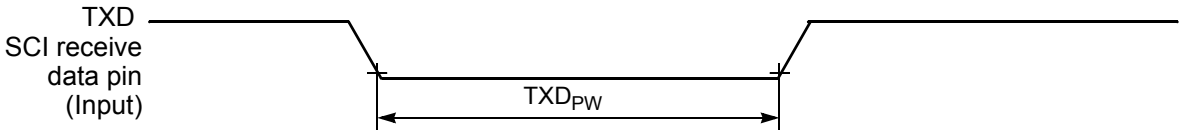


Figure 3-29 TXD Pulse Width

3.14 JTAG Timing

Table 3-18 JTAG Timing[1, 3]

Operating Conditions: $V_{SSIO} = V_{SS} = V_{SSA} = 0V$, $V_{DDA} = V_{DDIO} = 3.0–3.6V$, $V_{DD} = 2.25–2.75V$, $T_A = –40°$ to $+85°C$, $C_L \leq 50pF$, $f_{op} = 80MHz$

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	10	MHz
TCK cycle time	t_{CY}	100	—	ns
TCK clock pulse width	t_{PW}	50	—	ns
TMS, TDI data set-up time	t_{DS}	0.4	—	ns
TMS, TDI data hold time	t_{DH}	1.2	—	ns
TCK low to TDO data valid	t_{DV}	—	26.6	ns
TCK low to TDO tri-state	t_{TS}	—	23.5	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	50	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 80MHz operation, T = 12.5ns.
2. TCK frequency of operation must be less than 1/8 the processor rate.
3. Parameters listed are guaranteed by design.

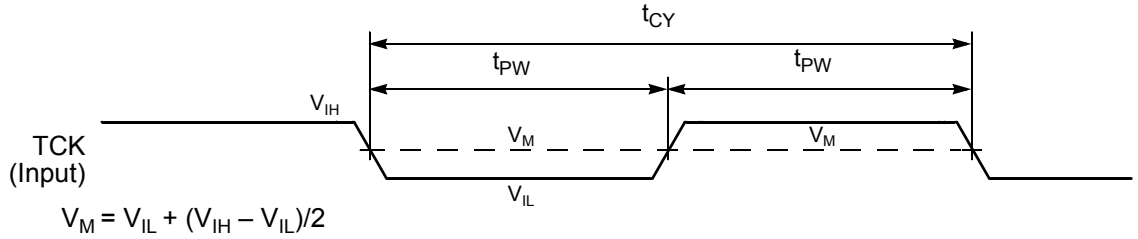


Figure 3-30 Test Clock Input Timing Diagram

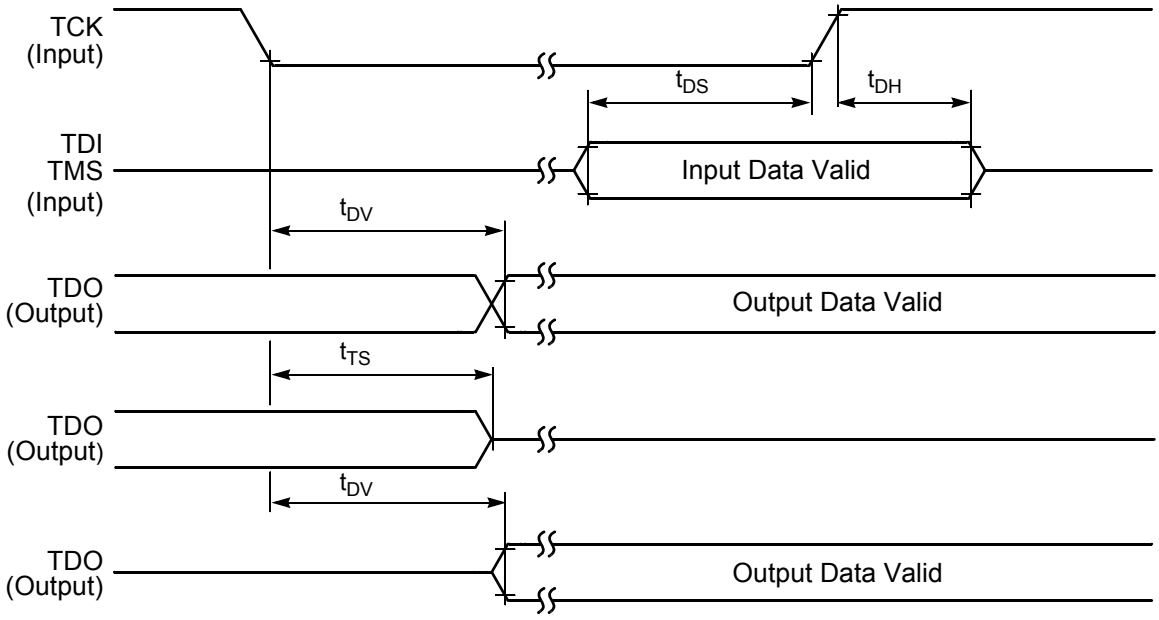


Figure 3-31 Test Access Port Timing Diagram

Figure 3-32 $\overline{\text{TRST}}$ Timing Diagram

Figure 3-33 OnCE—Debug Event

Part 4 Packaging

4.1 Package and Pin-Out Information 56F827

This section contains package and pin-out information for the 128-pin LQFP configuration of the 56F827.

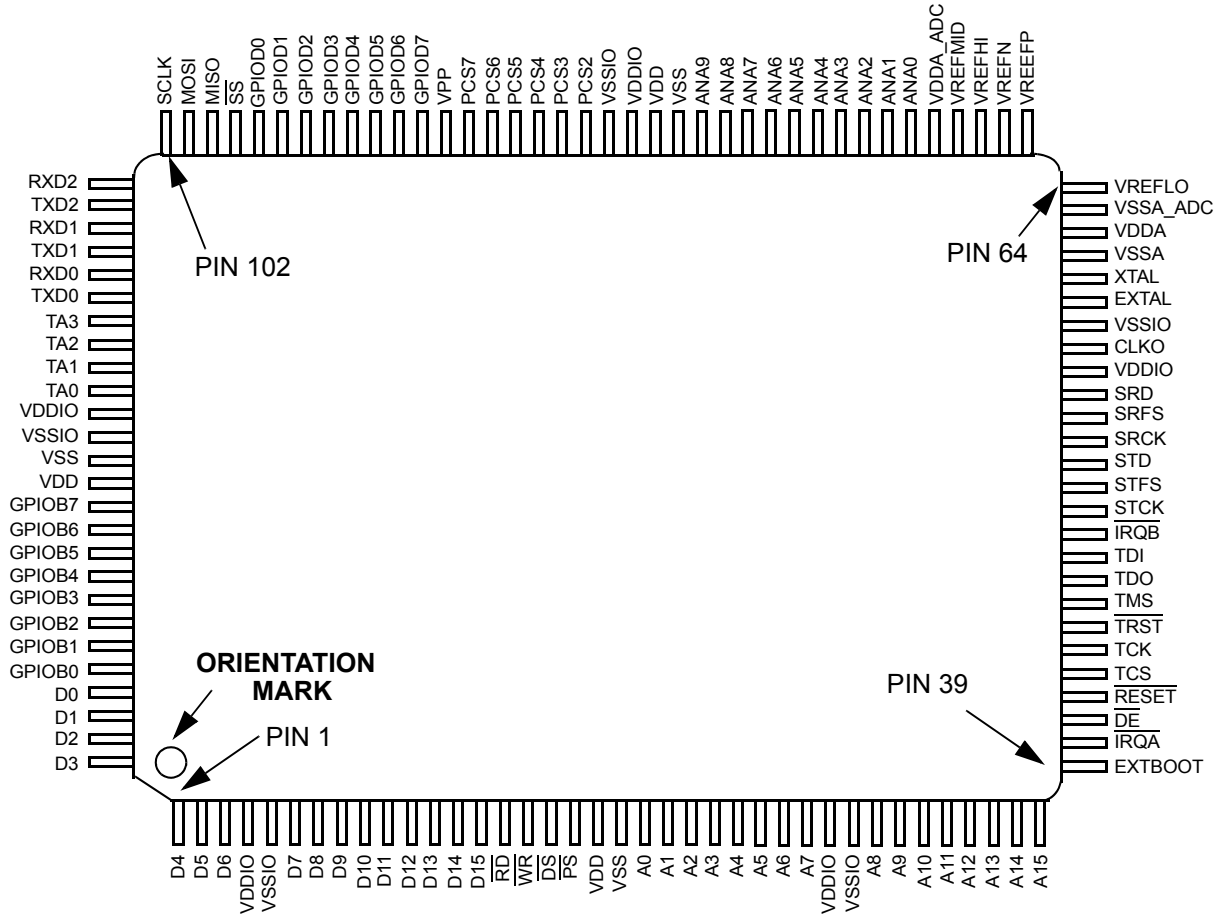


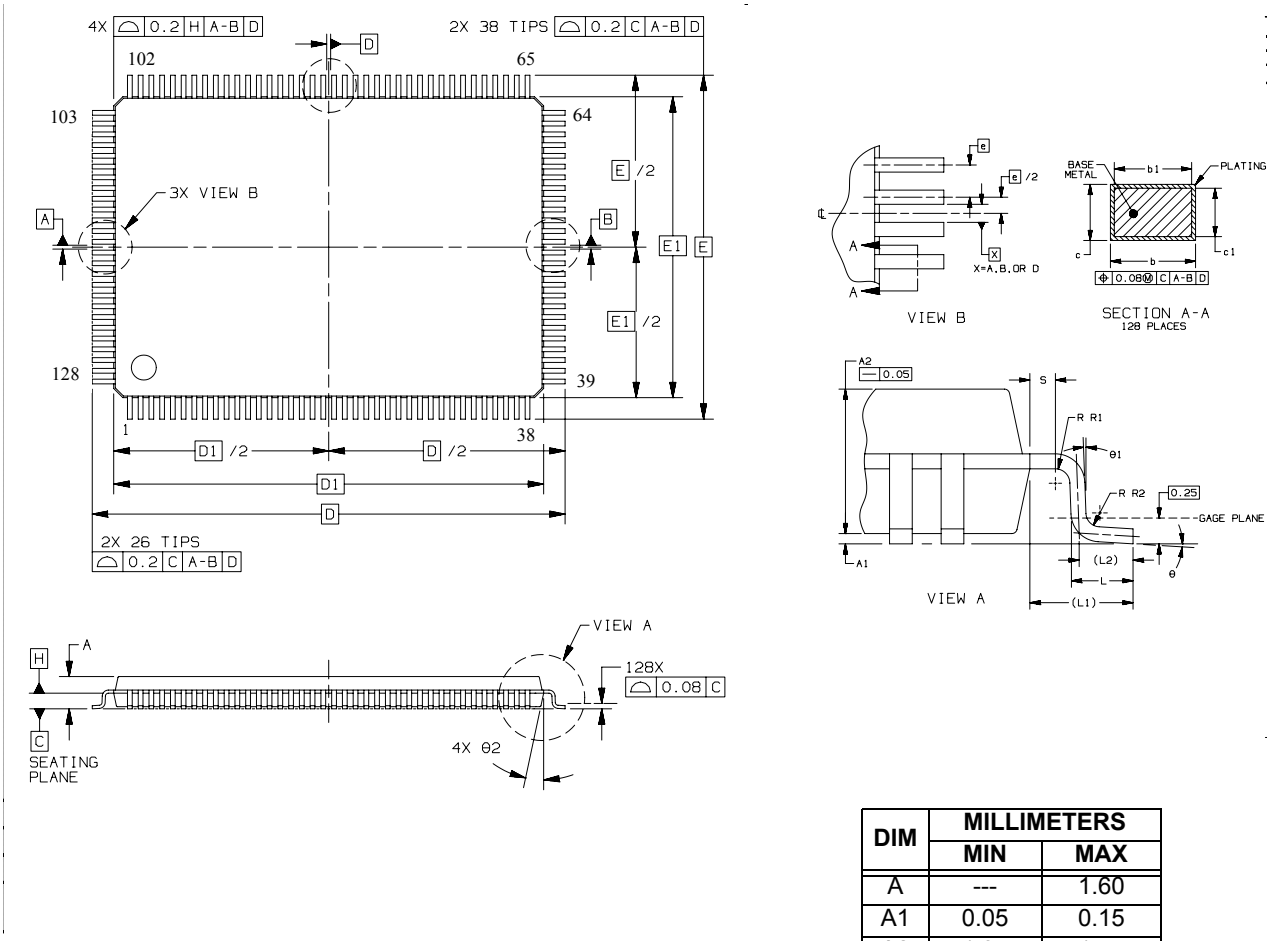
Figure 4-1 Top View, 56F827 128-pin LQFP Package

Table 4-1 56F827 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	D4	33	A10	65	V_{REFP}	97	GPIOD1
2	D5	34	A11	66	V_{REFN}	98	GPIOD0
3	D6	35	A12	67	V_{REFHI}	99	$\overline{SS}$
4	V_{DDIO}	36	A13	68	V_{REFMID}	100	MISO
5	V_{SSIO}	37	A14	69	V_{DDA_ADC}	101	MOSI
6	D7	38	A15	70	ANA0	102	SCLK
7	D8	39	EXTBOOT	71	ANA1	103	RXD2
8	D9	40	$\overline{IRQA}$	72	ANA2	104	TXD2
9	D10	41	$\overline{DE}$	73	ANA3	105	RXD1
10	D11	42	$\overline{RESET}$	74	ANA4	106	TXD1
11	D12	43	TCS	75	ANA5	107	RXD0
12	D13	44	TCK	76	ANA6	108	TXD0
13	D14	45	$\overline{TRST}$	77	ANA7	109	TA3
14	D15	46	TMS	78	ANA8	110	TA2
15	$\overline{RD}$	47	TDO	79	ANA9	111	TA1
16	$\overline{WR}$	48	TDI	80	V_{SS}	112	TA0
17	$\overline{DS}$	49	$\overline{IRQB}$	81	V_{DD}	113	V_{DDIO}
18	$\overline{PS}$	50	STCK	82	V_{DDIO}	114	V_{SSIO}
19	V_{DD}	51	STFS	83	V_{SSIO}	115	V_{SS}
20	V_{SS}	52	STD	84	PCS2	116	V_{DD}
21	A0	53	SRCK	85	PCS3	117	GPIOB7
22	A1	54	SRFS	86	PCS4	118	GPIOB6
23	A2	55	SRD	87	PCS5	119	GPIOB5
24	A3	56	V_{DDIO}	88	PCS6	120	GPIOB4
25	A4	57	CLKO	89	PCS7	121	GPIOB3
26	A5	58	V_{SSIO}	90	VPP	122	GPIOB2
27	A6	59	EXTAL	91	GPIOD7	123	GPIOB1

Table 4-1 56F827 Pin Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
28	A7	60	XTAL	92	GPIOD6	124	GPIOB0
29	V_{DDIO}	61	V_{SSA}	93	GPIOD5	125	D0
30	V_{SSIO}	62	V_{DDA}	94	GPIOD4	126	D1
31	A8	63	V_{SSA_ADC}	95	GPIOD3	127	D2
32	A9	64	V_{REFLO}	96	GPIOD2	128	D3



DIM	MILLIMETERS	
	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	22.00 BSC	
D1	20.00BSC	
e	0.50 BSC	
E	16.00 BSC	
E1	14.00 BSC	
L	0.45	0.75
L1	1.00 REF	
L2	0.50 REF	
S	0.20	---
R1	0.08	---
R2	0.08	0.20
0	0°	7°
01	0°	---
02	11°	13°

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35.

Case Outline - 1129-01

Figure 4-2 128-pin LQFP Mechanical Information

Please see **www.freescale.com** for the most current case outline.

Part 5 Design Considerations

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system-level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system-level model may be appropriate.

Definitions:

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.

- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

5.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each $V_{DD,}$ $V_{DDIO,}$ and V_{DDA} pin on the controller, and from the board ground to each $V_{SS,}$ $V_{SSIO,}$ and V_{SSA} (GND) pin.
- The minimum bypass requirement is to place 0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA} and $V_{DDIO}/V_{SSIO.}$ Ceramic and tantalum capacitors tend to provide better performance tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip $V_{DD,}$ $V_{DDIO,}$ and V_{DDA} and $V_{SS,}$ $V_{SSIO,}$ and V_{SSA} (GND) pins are less than 0.5 inch per capacitor lead.

- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the controller's output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the VREF, V_{DDA} and V_{SSA} pins.
- When using Wired-OR mode on the SPI or the $\overline{\text{IRQx}}$ pins, the user must provide an external pull-up device.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. $\overline{\text{TRST}}$ must be asserted at power up for proper operation. Designs that do not require debugging functionality, such as consumer products, $\overline{\text{TRST}}$ should be tied low.
- Because the Flash memory is programmed through the JTAG/OnCE port, designers should provide an interface to this port to allow in-circuit Flash programming.

Part 6 Ordering Information

Table 6-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 6-1 56F827 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Ambient Frequency (MHz)	Order Number
56F827	2.25–2.75V	Low Profile Quad Flat Pack (LQFP)	128	80	DSP56F827FG80
56F827	2.25–2.75V	Low Profile Quad Flat Pack (LQFP)	128	80	DSP56F827FG80E *

*This package is RoHS compliant.

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