DAC348x EVM

Contents

1 Introduction 2
1.1 Overview 2
1.2 EVM Block Diagram 3
2 Software Control 3
2.1 Installation Instructions 3
2.2 Software Operation 4
3 Basic Test Procedure with TSW1400 11
3.1 TSW1400 Overview 11
3.2 Test Block Diagram for TSW1400 11
3.3 Test Setup Connection 12
3.4 DAC348x Example Setup Procedure 12
4 Basic Test Procedure with TSW3100 16
4.1 TSW3100 Overview 16
4.2 Test Setup Connection 17
4.3 DAC348x Example Setup Procedure 17
4.4 TSW3100 Example Setup Procedure 17

List of Figures

1 DAC348x EVM Block Diagram 3
2 Input Control Option 4
3 PLL Configuration 6
4 Digital Block Options 7
5 Output control Options 8
6 CDCE62005 Tab Configured for 4x Interpolation 9
7 USB Port Reset 10
8 Test Setup Block Diagram for TSW1400 11
9 EVM Platform Selection 12
10 Select DAC348x Devices in the High Speed Converter Pro GUI Program 13
11 Load DAC Firmware Prompt 13
12 Load File to Transfer into TSW1400 14
13 DAC348x Transformer Coupled Output at 60MHz IF 15
14 DAC348x Transformer Coupled Output at 30MHz IF 15
15 TSW3100 FPGA Clock 100-Ω LVDS Termination at Pins T31 and T32 of the FPGA 16
16 Test Setup Block Diagram for TSW3100 17
17 TSW3100 CommSignalPattern (WCDMA) Programming GUI for DAC3484 18
18 TSW3100 CommSignalPattern (WCDMA) Programming GUI for DAC3482, DAC34H84, and DAC34SH84 19

1 Introduction

1.1 Overview

This document is intended to serve as a basic user's guide for the DAC3484/2 EVM Revision F, and DAC34H84/SH84 EVM revision C and above.

The Texas Instruments DAC348x evaluation module (EVM) is a family of circuit boards that allows designers to evaluate the performance of Texas Instruments' DAC348x family of digital-to-analog converters (DAC). The 16-bit, ultra low power family of DACs has either 16-bit wide or 32-bit wide DDR LVDS data input, integrated 2x/4x/8x/16x interpolation filters, 32-bit NCO, on-chip PLL, and exceptional linearity at high IFs. The EVM provides a flexible environment to test the DAC348x under a variety of clock, data input, and IF output conditions.

	DAC3484	DAC3482	DAC34H84	DAC34SH84
Output Channel	4	2	4	4
EVM Part No.	DAC348x Rev. F	DAC348x Rev. F	DAC34H84 Rev. C	DAC34H84 Rev. C
Maximum DAC Rate	1.25GSPS	1.25GSPS	1.25GSPS	1.5GSPS
Digital Interface	16-bit LVDS Interface	16-bit LVDS Interface	32-bit LVDS Interface	32-bit LVDS Interface
Maximum Data Rate per Channel	312.5MSPS	625MSPS	625MSPS	750MSPS
Maximum LVDS Bus Toggle Rate	1.25GSPS	1.25GSPS	1.25GSPS	1.5GSPS
Pattern Generator Support	TSW1400/TSW3100	TSW1400/TSW3100	TSW1400/TSW3100	TSW1400/TSW3100 with limited data rate support

For ease of use as a complete IF transmit solution, the DAC348xEVM includes the Texas Instruments CDCE62005 clock generator/jitter cleaner for clocking the DAC348x. Besides providing a high-quality, low jitter DAC sampling clock to the DAC348x, the CDCE62005 also provides FPGA clocks to the TSW1400EVM (or TSW3100EVM) as FPGA reference clocks.

The EVM can be used along with Texas Instruments TSW1400 or TSW3100 with limited data rate support (up to 1.25GSPS LVDS Bus rate) to perform a wide varieties of test and measurements. The TSW1400 generates the test patterns that are fed to the DAC348x through a maximum 1.5 GSPS LVDS Bus port. These EVM boards are also compatible with Altera® and Xilinx® FPGA development platforms for rapid evaluation and prototyping. The on-board HSMC connector input allows direct connection to the HSMC compatible Altera development platforms, and the externally attached FMC-DAC-Adapter board available from TI enables the connection of the EVM to the Xilinx development platforms with FMC headers.

For evaluation of complete RF transmit solution, see the TSW308x EVM. The EVM integrates the DAC348x, TRF3705, and LMK04800 devices into one RF transmitter system.

See the TSW308x EVM web folders at:

http://www.ti.com/tool/tsw3085evm
http://www.ti.com/tool/tsw3084evm
http://www.ti.com/tool/tsw30h84evm
http://www.ti.com/tool/tsw30sh84evm

1.2 EVM Block Diagram

Figure 1 shows the configuration of the EVM with the TSW1400 or TSW3100 used for pattern generation.

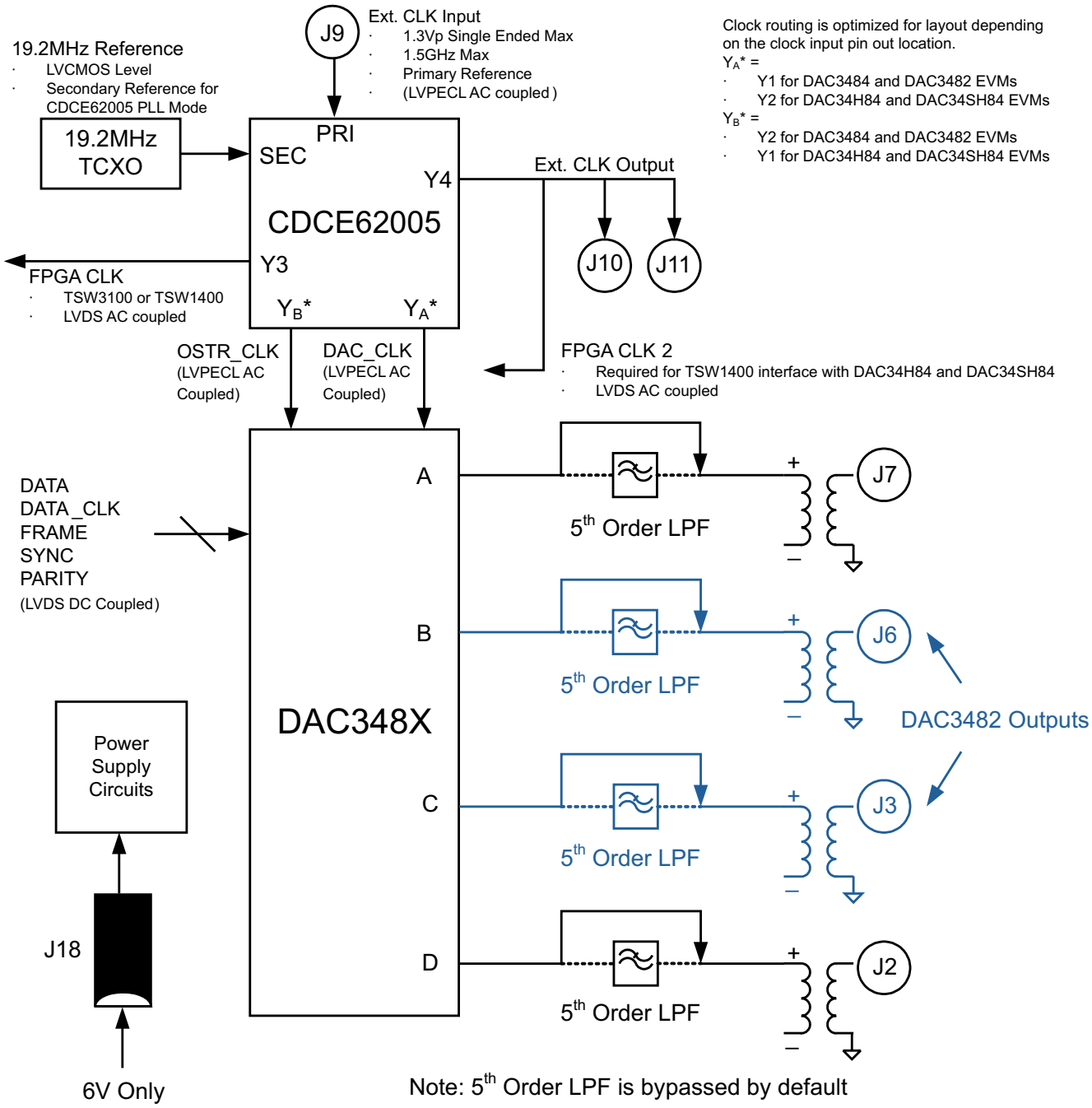


Figure 1. DAC348x EVM Block Diagram

2 Software Control

2.1 Installation Instructions

- Open folder named DAC348x_Installer_vxpx (xpx represents the latest version)
- Run Setup.exe
- Follow the on-screen instructions

- Once installed, launch the program by clicking on the DAC348x_GUI_vxpx program in Start>Texas Instruments DACs. The installation directory is located at C:\Program Files\Texas Instruments\DAC348x
- When plugging in the USB cable for the first time, you will be prompted to install the USB drivers.
  - When a pop-up screen opens, select “Continue Downloading”.
  - Follow the on screen instructions to install the USB drivers
  - If needed, you can access the drivers directly in the install directory

2.2 Software Operation

The software allows programming control of the DAC device and the CDC device. The front panel provides a tab for full programming of each device. The GUI tabs provide more convenient and simplified interface to the most used registers of each device.

Each device, including the DAC3484, DAC3482, and DAC34H84/SH84, has its own custom control interface. At the top level of the GUI are five control tabs. The first four are used to configure the DAC348x and the last for the CDCE62005.

2.2.1 Input Control Options

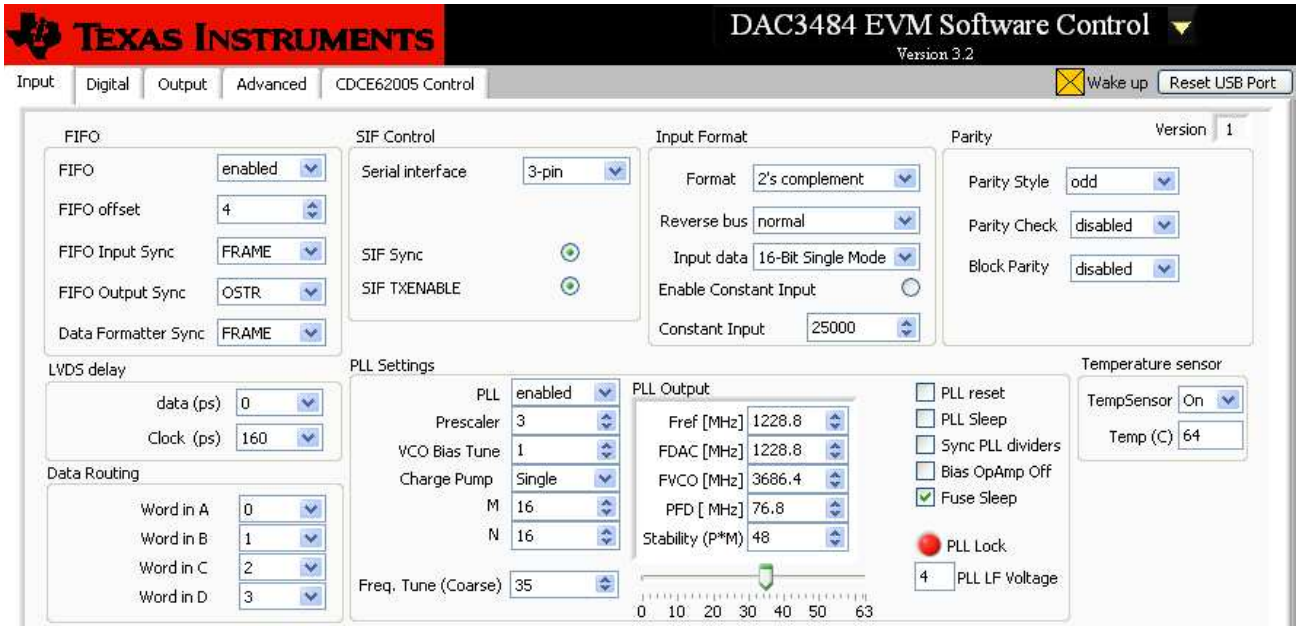


Figure 2. Input Control Option

- FIFO: allows the configuration of the FIFO and FIFO synchronization (sync) sources.
- LVDS delay: provides internal delay of either the LVDS DATA or LVDS DATACLK to help meet the input setup/hold time.
- Data Routing: provides flexible routing of the A, B, C, and D sample input data to the appropriate digital path.
  Note: the DAC3482 does not support this mode
- SIF Control: provides control of the Serial Interface (3-wires or 4-wires) and Serial Interface Sync (*SIF Sync*).
- Input Format: provides control of the input data format (i.e., 2s complement or offset binary)
- Parity: provides configuration of the parity input.
- PLL Settings: provides configuration of the on-chip PLL circuitry.
- Temperature Sensor: provides temperature monitoring of DAC3484/2 die temperature.

2.2.1.1 FIFO Settings

The DAC348x has 8-samples deep FIFO to relax the timing requirement of a typical transmitter system. The FIFO has an input pointer and an output pointer, and both pointers can accept various input sources as reset triggers of input and output pointer position. One important application for input and output pointer control is the ability to synchronize multiple DACs in the system. For additional information, see the relevant DAC348x data sheet.

- FIFO Offset: The default position of FIFO output pointer after reset by the synchronization source. This setting can be used to change the latency of the DAC348x.
- Data Formatter Sync (DAC3482 and DAC3484): Synchronization source for FIFO data formatter. Select between LVDS FRAME or LVDS SYNC signals.
- FIFO Sync Select (DAC34H84 and DAC34SH84): Select the internal digital routing of LVDS ISTR or LVDS SYNC to the FIFO ISTR path
- FIFO Input Sync: Synchronization source for FIFO input pointer. Select among the LVDS FRAME (ISTR), LVDS SYNC, and/or SPI register SIF-SYNC to reset the FIFO input pointer position.
- FIFO Output Sync: Synchronization source for FIFO output pointer. Select among the LVDS FRAME (ISTR), LVDS SYNC, SPI register SIF-SYNC, and/or OSTR signal to reset the FIFO output pointer position.
  - For single device application without the need for precise latency control, Single Sync Source Mode may be used. The FIFO output pointer position can be reset with LVDS FRAME (ISTR), LVDS SYNC, and/or SPI register SIF-SYNC. See the Single Sync Source Mode in the relevant DAC348x data sheet for details.
  - For multiple device synchronization, select the OSTR signal as the FIFO output synchronization source. If the DAC is configured to accept external DAC Clock input, then the OSTR signal is the external LVPECL signal to the OSTRP/N pins. If the DAC is configured to accept the internal on-chip PLL clock, then the OSTR signal is the internally generated PFD frequency. See the Dual Sync Sources Mode in the relevant DAC348x data sheet for details.

2.2.1.2 LVDS Delay Settings

Depending on the signal source implementation (i.e. TSW1400, TSW3100, or FPGA System), the following options can be implemented to meet the minimum setup and hold time of DAC348x data latching:

- Set the on-chip LVDS DATA or DATACLOCK delay: The DAC348x includes on-chip LVDS DATA or DATACLK delay. The delay ranges from 0ps to 280ps with an approximate 40ps step. This LVDS DATACLOCK delay does not account for additional PCB trace-to-trace delay variation, only the internal DATACLK delay.
  - The TSW1400 pattern generator sends out LVDS DATA and DATACLK as center aligned signal. Additional DATACLK delay is not needed.
  - The TSW3100 pattern generator sends out LVDS DATA and DATACLK as edge-aligned signal. Typical setting of 160ps or more will help meet the timing requirement for most of the TSW3100 + DAC348x EVM setup.
- Modify the external LVDS DATACLK PCB trace delay: Additional trace length on the bottom side of the PCB can be added to the LVDS DATACLK PCB trace length. Set SJP9, SJP10, SJP11, and SJP12 to 2-3 position for approximately 220ps of trace delay.

2.2.1.3 PLL Settings

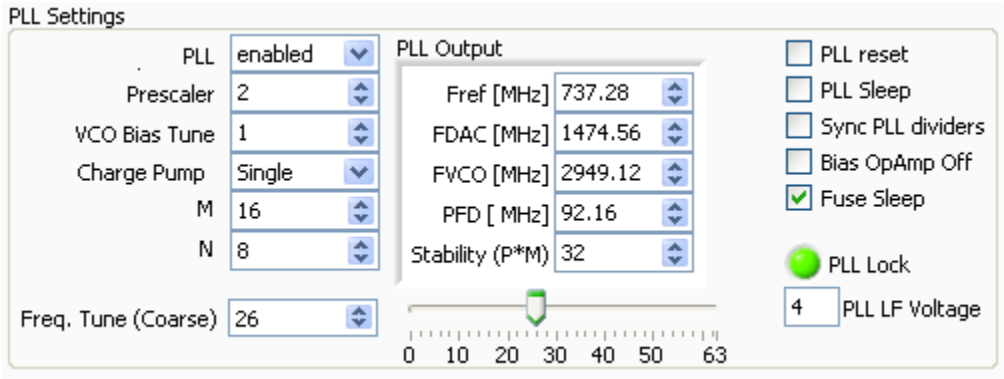


Figure 3. PLL Configuration

Follow the steps below to configure the PLL.

1. Enable PLL
2. Uncheck *PLL reset* and *PLL sleep*
3. Set *M* and *N* ratio such that F_{DAC} = (M)/(N) x Fref
4. For the DAC3482, DAC3484, and DAC34H84: Set the *prescaler* such that the F_{DAC} x prescaler is within 3.3GHz and 4GHz.
5. For the DAC34SH84, Set the *prescaler* such that the F_{DAC} x prescaler is within 2.7GHz and 3.3GHz.
6. Set *VCO Bias Tune* to “1”
7. *Charge Pump* setting
   (a) If stability (P x M) is less than 120, then set to “Single”.
   (b) If stability (P x M) is greater than 120, then set to “Double” or install external loop filter
8. Adjust the *Freq. Tune* (*coarse tune*) accordingly. For additional information, see the relevant DAC348x data sheet.

2.2.2 Digital Block Options

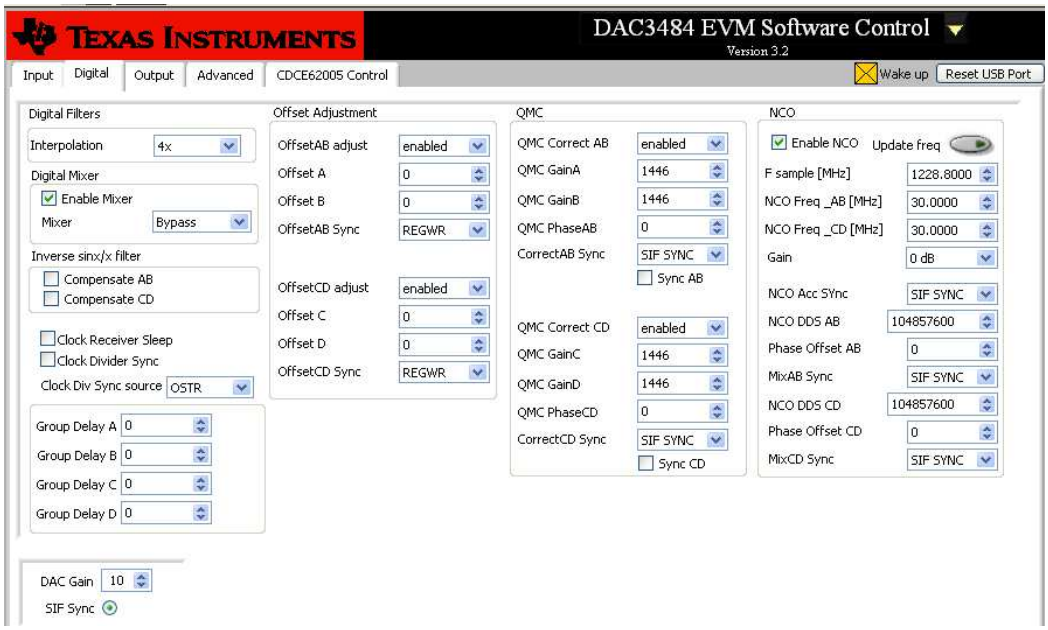


Figure 4. Digital Block Options

- Interpolation: allows control of the data rate versus DAC sampling rate ratio (i.e. data rate x interpolation = DAC sampling rate).
- Digital Mixer: allows control of the coarse mixer function.
  Note: If fine mixer (NCO) is used, the "Enable Mixer" button must be checked, and the coarse mixer must be bypassed. See the following NCO bullet for detail.
- Inverse sinx/x filter: allows compensation of the sinx/x attenuation of the DAC output.
  Note: If inverse sinx/x filter is used, the input data digital full-scale must be backed off accordingly to avoid digital saturation.
- Clock Receiver Sleep: allows the DAC clock receiver to be in sleep mode. The DAC has minimum power consumption in this mode.
- Clock Divider Sync: allows the synchronization of the internal divided-down clocks using either FRAME, SYNC, or OSTR signal. Enable the divider sync as part of the initialization procedure or resynchronization procedure.
- Group Delay: allows adjustment of group delay for each I/Q channel. This is useful for wideband sideband suppression. **Note:** This feature is not available for the DAC34SH84.
- Offset Adjustment: allows adjustment of dc offset to minimize the LO feed-through of the modulator output. This section requires syncing for proper operation. The synchronization options are listed below:
  - **REGWR: auto-sync from SIF register write. If this option is chosen, the GUI automatically synchronizes the offset adjustment with each value update by writing to 0x08 (offset A) or 0x0A (offset B) registers last.**
  - OSTR: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source
  - SYNC: sync from the external LVDS SYNC signal.
  - **SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**
- QMC Adjustment: allows adjustment of the gain and phase of the I/Q channel to minimize sideband power of the modulator output.
  - **REGWR: auto-sync from SIF register write. If this option is chosen, the GUI automatically synchronizes the offset adjustment with each value update by writing to 0x10 (QMC phase AB) or 0x11 (QMC phase CD) registers last.**

  - OSTR: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source.
  - SYNC: sync from the external LVDS SYNC signal.
  - **SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**
- NCO: allows fine mixing of the I/Q signal. The procedure to adjust the NCO mixing frequency are listed below:
  1. Enter the DAC sampling frequency in *Fsample.*
  2. Enter the desired mixing frequency in both *NCO freq_AB* and *NCO freq_CD*.
  3. Press *Update freq*
  4. Sync the NCO block from the following options:
     - **REGWR: auto-sync from SIF register write. Writing to either Phase OffsetAB or Phase OffsetCD can create a sync event.**
     - *OSTR*: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source. Refer to the datasheet for OSTR period requirement.
     - *SYNC*: sync from the external SYNC signal
     - **SIF SYNC: sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**

2.2.3 Output Control Options

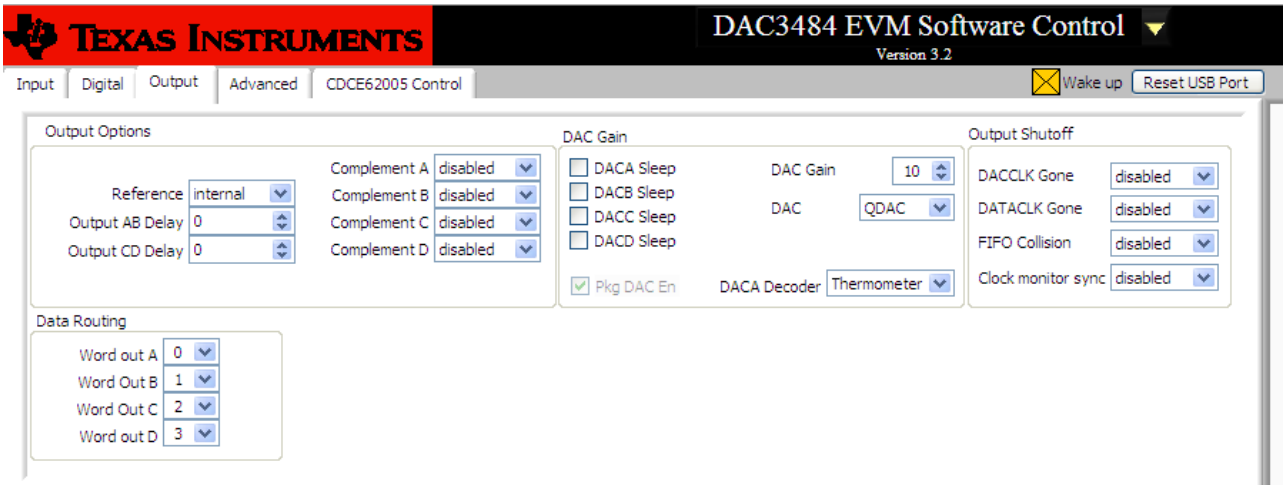


Figure 5. Output control Options

- Output Options: allows the configuration of reference, output polarity, and output delay
- Data Routing: provides flexible routing of the A, B, C, and D digital path to the desired output channels. **Note:** The DAC3482 does not support this mode.
- DAC Gain: configures the full-scale DAC current and DAC3484/DAC3482 mode. With Rbiaj resistor set at 1.28kΩ:
  - DAC Gain = 15 for 30mA full-scale current.
  - DAC Gain = 10 for 20mA full-scale current (default).
- Output Shutoff On: allows outputs to shut-off when DACCLK GONE, DATACLK GONE, or FIFO COLLISION alarm event occurs.

2.2.4 CDCE62005

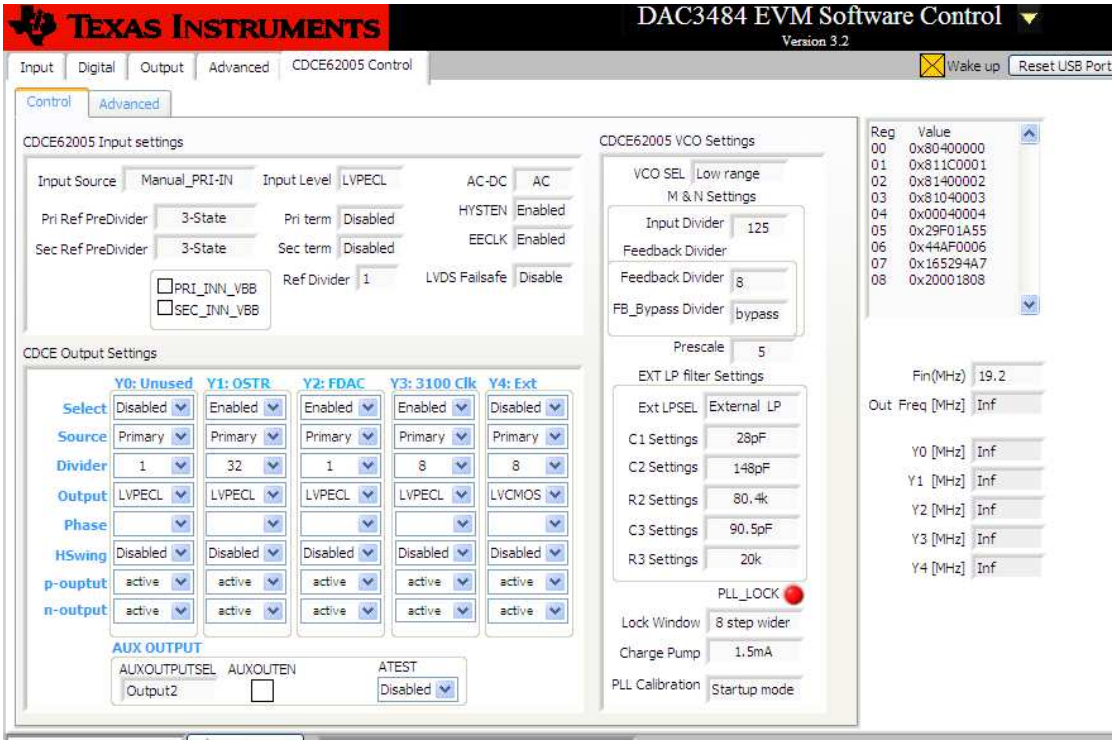


Figure 6. CDCE62005 Tab Configured for 4x Interpolation

Clock frequency control is determined by register values in the CDCE62005 Control tab. See the CDCE62005 data sheet for detailed explanations of the register configuration to change the clock frequency.

The following CDCE62005 outputs are critical to proper operation of the DAC348x:

- **Y_A*: DAC348x DAC sampling clock.** This clock is an ac coupled LVPECL. If the DAC348x is configured for internal PLL mode, this will be the reference clock input for the PLL block.
  - Y_A* = Y1 for DAC3484 and DAC3482 EVMs
  - Y_A* = Y2 for DAC34H84 and DAC34SH84 EVMs
- **Y_B*: DAC348x FIFO OSTR clock.** This clock is an ac coupled LVPECL. The clock rate for this should be at least F_{DAC}/*Interpolation/8*. See the DAC348x data sheet for more details.
  - The whole OSTR clock equation needs to take account of both the Y1 CDCE62005 clock divider ratio and the additional CDCP1803 divide-by-2 clock divider.
  - This OSTR signal can be a slower periodic signal or a pulse depending on the application.
  - **Note:** The FIFO OSTR clock should be disabled when the DAC348x is configured in PLL mode.
  - Y_B* = Y2 for DAC3484 and DAC3482 EVMs
  - Y_B* = Y1 for DAC34H84 and DAC34SH84 EVMs
- **Y3: FPGA Clock 1.** This clock is an ac coupled LVDS. The clock rate for this should be
  - F_{DAC}/*interpolation/2* for DAC3484
  - F_{DAC}/*interpolation/4* for DAC3482, DAC34H84, and DAC34SH84
- **Y4: FPGA Clock 2.** This clock is an ac coupled LVDS. This clock must be enabled when using the DAC34H84 and DAC34SH84 with the TSW1400. The clock rate for this should be F_{DAC}/*interpolation/4* for DAC34H84, and DAC34SH84

2.2.5 Register Control

- **Send All:** Sends the register configuration to all devices
- **Read All:** Reads register configuration from DAC348x device
- **Load Regs:** Load a register file for all devices. Sample configuration files for common frequency plans are located in the install directory: C:\Programs Files\Texas Instruments\DAC348x\EVM Configuration File Released.
  - Select *Load Regs* button.
  - Double click on the *EVM Configuration File Released* folder and respective sub-folders for the EVM.
  - Double click on the desired register file.
  - Click on *Send All* to ensure all of the values are loaded properly.
- **Save Regs:** Saves the register configuration for all devices

2.2.6 Miscellaneous Settings

- **Reset USB:** Toggle this button if the USB port is not responding. This generates a new USB handle address
  - **Note:** It is recommended that the board be reset after every power cycle and the “reset usb” button on the GUI be clicked.

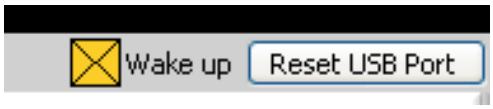


Figure 7. USB Port Reset

- **Exit:** Stops the program

3 Basic Test Procedure with TSW1400

This section outlines the basic test procedure for testing the EVM with the TSW1400.

3.1 TSW1400 Overview

The TSW1400 is a high speed data capture and pattern generator board. When functioning as a pattern generator, it has a maximum LVDS bus rate of 1.5 GSPS, and this allows evaluation of the DAC348x with maximum 750 MSPS of input data rate per channel.

See the TSW1400 user's guide (SLWU079) for more detailed explanation of the TSW1400 setup and operation. This document assumes that the High Speed Data Converter Pro software (SLWC107) is installed and functioning properly.

3.2 Test Block Diagram for TSW1400

The test setup for general testing of the DAC348x with the TSW1400 pattern generation card is shown in Figure 8.

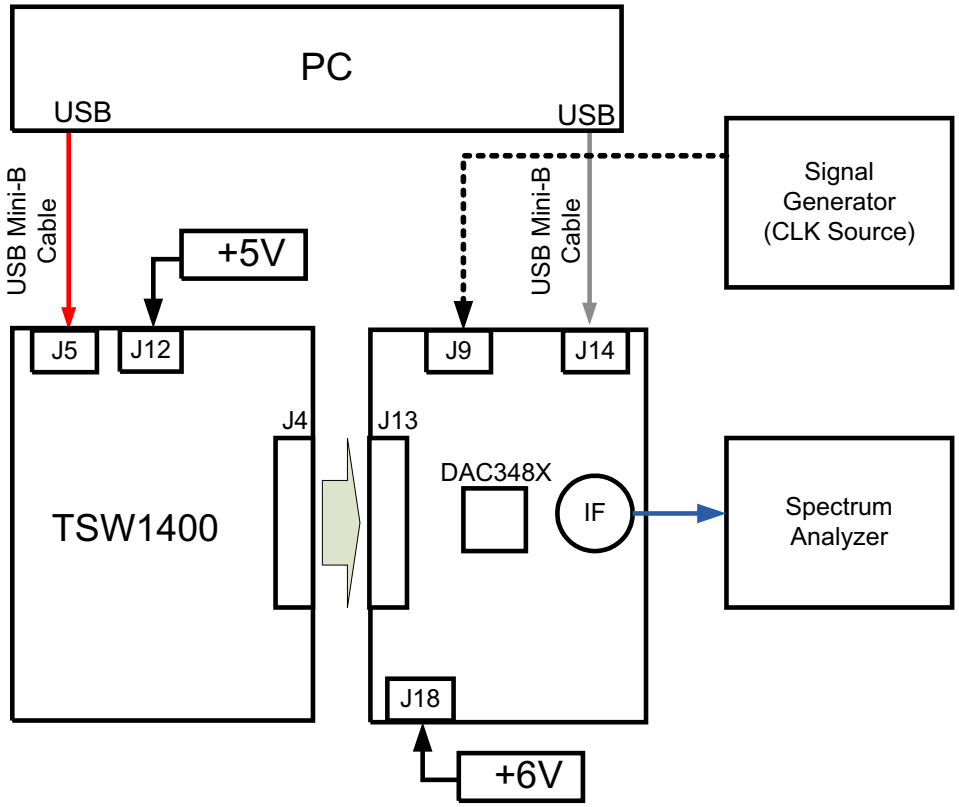


Figure 8. Test Setup Block Diagram for TSW1400

3.3 Test Setup Connection

TSW1400 Pattern Generator.

1. Connect the EVM-supplied 18-AWG wires to the DC plug cable (Tensility 10-01776) to a qualified lab bench power supply. The 18-AWG red wire is the 5-V wire while the 18-AWG black wire is the ground wire.
2. Connect a 5-V power supply cable to J12, the *5V_IN* jack of the TSW1400 EVM.
3. Connect PC's USB port to J5 USB port of the TSW1400 EVM. The cable should be a standard A to mini-B connector cable.

DAC348xEVM

1. Connect the EVM-supplied 18-AWG wires to the DC plug cable (Tensility 10-01776) to a qualified lab bench power supply. The 18-AWG red wire is the 6-V wire while the 18-AWG black wire is the ground wire.
2. Connect J13 connector of DAC348xEVM to J4 connector of TSW1400 EVM.
3. Connect a 6-V power supply cable to J18, the *Power In* jack of the DAC3484 EVM.
4. Connect PC's USB port to J14 USB port of the DAC348x EVM. The cable should be a standard A to mini-B connector cable.
5. Provide a 1.3Vp, 1.5GHz max clock at J9, *CLKIN* SMA port of DAC348x EVM.
6. Connect the IF output port of J2, J3, J6, or J7 to the spectrum analyzer.

DAC348xEVM Jumpers: (make sure the following jumpers are at their default setting)

Reference Designator	Setting	Function
JP2	1-2	DAC348x TXENABLE.
JP3	2-3	DAC348x SLEEP.
JP4	2-3	CDCE62005 Primary Input LVPECL Bias Enable.
JP5	1-2	CDCE62005 Reference Input Select.
JP6	1-2	CDCE62005 Power Down.
JP7	short	19.2MHz TCXO Enable.
JP8, JP9, JP12, JP13	short	SPI connection break point. This allows routing of SPI connection to external system if troubleshooting is needed.
JP10	1-2	6V Input Select. Default is 6V at J18.
JP11	open	For DAC34H84/SH84 EVM only. Allows SPI and IO logic threshold to switch among 1.8V, 2.5V, or 3.3V.
SJP9, SJP10, SJP11, SJP12	1-2	DAC348x DATACLK delay. Default is zero trace delay.

3.4 DAC348x Example Setup Procedure

1. Provide the clock input **1228.8** MHz at 1.5Vrms at J9 SMA Connector of the DAC348x EVM.
2. Turn on power to the board and press the reset SW1 button on the EVM
3. Press the "Reset USB Port" button in GUI and verify USB communication.
4. Select the appropriate EVM platform on the software menu.

Figure 9. EVM Platform Selection

5. Click "LOAD REGS", browse to the installation folder and load example file "*DAC3484_FDAC_1228p8MHz_4xint_NCO_30MHz_QMCon.txt*". This file contains settings for 4x interpolation with the DAC3484 running at 1228.8MSPS. Load this file and wait a couple of seconds for the settings to go into effect. The DAC3482, DAC34H84, and DAC34SH84 equivalent example files are also available in the installation folder.

TSW1400 Example Setup Procedure

1. Start the High Speed Converter Pro GUI program. When the program starts, select the DAC tab and then select the corresponding device in the “Select DAC” menu.

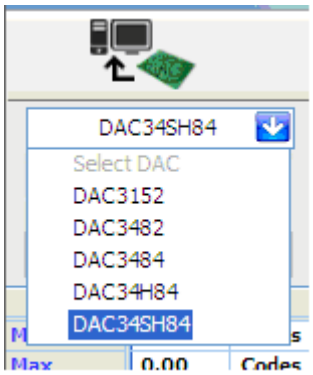


Figure 10. Select DAC348x Devices in the High Speed Converter Pro GUI Program

2. When prompted *Load DAC Firmware?*, select *YES*.

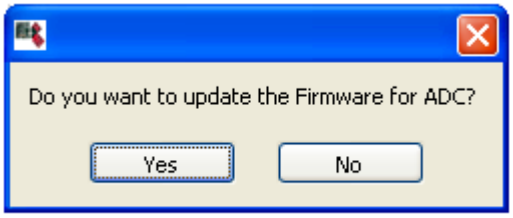


Figure 11. Load DAC Firmware Prompt

3. Click on the button labeled “Load File to transfer into TSW 1400”, located near the top left of the GUI.

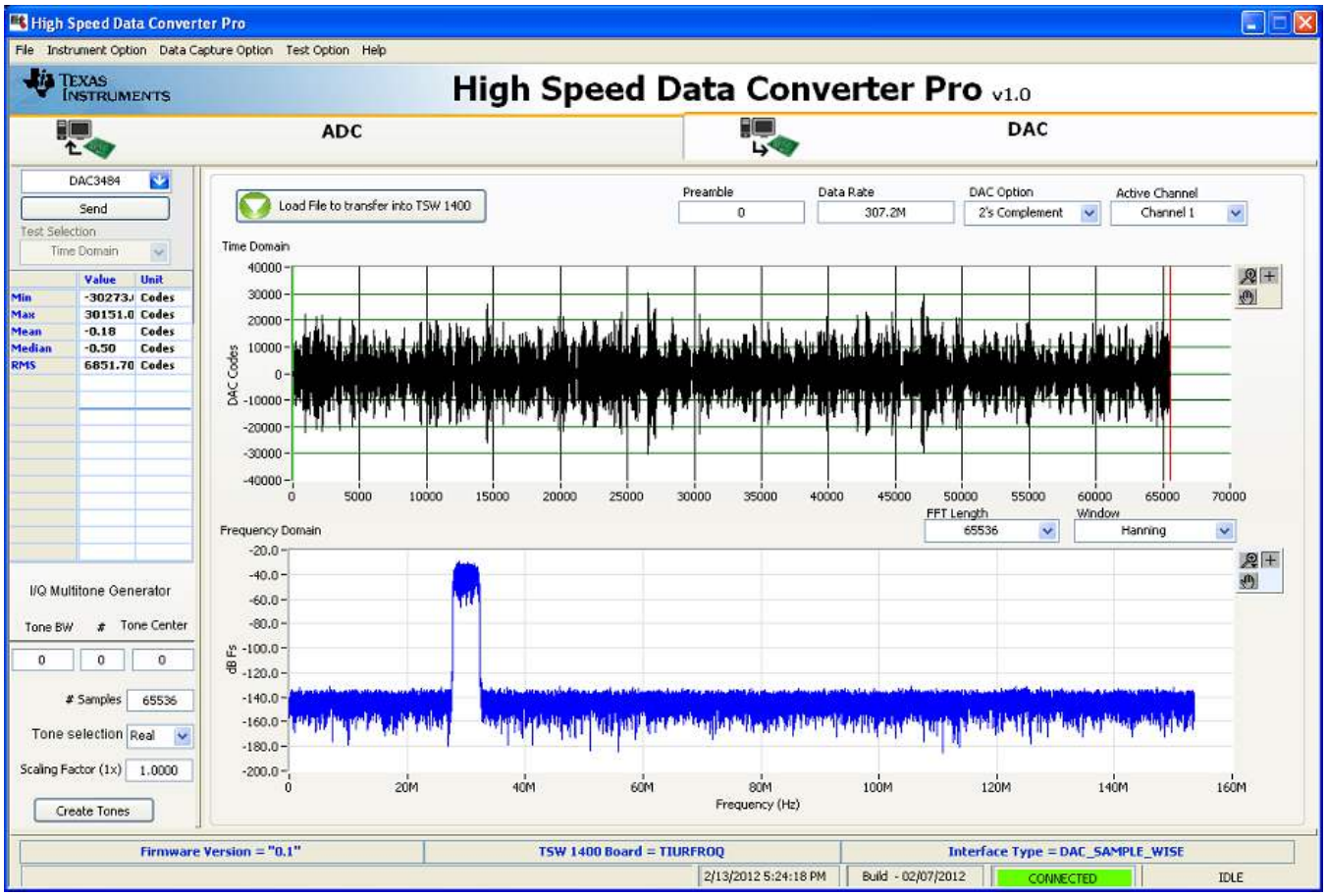
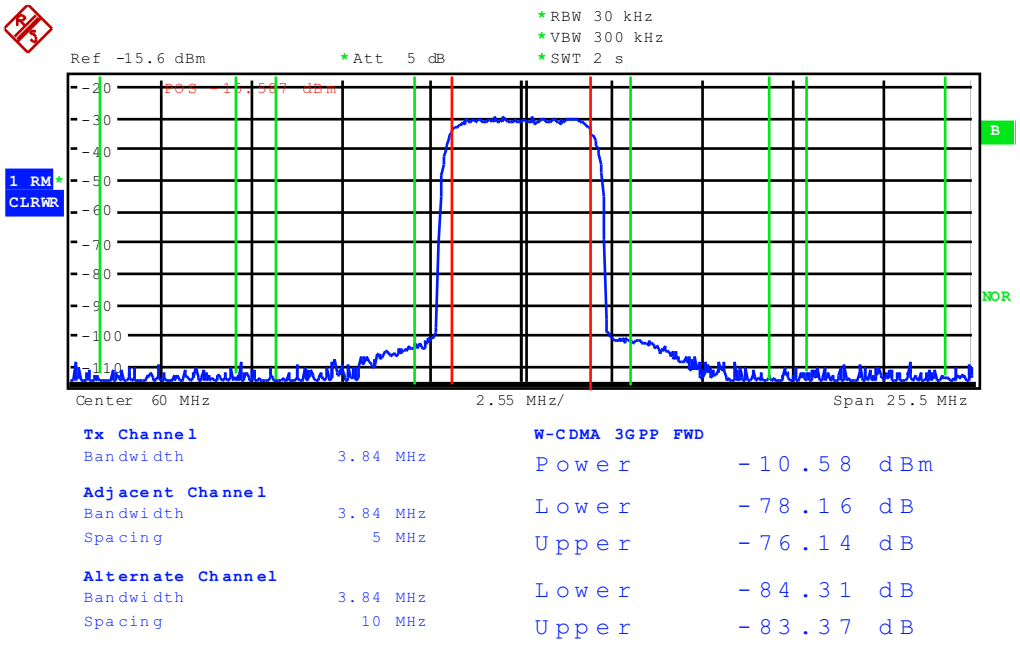


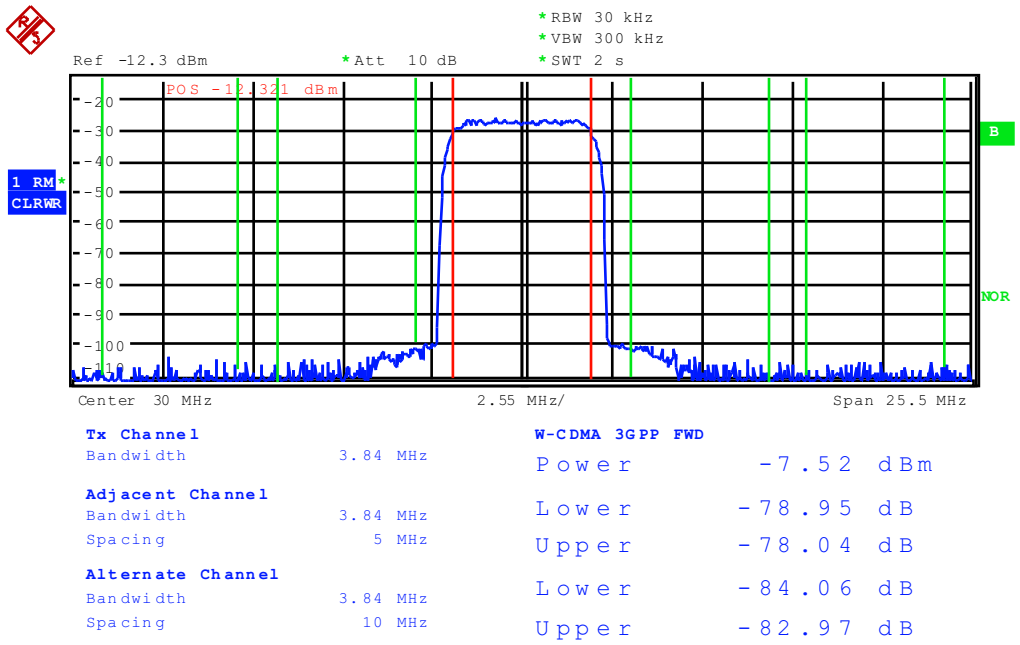
Figure 12. Load File to Transfer into TSW1400

4. Select the file "WCDMA_TM1_complexIF30MHz_Fdata307.2MHz_1000.tsw" under C:\Program Files\Texas Instruments\High Speed Data Converter Pro\1400 Details\Testfiles. The data rate of the file selected will depend on the sampling rate and interpolation ratio of the DAC configuration.
5. Enter 307.2M for the "Data Rate" and 2's complement for the "DAC Option".
6. Select Hanning for "Window".
7. In the “DAC Selection” panel on the left side of the GUI, click on “Send” to load the data into memory.
8. **Toggle the SIF SYNC button of the DAC348x EVM GUI to synchronize the appropriate digital blocks, if the example file with NCO setting is used.**
9. Verify the spectrum using the Spectrum Analyzer at the four IF outputs of the DAC348x EVM (J7, J6, J3, and J2).
   - For the DAC3482 EVM, the IF outputs are at the J6 and J3 SMA connector
10. The expect results are shown in Figure 13 (NCO enabled at 30MHz) and Figure 14 (NCO disabled).



(baseband = 30MHz, NCO = 30MHz with NCO Gain disabled, QMC Gain = 1446)

Figure 13. DAC348x Transformer Coupled Output at 60MHz IF



(baseband = 30MHz, NCO disabled, QMC Gain = 1024)

Figure 14. DAC348x Transformer Coupled Output at 30MHz IF

4 Basic Test Procedure with TSW3100

This section outlines the basic test procedure for testing the EVM with TSW3100.

4.1 TSW3100 Overview

The TSW3100 is a high speed pattern generator board. The LVDS Bus rate is limited to 1.25GSPS, and this limits the maximum input data rate per channel of DAC34SH84 to 625MSPS. To evaluate the DAC34SH84 at 1.5GSPS DAC sampling rate, 4x or higher interpolation filter must be enabled. To evaluate the DAC34SH84 at 1.5GSPS DAC sampling rate with 2x interpolation filter (i.e. 750MSPS of input data rate per channel), the TSW1400 must be used.

See the TSW3100 user's guide (SLLU101) for more detailed explanations of the TSW3100 setup and operation. This document assumes that the TSW3100 software is installed and functioning properly. The TSW30SH84 needs TSW3100 operating software version 2.5 or higher with TSW3100 board Rev D (or higher).

The DAC348xEVM sends the FPGA reference clock to the FPGA of the TSW3100EVM in LVDS format. Therefore, a 100-Ω LVDS termination resistor is needed at the TSW3100 FPGA clock input. All the latest TSW3100EVMs from TI have the 100-Ω termination installed at the bottom side of the board on pins T31 and T32 of the FPGA. Contact TI Application Support if the 100-Ω termination is missing and assistance is needed for the 100-Ω installation.

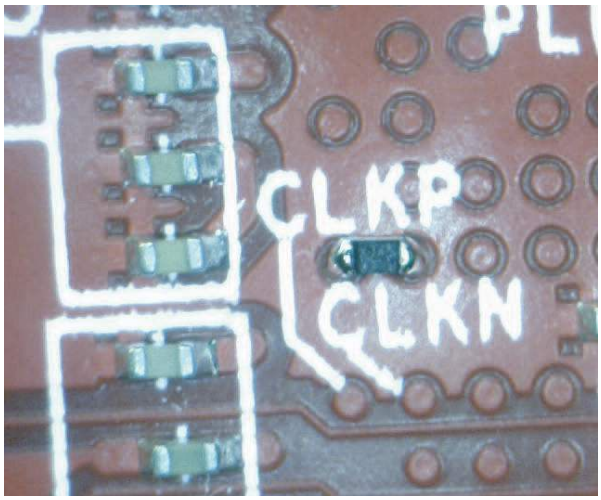


Figure 15. TSW3100 FPGA Clock 100-Ω LVDS Termination at Pins T31 and T32 of the FPGA

Test Block Diagram for TSW3100

The test setup for general testing of the DAC348x with the TSW3100 pattern generation card is shown in Figure 16.

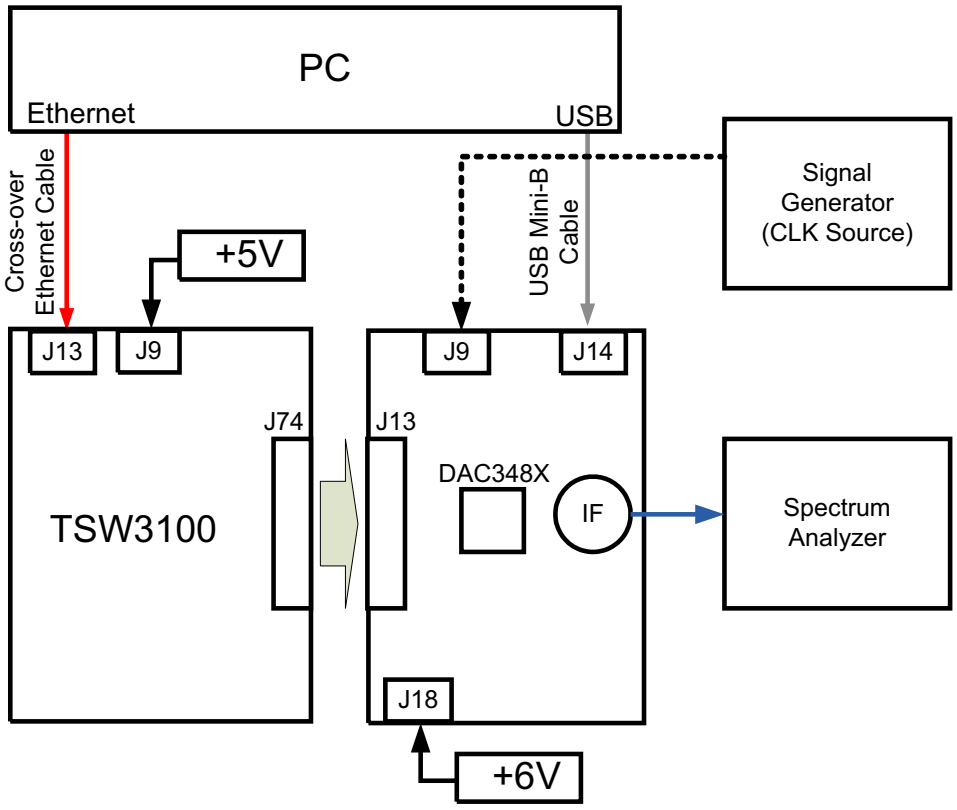


Figure 16. Test Setup Block Diagram for TSW3100

4.2 Test Setup Connection

- TSW3100 Pattern Generator
  1. Connect the EVM-supplied 18-AWG wires to the DC plug cable (Tensility 10-01776) to a qualified lab bench power supply. The 18-AWG red wire is the 5-V wire while the 18-AWG black wire is the ground wire.
  2. Connect a 5-V power supply cable to J9, the *5V_IN* jack of the TSW3100 EVM.
  3. Connect the PC's Ethernet port to J13, *Ethernet* port of the TSW3100. The cable should be a standard cross-over Cat5e Ethernet cable.
- DAC348x EVM
  1. Connect J13 connector of DAC348x EVM to J74 connector of TSW3100EVM.
  2. See the Test Setup Connection section.

4.3 DAC348x Example Setup Procedure

See the DAC348x Example Setup Procedure section.

4.4 TSW3100 Example Setup Procedure

Reference the TSW3100 User's Guide (SLWU079) for more detailed explanations of the TSW3100 setup and operation. This document assumes the TSW3100 software is installed and functioning properly. *The DAC348x needs TSW3100 operating software version 2.5 or higher with TSW3100 board Rev D (or higher).*

CommsSignalPattern Setup from Default Configuration (WCDMA)

- Change Interpolation value to DAC Clock Rate / Interpolation / 3.84 (i.e. **1228.8** / **4**/ **3.84 = 80**)
- Enter desired Offset Frequency (i.e. 30 MHz) for each desired carrier

- Select the **16b QDAC** output button for DAC3484 (see Figure 17) or **LVDS** output button for DAC3482, DAC34H84, and DAC34SH84 (see Figure 18).
- Check the “LOAD and Run” box
- Press the green“Create” button
- **Toggle the SIF SYNC button of the DAC348x EVM GUI to synchronize the appropriate digital blocks, if the example file with NCO setting is used.**
- Verify the spectrum using the Spectrum Analyzer at the four IF outputs of the DAC348x EVM (J7, J6, J3, and J2).
  - For the DAC3482 EVM, the IF outputs are at the J6 and J3 SMA connector
- The expect results are shown in Figure 13 (NCO enabled at 30MHz) and Figure 14 (NCO disabled).

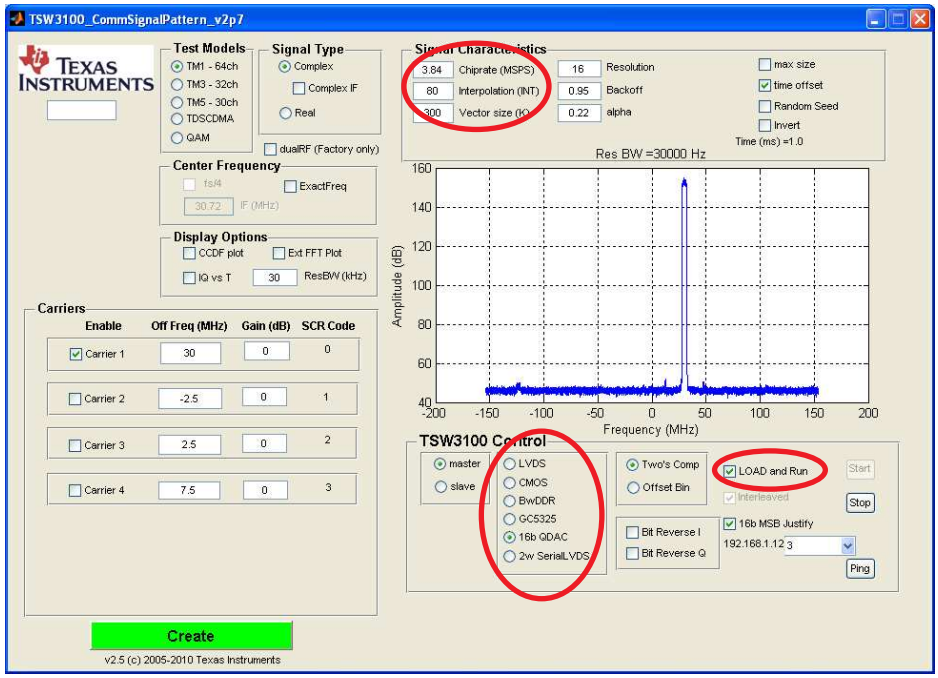


Figure 17. TSW3100 CommSignalPattern (WCDMA) Programming GUI for DAC3484

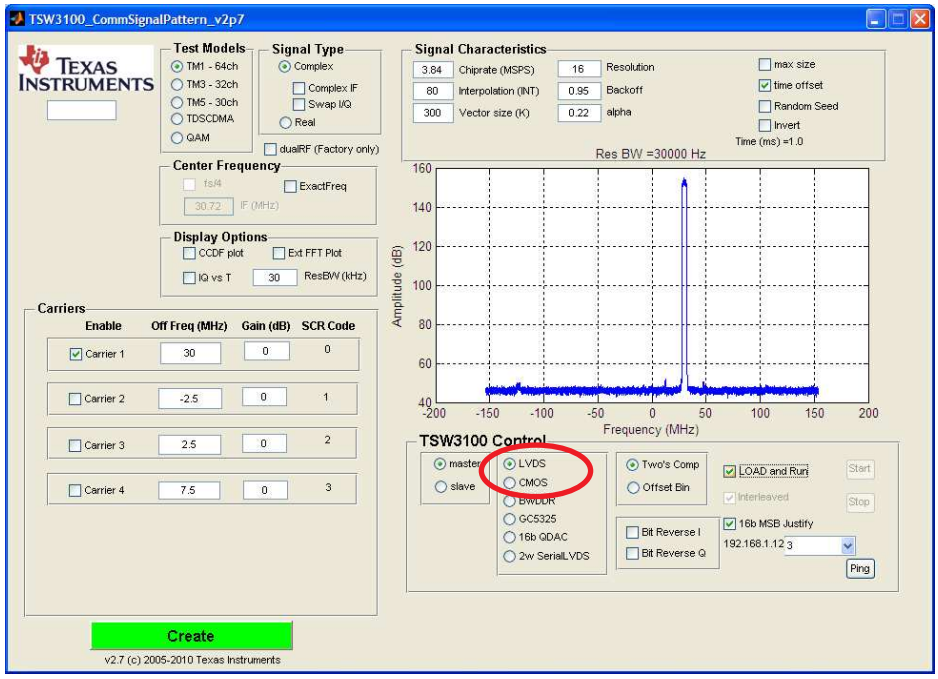


Figure 18. TSW3100 CommSignalPattern (WCDMA) Programming GUI for DAC3482, DAC34H84, and DAC34SH84

References

Related Products From Texas Instruments

Dual-Channel, 16-Bit, 1.25 GSPS Digital-To-Analog Converter (DAC), DAC3482 (SLAS748)

Quad-Channel, 16-Bit, 1.25 GSPS Digital-To-Analog Converter (DAC), DAC3484 (SLAS749)

Quad-Channel, 16-Bit, 1.25 GSPS Digital-To-Analog Converter (DAC), DAC34H84 (SLAS751)

Quad-Channel, 16-Bit, 1.5 GSPS Digital-to-Analog Converter (DAC) , DAC34SH84 (SLAS808)

Five/Ten Output Clock Generator/Jitter Cleaner With Integrated Dual VCO, CDCE62005 (SCAS862)

Related Tools From Texas Instruments

TSW1400 High Speed Data Capture/Pattern Generator Card (SLWU079)

TSW3100 High Speed Digital Pattern Generator (SLUU101)

FMC-DAC-ADAPTER Physical Design Database Rev D Board (SLOR102)

DAC34H84EVM Design Package board rev C (SLAC518)

DAC348x EVM Software (SLAC483)

High Speed Data Converter Pro software (SLWC107)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2012) to A Revision	Page
• Changed information regarding power supplies and connections in the TSW1400 *Test Setup Connection* section.	12
• Changed information regarding power supplies and connections in the DAC348xEVM *Test Setup Connection* section.	12
• Changed information regarding power supplies and connections in the TSW3100 *Test Setup Connection* section.	17

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS AND CONDITIONS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT MADE, CONCEIVED OR ACQUIRED PRIOR TO OR AFTER DELIVERY OF THE EVM.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS ANDCONDITIONS OR THE USE OF THE EVMS PROVIDED HEREUNDER, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY WARRANTY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS AND CONDITIONS, OR ANY USE OF ANY TI EVM PROVIDED HEREUNDER, EXCEED THE TOTAL AMOUNT PAID TO TI FOR THE PARTICULAR UNITS SOLD UNDER THESE TERMS AND CONDITIONS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM AGAINST THE PARTICULAR UNITS SOLD TO USER UNDER THESE TERMS AND CONDITIONS SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy*. Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265