



# N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)	
100	0.0183 at V <sub>GS</sub> = 10 V	60	48	
	0.023 at V <sub>GS</sub> = 8.0 V	53	40	

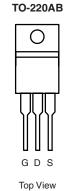
### **FEATURES**

- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



### **APPLICATIONS**

- Industrial
- Power Supply



Ordering Information: SUP60N10-18P-E3 (Lead (Pb)-free)

G S

N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b>	$T_C = 25  ^{\circ}C$ , unless oth	erwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	100	V		
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
Continuous Drain Current (T <sub>.I</sub> = 175 °C)	T <sub>C</sub> = 25 °C	1-	60	A	
Continuous Diam Current (1j = 173 O)	T <sub>C</sub> = 70 °C	l <sub>D</sub>	50		
Pulsed Drain Current		I <sub>DM</sub>	100	7 ^	
Avalanche Current		I <sub>AS</sub>	45		
Single Avalanche Energy <sup>a</sup>	Avalanche Energy <sup>a</sup> L = 0.1 mH		101	mJ	
Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	В	150 <sup>b</sup>	W	
	T <sub>A</sub> = 25 °C <sup>c</sup>	$ P_D$	3.75	VV	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W	
Junction-to-Case (Drain)	R <sub>thJC</sub>	1.0	- C/VV	

### Notes:

- a. Duty cycle  $\leq$  1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).

## SUP60N10-18P

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	100			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.5		4.5	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 250	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	μΑ
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	50			Α
Drain-Source On-State Resistance <sup>a</sup>		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.015	0.0183	Ω
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A, T <sub>J</sub> = 125 °C		0.027	0.033	
		V <sub>GS</sub> = 8.0 V, I <sub>D</sub> = 10 A		0.018	0.023	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		33		S
Dynamic <sup>b</sup>	•			1		
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V, f = 1 MHz		2600		pF
Output Capacitance	C <sub>oss</sub>			230		
Reverse Transfer Capacitance	C <sub>rss</sub>			80		
Total Gate Charge <sup>c</sup>	$Q_g$			48	75	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A}$		16		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			13		
Gate Resistance	$R_{g}$	f = 1 MHz	0.25	1.1	2.4	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			12	20	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, R_{L} = 1.0 \Omega$		10	20	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		18	35	
Fall Time <sup>c</sup>	t <sub>f</sub>			8	15	
Drain-Source Body Diode Character	stics T <sub>C</sub> = 25	°Cp				
Continuous Current	Is				60	А
Pulsed Current	I <sub>SM</sub>				100	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0 V		0.85	1.5	V
Reverse Recovery Time	t <sub>rr</sub>			80	120	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	I <sub>F</sub> = 50 A, dl/dt = 100 A/μs		4		Α
Reverse Recovery Charge	Q <sub>rr</sub>	·		160	240	nC

### Notes:

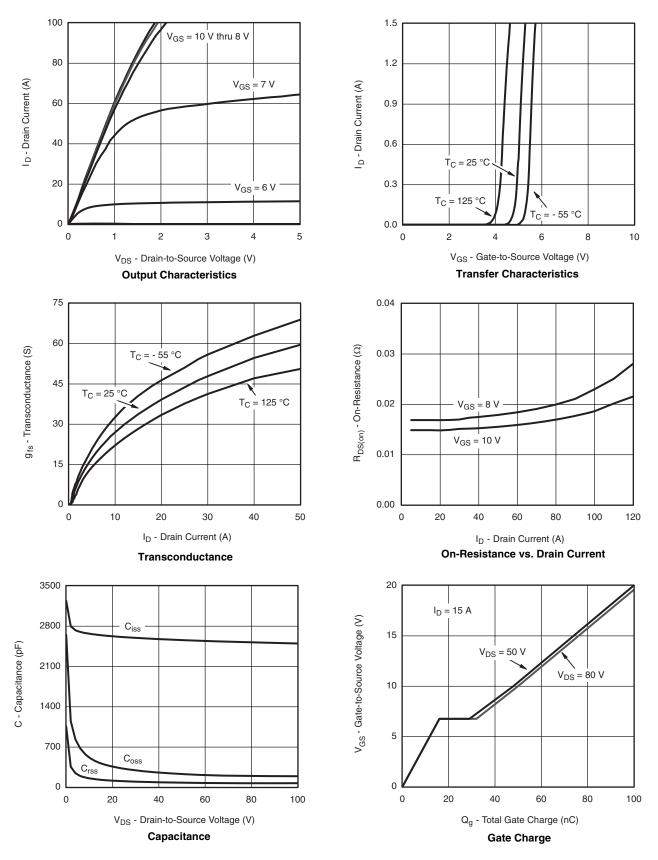
- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



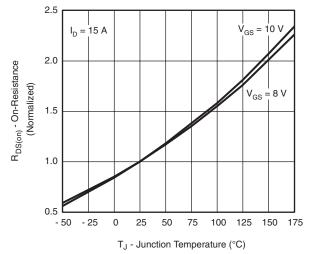


### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

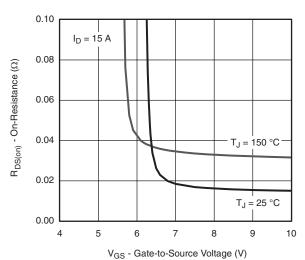


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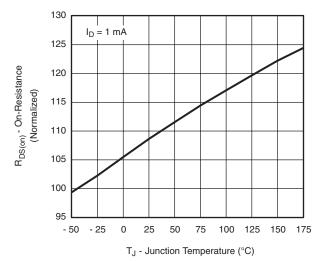
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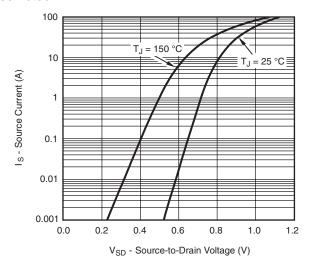
On-Resistance vs. Junction Temperature



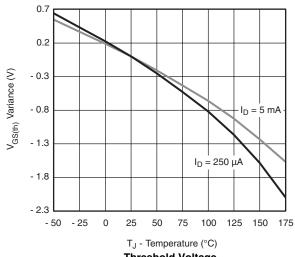
On-Resistance vs. Gate-to-Source Voltage



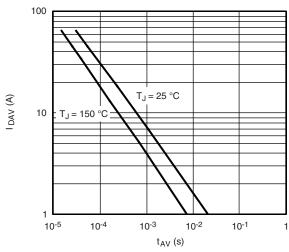
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

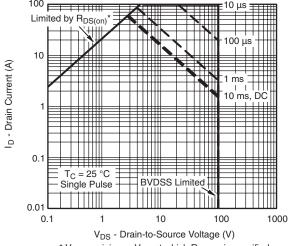


**Threshold Voltage** 



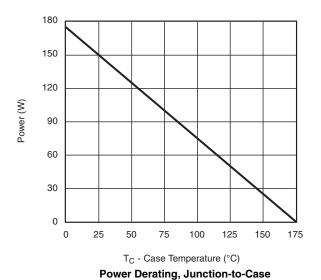
Avalanche Current vs. Time

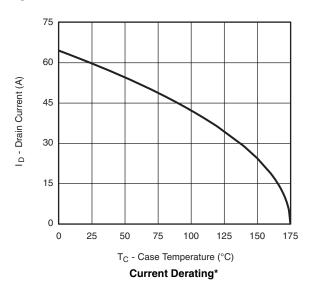
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



\*  $V_{GS} > \mbox{ minimum } V_{GS}$  at which  $R_{DS(on)}$  is specified

### Safe Operating Area



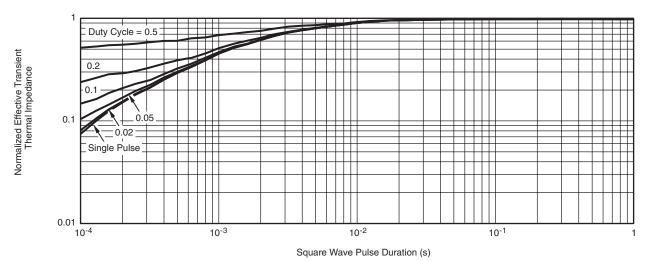


 $<sup>^{\</sup>star}$  The power dissipation  $P_D$  is based on  $T_{J(max.)}$  = 175  $^{\circ}$ C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package

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### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?65003">www.vishay.com/ppg?65003</a>.



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