

## Evaluating the **ADA4098-1** 50 V, 1 MHz, 165 $\mu$ A, Robust, Over-The-Top Precision Op Amp

### FEATURES

**Fully featured evaluation board for the ADA4098-1**  
**Enables efficient prototyping**  
**User defined circuit configuration**  
**Simplified connection to test equipment and other circuits**

### EVALUATION KIT CONTENTS

**EVAL-ADA4098-1HUJZ**

### EQUIPMENT NEEDED

**Dual-output dc power supply**  
**Dual-channel signal generator**  
**Oscilloscope**  
**Banana jack to grabber cables**  
**BNC to SMA cables**

### DOCUMENTS NEEDED

**ADA4098-1 data sheet**

### GENERAL DESCRIPTION

The EVAL-ADA4098-1HUJZ evaluates the ADA4098-1 6-lead, thin small outline transistor (TSOT), robust Over-The-Top™ precision operational amplifier (op amp). The EVAL-ADA4098-1HUJZ is a prepopulated board using a gain of 1 configuration.

The EVAL-ADA4098-1HUJZ design allows simplified and efficient use. The EVAL-ADA4098-1HUJZ has edge mounted Subminiature Version A (SMA) connectors on the inputs and outputs to allow efficient connection to test equipment or other circuits. Bulk test points are also incorporated as an alternative option to be used for the inputs and outputs. The optimized EVAL-ADA4098-1HUJZ ground plane, component placement, and power supply allow maximum circuit flexibility and performance. The EVAL-ADA4098-1HUJZ combines surface-mount technology (SMT) with almost all 0805 size components to provide simplified installation and the option to replace and solder when needed, except for the bypass capacitors (C1 to C4) that are fixed 0603 sized. The EVAL-ADA4098-1HUJZ also has unpopulated resistor and capacitor pads that provide the user with options and flexibility to implement different application circuits and configurations.

Figure 1 shows the primary side of the EVAL-ADA4098-1HUJZ, and Figure 2 shows the secondary side of the EVAL-ADA4098-1HUJZ.

### EVALUATION BOARD PHOTOGRAPHS



Figure 1. EVAL-ADA4098-1HUJZ, Primary Side

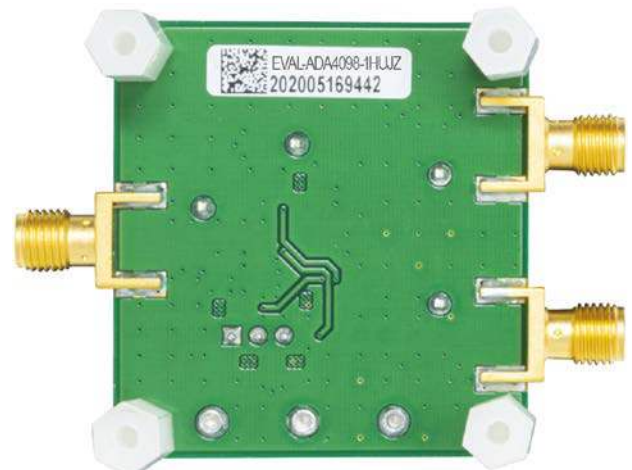


Figure 2. EVAL-ADA4098-1HUJZ, Secondary Side

Refer to the ADA4098-1 data sheet for full specifications, details on device operation, and application circuit configurations. Consult the data sheet in conjunction with this user guide when using the EVAL-ADA4098-1HUJZ.

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**REVISION HISTORY**

3/2021—Revision 0: Initial Version

## EVALUATION BOARD QUICK START PROCEDURES

The Power Supply Consideration section, the Initial Board Configuration section, and the Using the Evaluation Board for Testing section outline the basic, prepopulated EVAL-ADA4098-1HUIZ configuration required to test the basic functionality of the device.

### POWER SUPPLY CONSIDERATION

Use the turret pins (VS+, VS–, and GND) to power up the EVAL-ADA4098-1HUIZ. Ensure that the correct polarity and voltage level is used to avoid reverse polarity and overvoltage, which can permanently damage the EVAL-ADA4098-1HUIZ. The operating supply voltage range is 3 V to 50 V. Higher voltages can damage the amplifier. Decoupling capacitors of 10  $\mu$ F and 0.1  $\mu$ F are preinstalled on the EVAL-ADA4098-1HUIZ for ready operation.

### INITIAL BOARD CONFIGURATION

To set up the initial EVAL-ADA4098-1HUIZ configuration, perform the following steps:

1. Ensure that all equipment is powered down, including the power supply and the signal generator. Use the banana jack to grabber cables to connect the positive supply, ground, and negative supply to the VS+, VS–, and GND turret pins, respectively.
2. Verify that the P1 jumper for the SHDN pin on the EVAL-ADA4098-1HUIZ is in Position 1 (ENABLE) so that the device is enabled.
3. Connect the signal generator at the IN+ SMA pad using a Bayonet Neill-Concelman (BNC) to SMA cable or at the IN+ bulk test point and GND turret using a BNC to grabber cable.
4. Connect VOUT on the EVAL-ADA4098-1HUIZ to the oscilloscope using a BNC to SMA cable or connect an oscilloscope probe with a 10 $\times$  attenuation factor to the VOUT bulk test point and clip the ground of the oscilloscope probe with a 10 $\times$  attenuation factor to the GND turret pin.

### USING THE EVALUATION BOARD FOR TESTING

When the procedure in the Initial Board Configuration section is complete, implement the following settings and verify the expected output:

1. Set the power supply to +15 V for the positive supply and –15 V for the negative supply, and then turn on the power supply.
2. Configure the signal generator to output a 100 Hz sine wave with 0 V offset and 1 V p-p, and enable the generator.
3. Set the oscilloscope scaling to 200 mV/2 ms per division. If using a 10 $\times$  probe instead of a BNC to SMA cable to monitor VOUT, set the oscilloscope input impedance to 1 M $\Omega$ , and the oscilloscope probe setting attenuation factor to 10 $\times$ . Ensure that a 100 Hz, 1 V p-p sine wave centered at 0 V appears on the oscilloscope.
4. To evaluate the device shutdown performance, move the P1 jumper into Position 3 (DISABLE) to tie SHDN to VS+. There is no output at the VOUT SMA pad or bulk test point. To re-enable the device, move the P1 jumper back into Position 1 (ENABLE).

EVALUATION BOARD SCHEMATICS AND ARTWORK

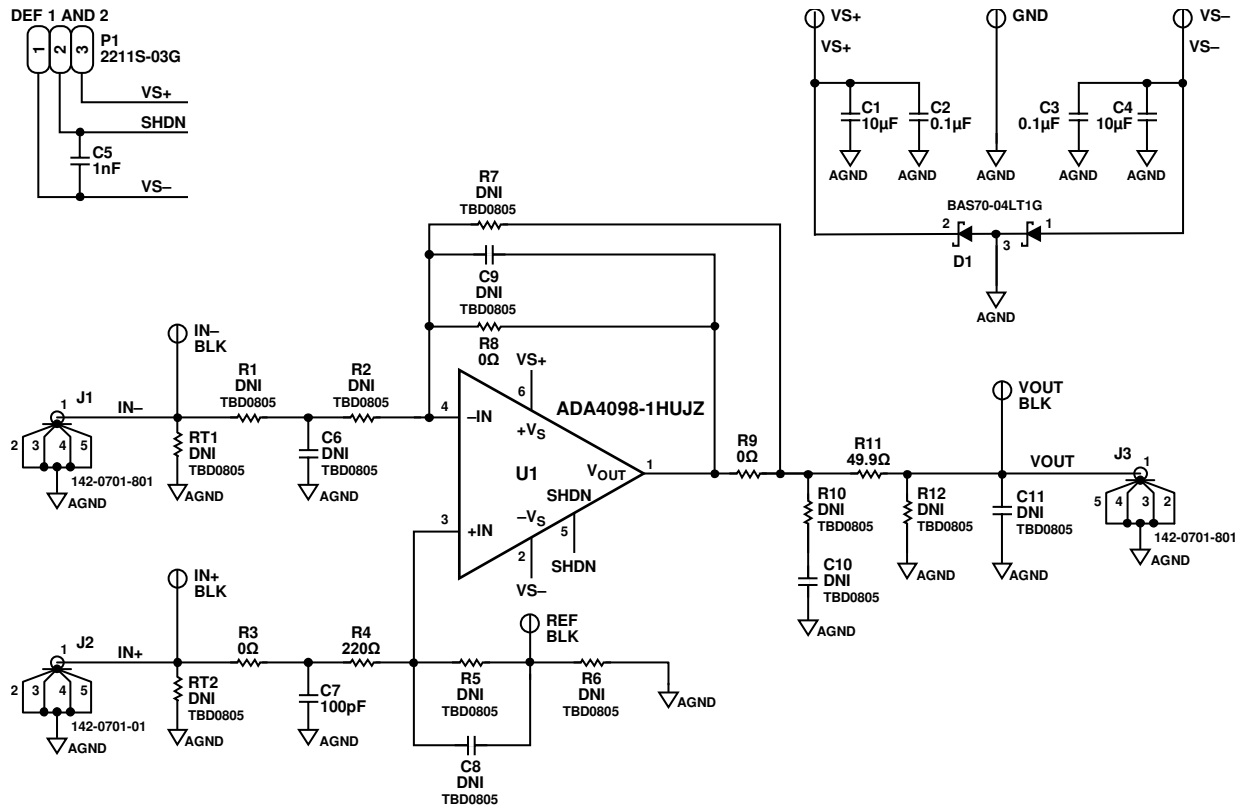


Figure 3. EVAL-ADA4098-1HUJZ Schematic

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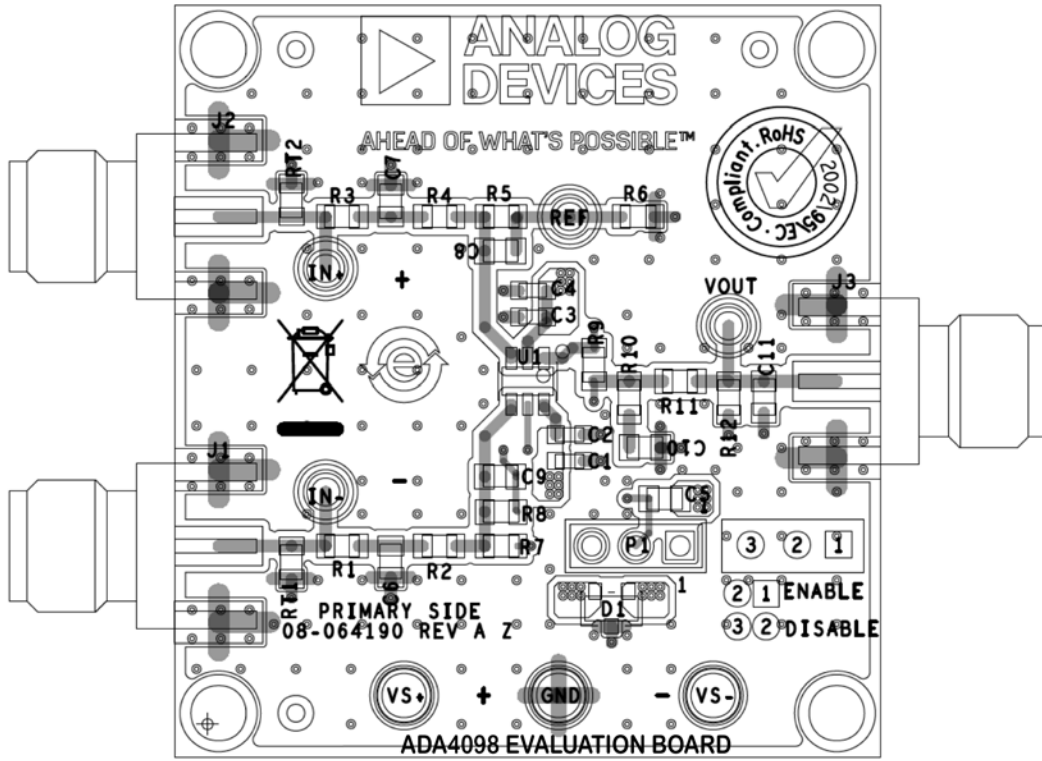


Figure 4. EVAL-ADA4098-1HUJZ Layout Pattern, Primary Side

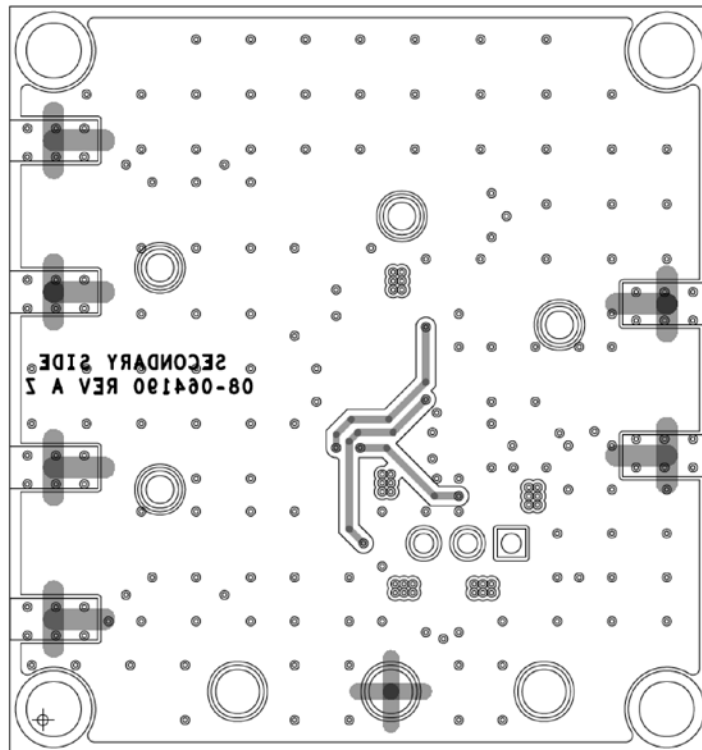


Figure 5. EVAL-ADA4098-1HUJZ Layout Pattern, Secondary Side

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 1.

| Qty | Reference Designator                 | Description  | Supplier             | Part Number             |
|-----|--------------------------------------|--|----------------------|-------------------------|
| 1   | U1                                   | 50 V, 1 MHz, 165 $\mu$ A, robust Over-The-Top precision op amp | Analog Devices       | ADA4098-1HUJZ           |
| 2   | C1, C4                               | Ceramic capacitors, X5R, 0603, 10 $\mu$ F                      | Murata               | GRM188R61E106KA73D      |
| 2   | C2, C3                               | Ceramic capacitors, X7R, 0603, 0.1 $\mu$ F                     | Kemet                | C0603C104K3RACTU        |
| 1   | C5                                   | Ceramic capacitors, X7R, 0805, 1 nF                            | Wurth Elektronik     | 885012207007            |
| 1   | C7                                   | Ceramic capacitors, X7R, 0805, 100 nF                          | AVX                  | 08051A101JAT2A          |
| 5   | C6, C8 to C11                        | Capacitors, 0805, do not install (DNI), user defined           | Not applicable       | Not applicable          |
| 1   | D1                                   | Diode Schottky barrier   | ON Semiconductor     | BAS70-04LT1G            |
| 3   | GND, VS+, VS-                        | Printed circuit board (PCB) connector, terminal turrets        | Mill-Max             | 2501-2-00-80-00-00-07-0 |
| 4   | IN+, IN-, REF, VOUT                  | PCB connector, bulk test points                                | Keystone Electronics | 5006                    |
| 3   | J1, J2, J3                           | Coax SMA end launch  | Cinch                | 142-0701-801            |
| 1   | P1                                   | PCB connector, 3-position, male header                         | Multicomp (SPC)      | 2211S-03G               |
| 1   | R4                                   | Resistor, 220 $\Omega$   | Multicomp (SPC)      | MC 0.1 W 0805 1% 220R.  |
| 1   | R11                                  | Resistors, 49.9 $\Omega$                                       | Panasonic            | ERA-6AEB49R9V           |
| 9   | R1, R2, R5 to R7, R10, R12, RT1, RT2 | Resistors, 0805, DNI, user defined                             | Not applicable       | Not applicable          |
| 3   | R3, R8, R9                           | Resistors, 0 $\Omega$  | Vishay               | CRCW08050000Z0EA        |

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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