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Kind regards,

Team Nexperia

# DATA SHEET

## **PDTA144W series**

PNP resistor-equipped transistors;

R1 = 47 k $\Omega$ , R2 = 22 k $\Omega$

Product data sheet  
Supersedes data of 2004 Mar 23

2004 Aug 05

## PNP resistor-equipped transistors; R1 = 47 k $\Omega$ , R2 = 22 k $\Omega$

## PDTA144W series

### FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

### APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	–	–50	V
I <sub>O</sub>	output current (DC)	–	–100	mA
R1	bias resistor	47	–	k $\Omega$
R2	bias resistor	22	–	k $\Omega$

### DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

### PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA144WE	SOT416	SC-75	5D	PDTC144WE
PDTA144WEF	SOT490	SC-89	2E	PDTC144WEF
PDTA144WK	SOT346	SC-59	46	PDTC144WK
PDTA144WM	SOT883	SC-101	F8	PDTC144WM
PDTA144WS	SOT54 (TO-92)	SC-43	TA144W	PDTC144WS
PDTA144WT	SOT23	–	*43 <sup>(1)</sup>	PDTC144WT
PDTA144WU	SOT323	SC-70	*28 <sup>(1)</sup>	PDTC144WU

### Note

1. \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.  
\* = W: Made in China.

PNP resistor-equipped transistors;  
 R1 = 47 kΩ, R2 = 22 kΩ

PDTA144W series

**SIMPLIFIED OUTLINE, SYMBOL AND PINNING**

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA144WS		1 2 3	base collector emitter
PDTA144WE PDTA144WEF PDTA144WK PDTA144WT PDTA144WU		1 2 3	base emitter collector
PDTA144WM		1 2 3	base emitter collector

PNP resistor-equipped transistors;  
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PDTA144W series

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTA144WE	–	plastic surface mounted package; 3 leads	SOT416
PDTA144WEF	–	plastic surface mounted package; 3 leads	SOT490
PDTA144WK	–	plastic surface mounted package; 3 leads	SOT346
PDTA144WM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm	SOT883
PDTA144WS	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTA144WT	–	plastic surface mounted package; 3 leads	SOT23
PDTA144WU	–	plastic surface mounted package; 3 leads	SOT323

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CB0</sub>	collector-base voltage	open emitter	–	–50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	–50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	–10	V
V <sub>I</sub>	input voltage positive negative		–	+10	V
			–	–40	V
I <sub>O</sub>	output current (DC)		–	–100	mA
I <sub>CM</sub>	peak collector current		–	–100	mA
P <sub>tot</sub>	total power dissipation SOT54 SOT23 SOT346 SOT323 SOT416 SOT490 SOT883	T <sub>amb</sub> ≤ 25 °C; note 1	–	500	mW
		note 1	–	250	mW
		note 1	–	250	mW
		note 1	–	200	mW
		note 1	–	150	mW
		notes 1 and 2	–	250	mW
		notes 2 and 3	–	250	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

## Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60  $\mu$ m copper strip line.

PNP resistor-equipped transistors;  
R1 = 47 k $\Omega$ , R2 = 22 k $\Omega$

PDTA144W series

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	T <sub>amb</sub> ≤ 25 °C		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	830	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W

#### Note

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions.; FR4 with 60  $\mu$ m copper strip line.

### CHARACTERISTICS

T<sub>amb</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -50 V; I <sub>E</sub> = 0 A	-	-	-100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A	-	-	-1	$\mu$ A
		V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	-50	$\mu$ A
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A	-	-	-110	$\mu$ A
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -5 mA	60	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -10 mA; I <sub>B</sub> = -0.5 mA	-	-	-150	mV
V <sub>i(off)</sub>	input-off voltage	I <sub>C</sub> = -100 $\mu$ A; V <sub>CE</sub> = -5 V	-	-1.7	-1.2	V
V <sub>i(on)</sub>	input-on voltage	I <sub>C</sub> = -2 mA; V <sub>CE</sub> = -0.3 V	-4	-2.7	-	V
R1	input resistor		33	47	61	k $\Omega$
$\frac{R2}{R1}$	resistor ratio		0.37	0.47	0.57	
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = i <sub>e</sub> = 0 A; V <sub>CB</sub> = -10 V; f = 1 MHz	-	-	3	pF

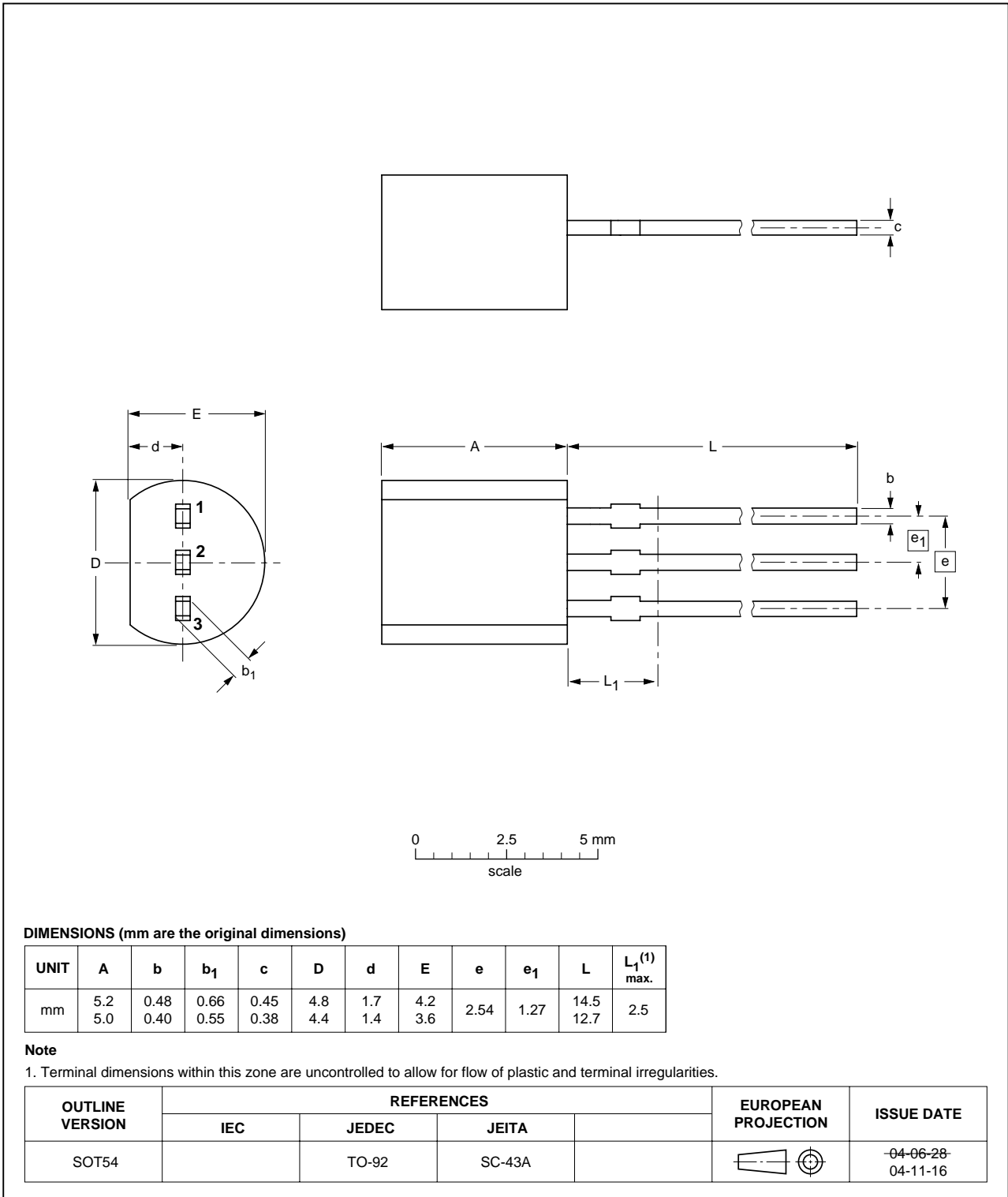
PNP resistor-equipped transistors;  
R1 = 47 kΩ, R2 = 22 kΩ

PDTA144W series

PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

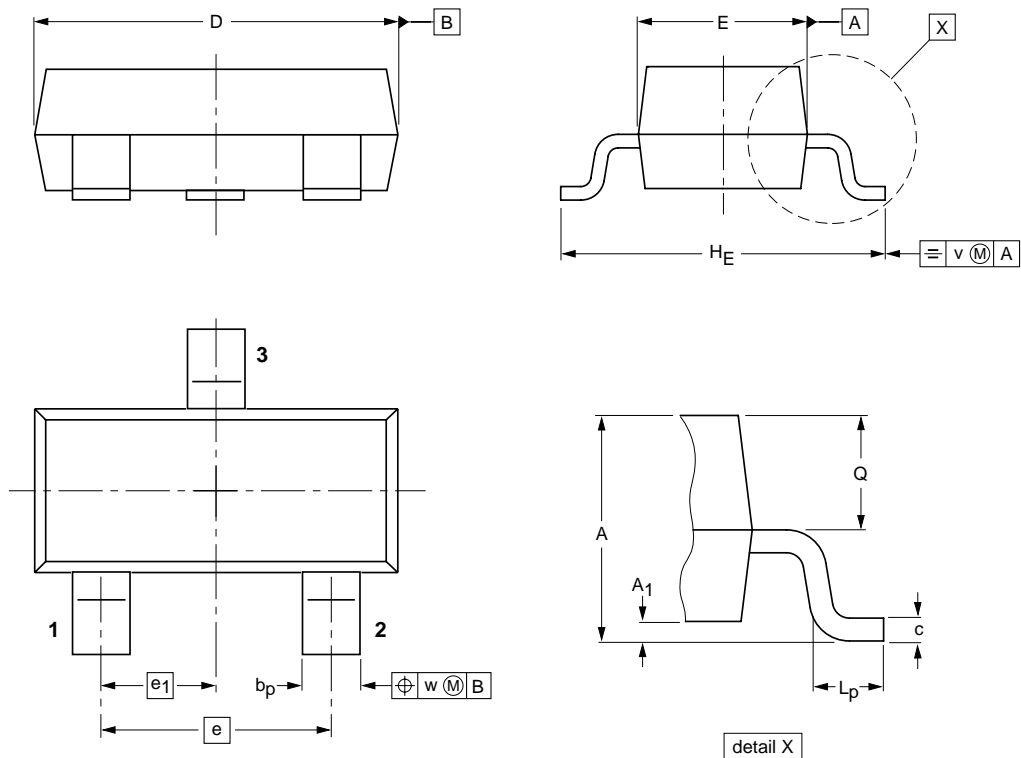


PNP resistor-equipped transistors;  
R1 = 47 kΩ, R2 = 22 kΩ

PDTA144W series

Plastic surface-mounted package; 3 leads

SOT23



**DIMENSIONS** (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max.	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT23		TO-236AB			04-11-04 06-03-16

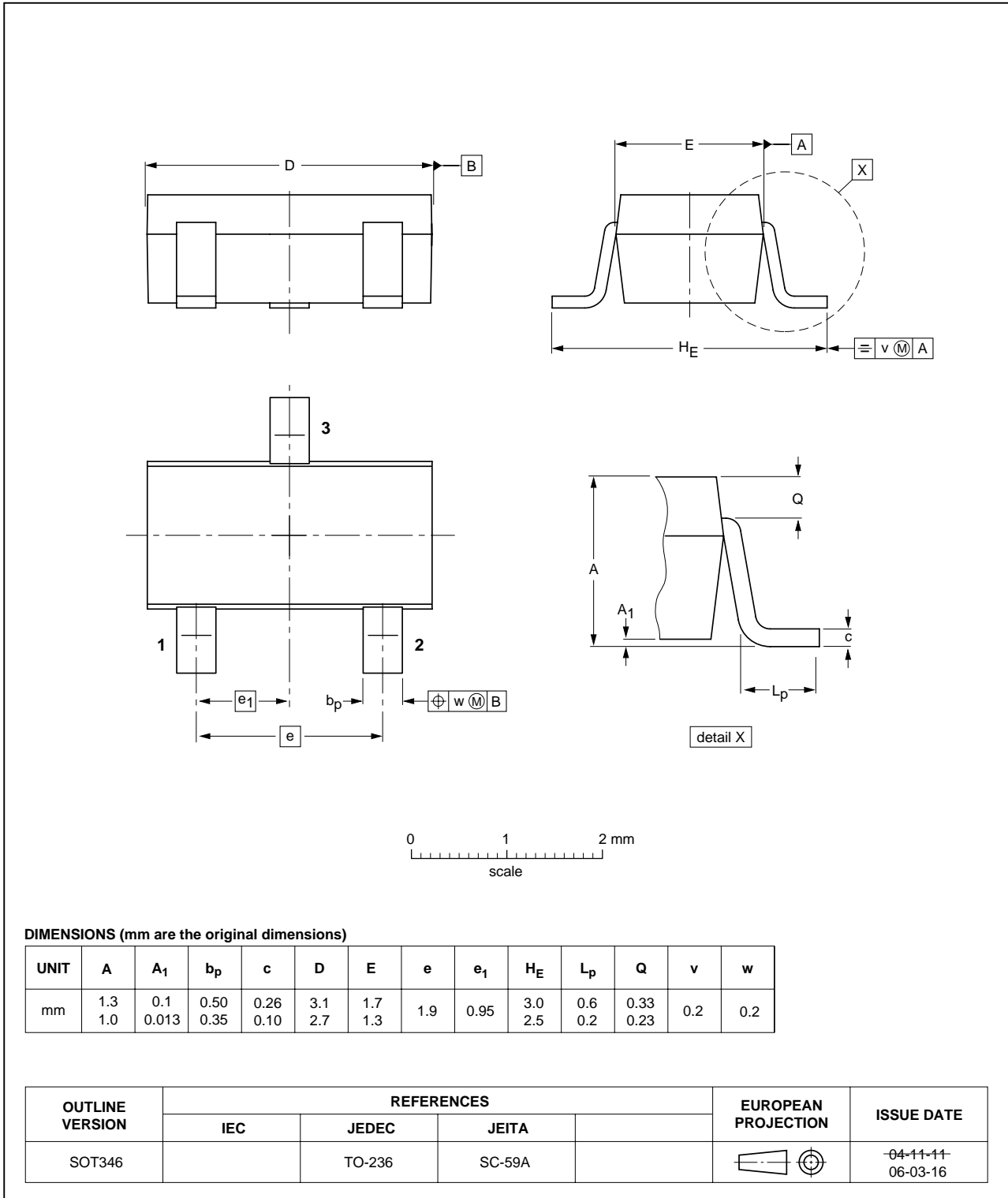


PNP resistor-equipped transistors;  
R1 = 47 kΩ, R2 = 22 kΩ

PDTA144W series

Plastic surface-mounted package; 3 leads

SOT346

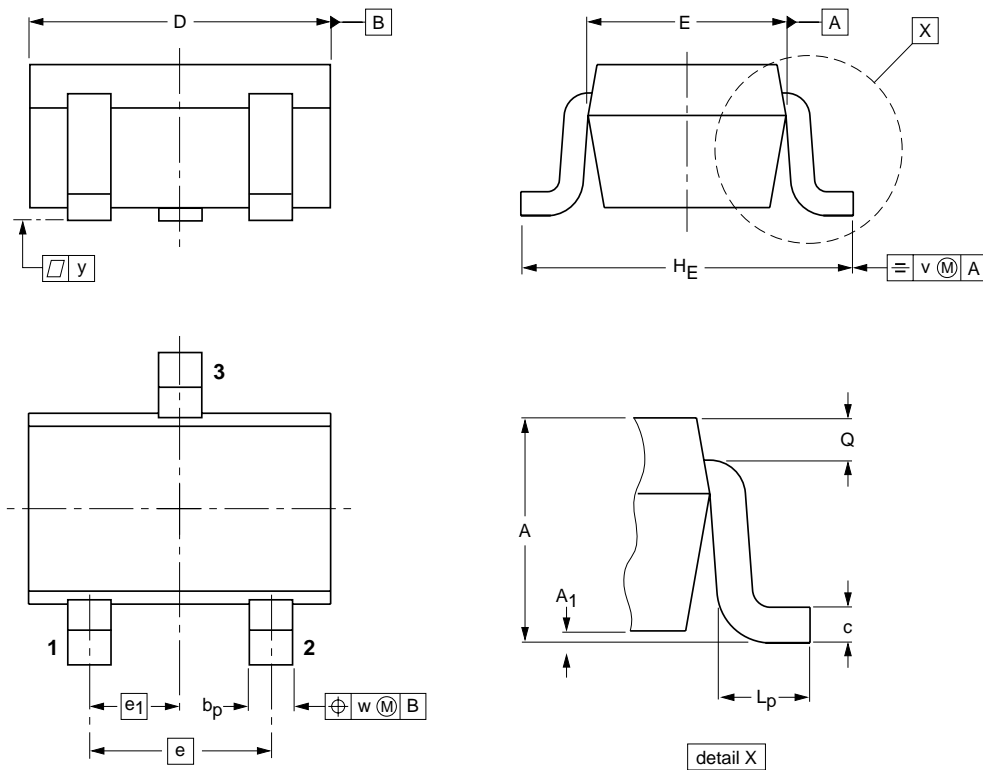


PNP resistor-equipped transistors;  
R1 = 47 kΩ, R2 = 22 kΩ

PDTA144W series

Plastic surface-mounted package; 3 leads

SOT323



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

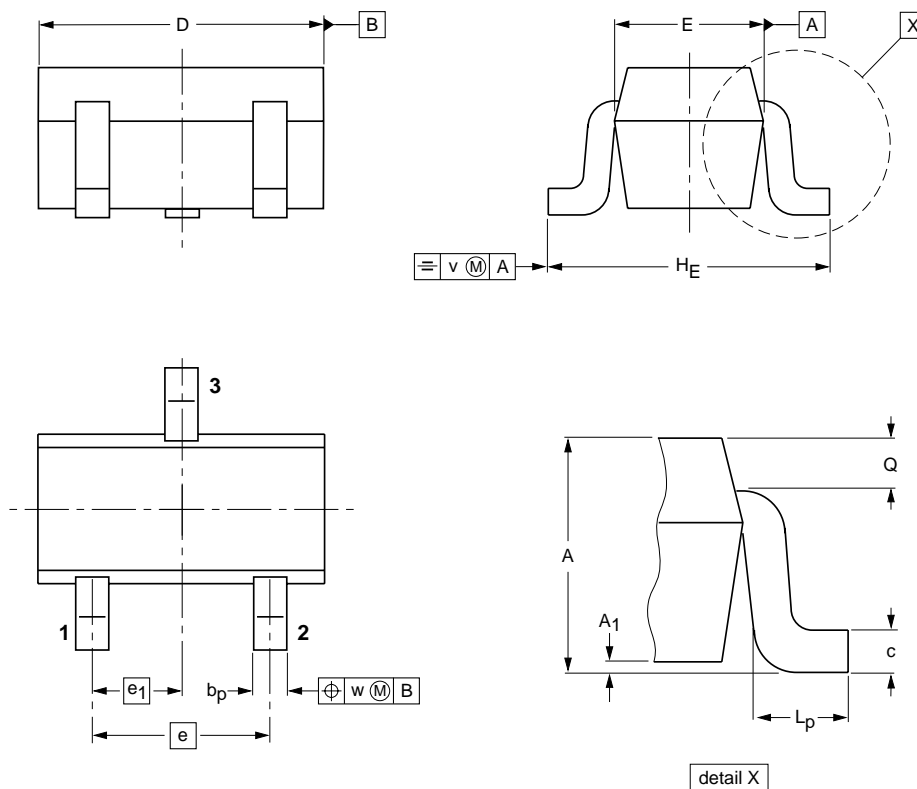
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			<del>04-11-04</del> 06-03-16

PNP resistor-equipped transistors;  
R1 = 47 kΩ, R2 = 22 kΩ

PDTA144W series

Plastic surface-mounted package; 3 leads

SOT416



**DIMENSIONS** (mm are the original dimensions)

UNIT	A	A1 max	bp	c	D	E	e	e1	HE	Lp	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

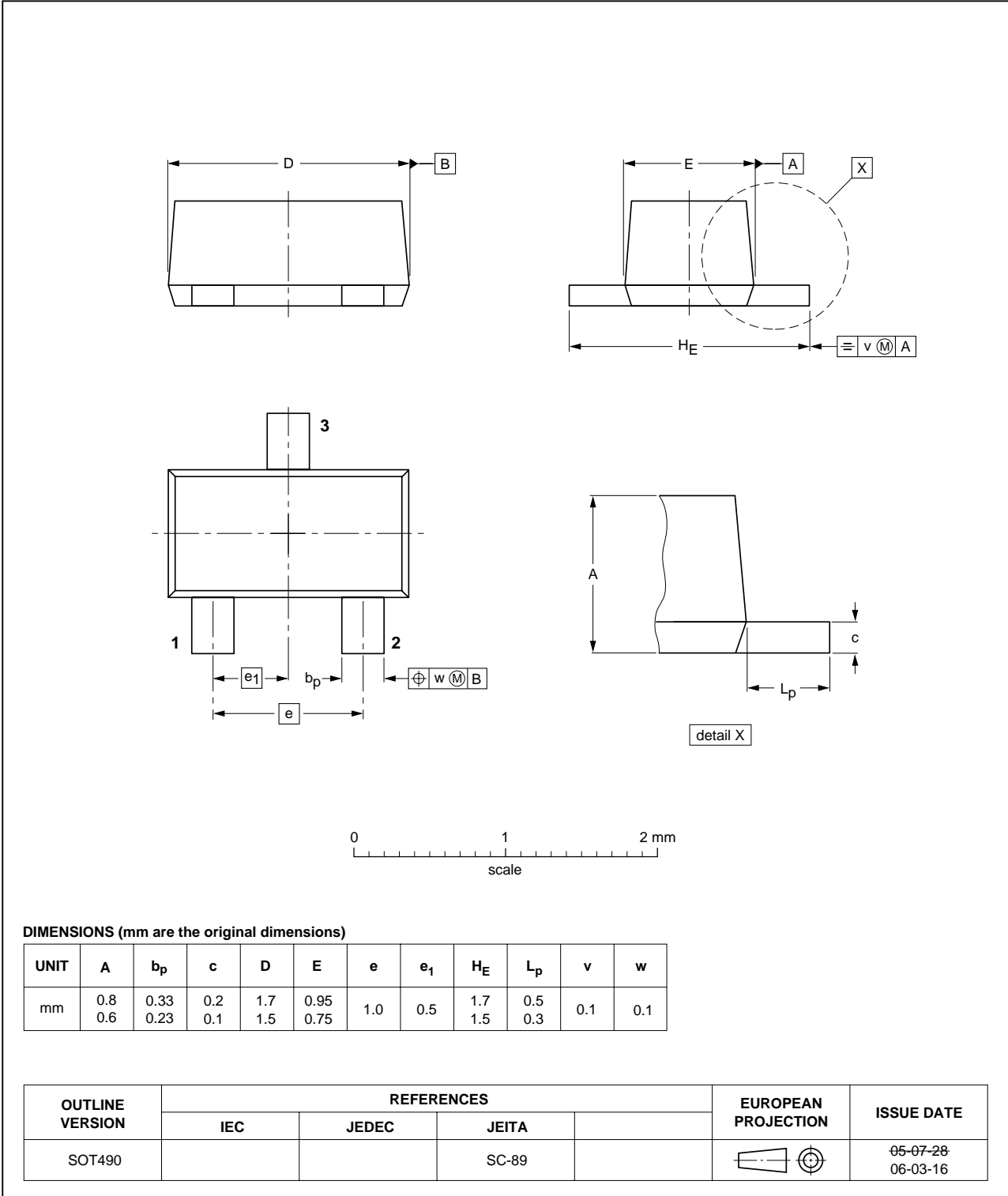
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT416			SC-75		04-11-04 06-03-16

PNP resistor-equipped transistors;  
R1 = 47 kΩ, R2 = 22 kΩ

PDTA144W series

Plastic surface-mounted package; 3 leads

SOT490

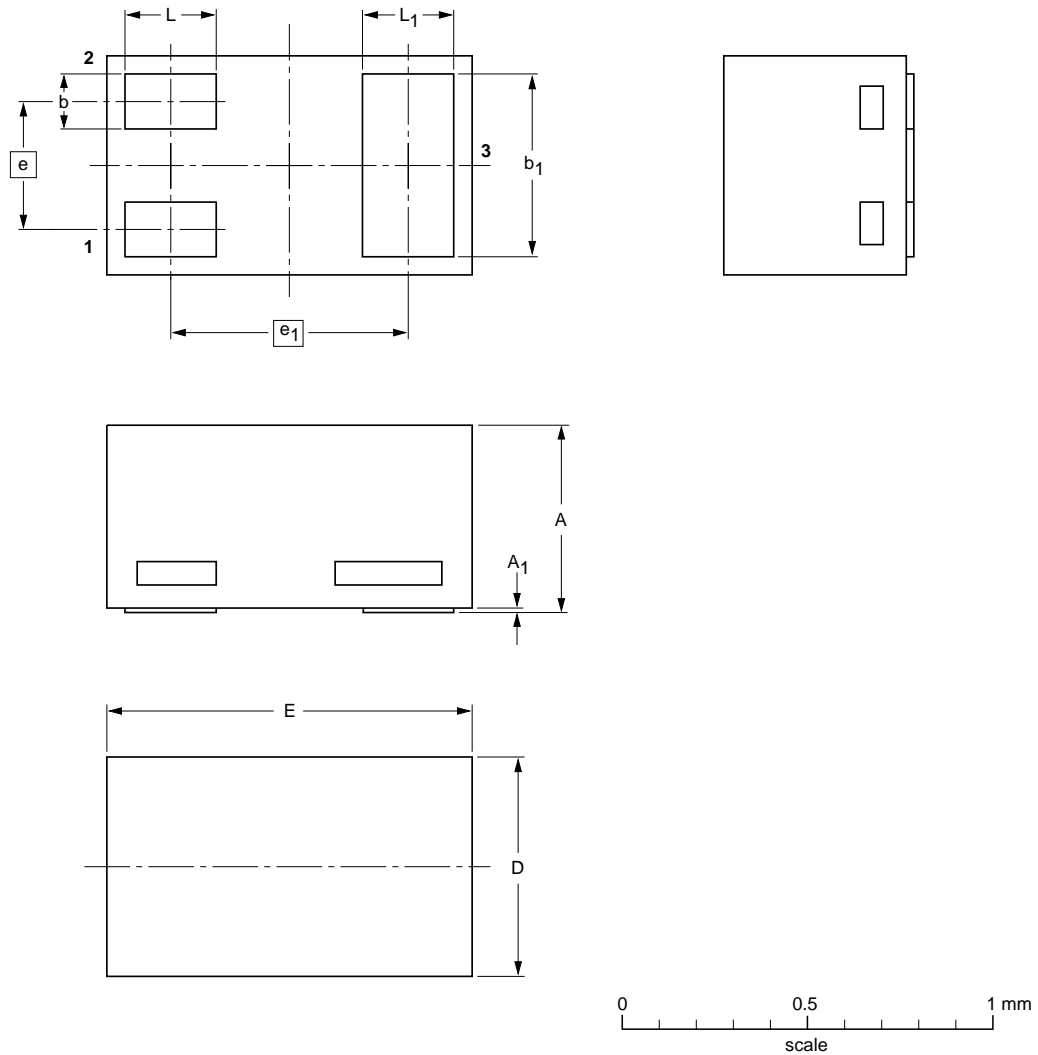


PNP resistor-equipped transistors;  
R1 = 47 kΩ, R2 = 22 kΩ

PDTA144W series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A <sup>(1)</sup>	A <sub>1</sub> max.	b	b <sub>1</sub>	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT883			SC-101		03-02-05 03-04-03

PNP resistor-equipped transistors;  
R1 = 47 k $\Omega$ , R2 = 22 k $\Omega$

PDTA144W series

## DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

## Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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# ***NXP Semiconductors***

## **Customer notification**

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

## **Contact information**

For additional information please visit: <http://www.nxp.com>

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