NSPM1042

ESD and Surge Protection Diode

Features

- Protection for the following IEC Standards:
  IEC61000−4−2 Level 4: ±30 kV Contact Discharge
  IEC61000−4−5 (Lightning) 200 A (8/20 μs)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IEC 61000−4−2 (ESD)	Contact Air		±30 ±30	kV
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−65 to +150	°C
Maximum Peak Pulse Current 8/20 μs @ T_A = 25°C, Pin 2 to Pin 1		I_{PP}	200	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ON Semiconductor®

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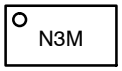
UDFN2
CASE 517DF

MARKING DIAGRAM



N3 = Specific Device Code
M = Date Code

ORDERING INFORMATION

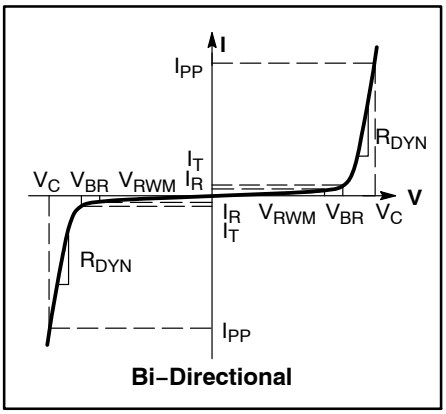
Device	Package	Shipping†
NSPM1042MUTBG	UDFN2 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS
(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	Pin 1 to Pin 2			3.3	V
Reverse Working Voltage	V_{RWM}	Pin 2 to Pin 1			4.8	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, Pin 1 to Pin 2	4.5	4.7	5.5	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, Pin 2 to Pin 1	5.0	5.4	6.0	V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V, Pin 1 to Pin 2		0.05	0.1	μA
Reverse Leakage Current	I_R	V_{RWM} = 4.8 V, Pin 2 to Pin 1		0.05	0.1	μA
Clamping Voltage (Note 1)	V_C	I_{PP} = 100 A, t_p = 8 x 20 μs, Pin 2 to Pin 1		6.6	7.2	V
Clamping Voltage (Note 1)	V_C	I_{PP} = 150 A, t_p = 8 x 20 μs, Pin 2 to Pin 1		7.6	8.4	V
Clamping Voltage (Note 1)	V_C	I_{PP} = 180 A, t_p = 8 x 20 μs, Pin 2 to Pin 1		8.2	9.1	V
Clamping Voltage (Note 1)	V_C	I_{PP} = 200 A, t_p = 8 x 20 μs, Pin 2 to Pin 1		8.8	9.5	V
Clamping Voltage TLP (Note 2)	V_C	I_{PP} = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±8 kV Air)		5.48		V
		I_{PP} = 16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±16 kV Air)		5.55		
Dynamic Resistance	R_{DYN}	TLP Pulse, Pin 1 to Pin 2		0.014		Ω
Dynamic Resistance	R_{DYN}	TLP Pulse, Pin 2 to Pin 1		0.01		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		300	480	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−5 waveform.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 1 ns, averaging window; t_1 = 70 ns to t_2 = 90 ns.

TYPICAL CHARACTERISTICS

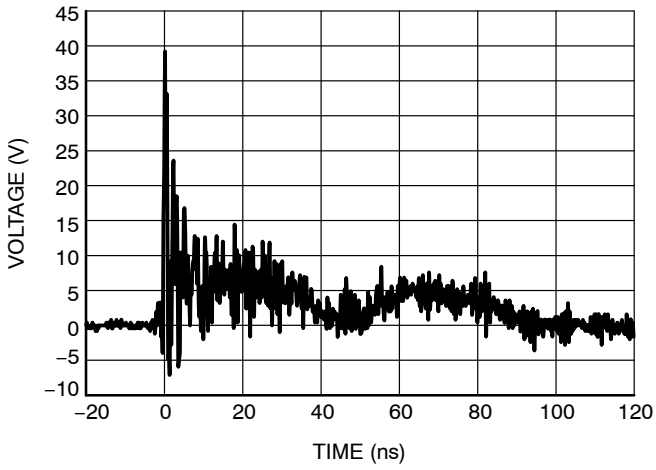


Figure 1. ESD Clamping Voltage Pin 1 to Pin 2, 8 kV Contact per IEC61000−4−2

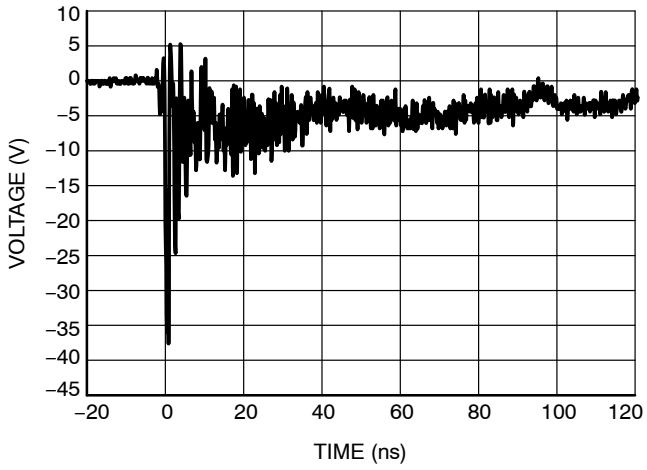


Figure 2. ESD Clamping Voltage Pin 2 to Pin 1, 8 kV Contact per IEC61000−4−2

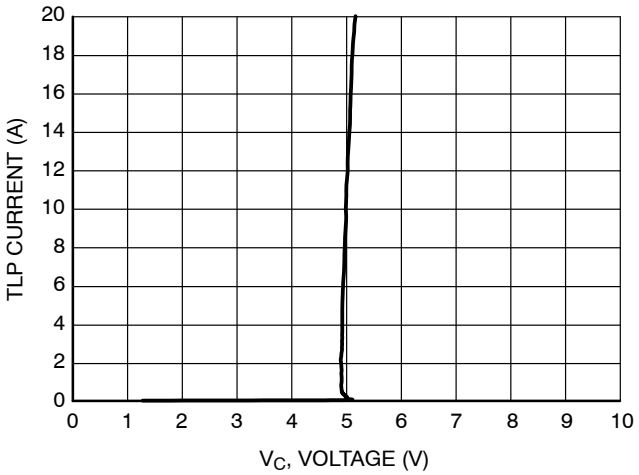


Figure 3. 100 ns TLP I−V Curve, Pin 1 to Pin 2

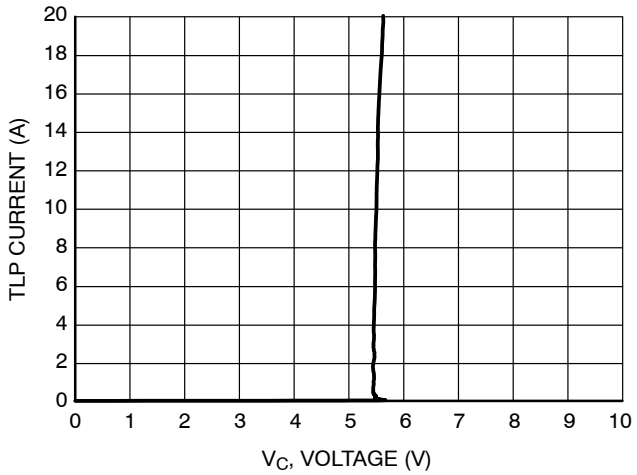


Figure 4. 100 ns TLP I−V Curve, Pin 2 to Pin 1

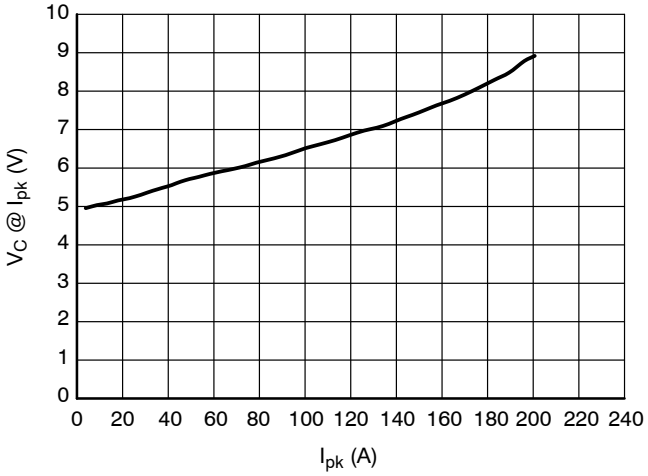


Figure 5. Clamping Voltage vs. Peak Pulse Current (t_p = 8/20 μs), Pin 1 to Pin 2

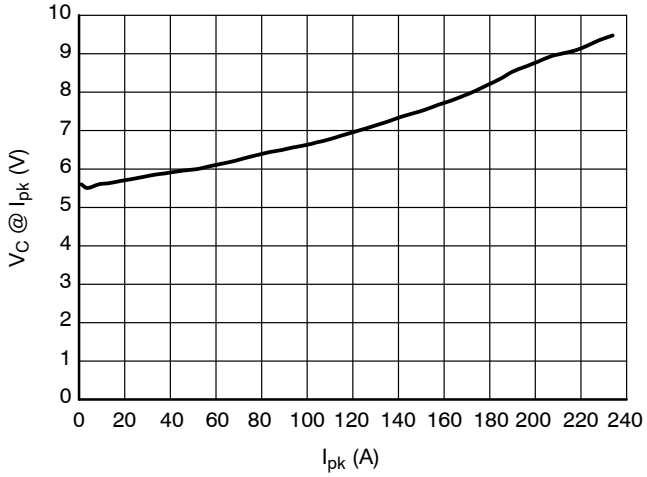


Figure 6. Clamping Voltage vs. Peak Pulse Current (t_p = 8/20 μs), Pin 2 to Pin 1

TYPICAL CHARACTERISTICS

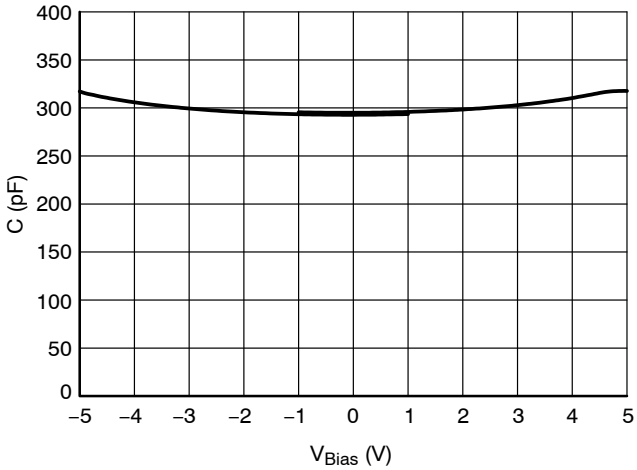


Figure 7. CV Characteristics

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

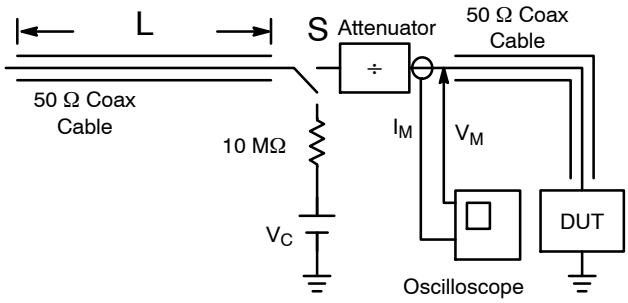


Figure 8. Simplified Schematic of a Typical TLP System

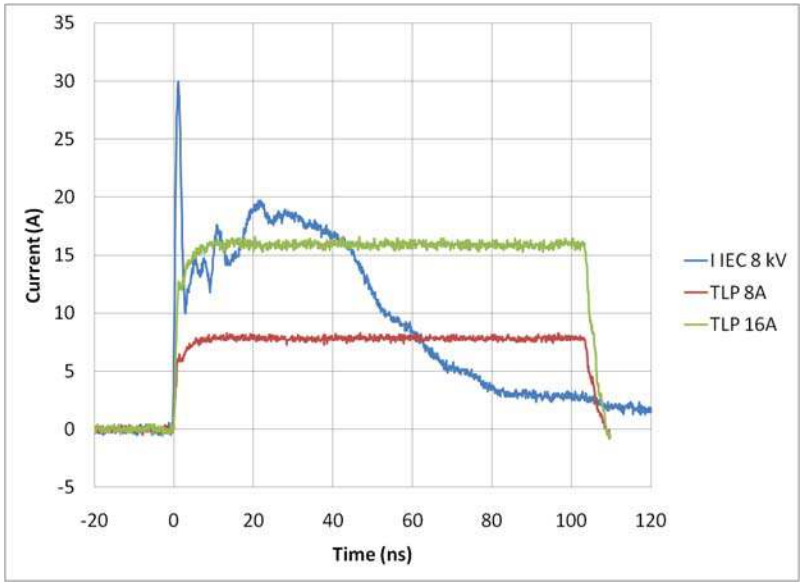


Figure 9. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

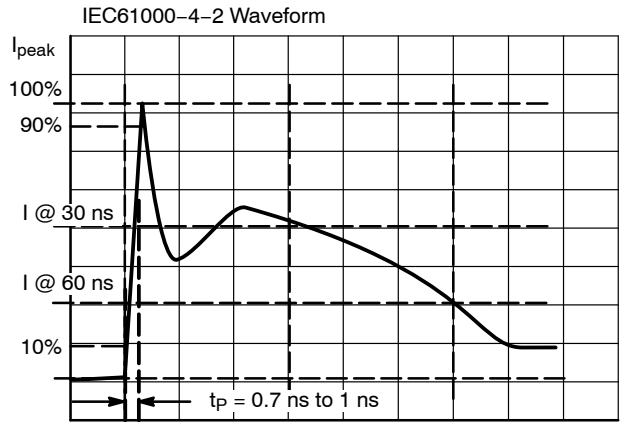


Figure 10. IEC61000−4−2 Spec

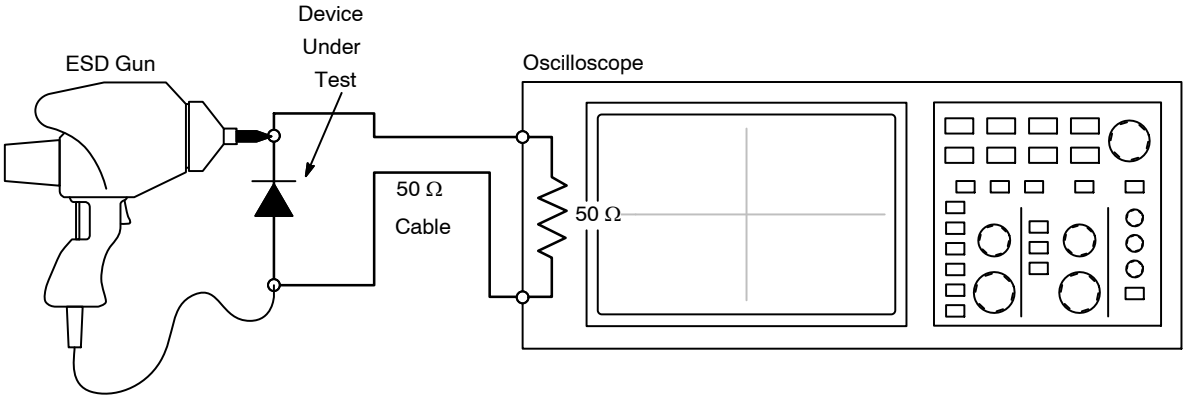


Figure 11. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

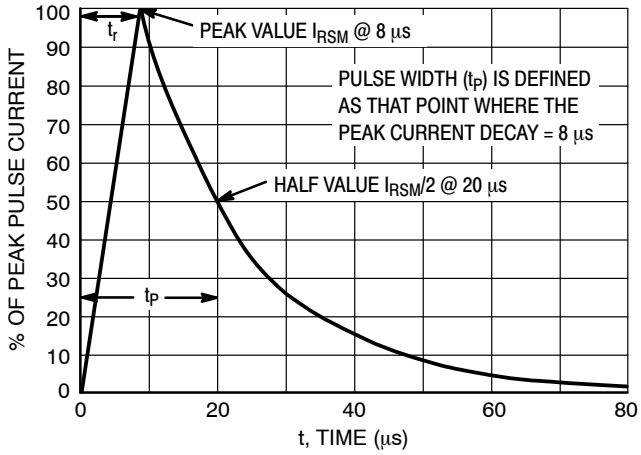


Figure 12. 8 x 20 μs Pulse Waveform

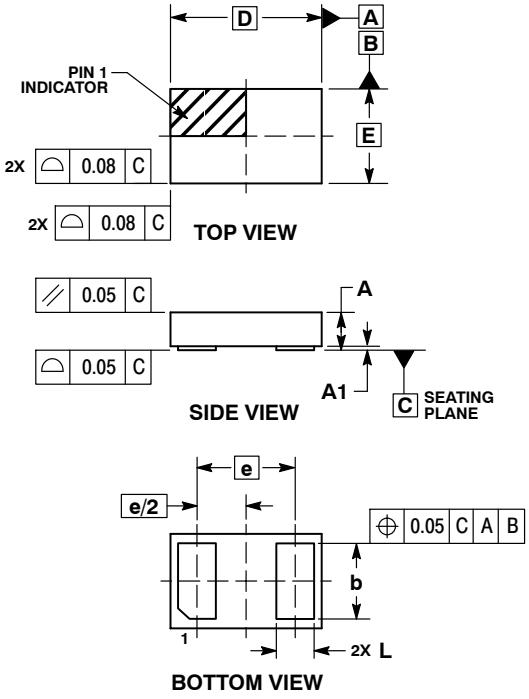
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 4:1

UDFN2 2.0x1.25, 1.3P
CASE 517DF
ISSUE A

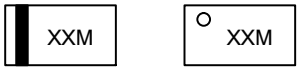
DATE 06 JUL 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
b	0.95	1.05
D	2.00 BSC	
E	1.25 BSC	
e	1.30 BSC	
L	0.45	0.55

GENERIC MARKING DIAGRAMS*



Style 1 **Style 2**

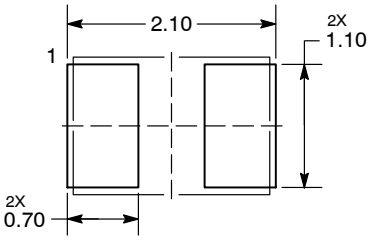
XX = Specific Device Code
M = Date Code

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
. NO POLARITY

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**UDFN2 2.0X1.25, 1.3P**	**PAGE 1 OF 1**

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