



BUK7M6R0-40H

N-channel 40 V, 6.0 mΩ standard level MOSFET in LFPAK33

29 January 2019

Product data sheet

1. General description

Automotive qualified standard level N-channel MOSFET in an LFPAK33 package using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101 for use in high performance automotive applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Trench 9 superjunction technology:
 - Low power losses, high power density
- LFPAK copper clip package technology:
 - High robustness and reliability
 - Gull wing leads for high manufacturability and AOI
- Repetitive Avalanche rated

3. Applications

- 12 V automotive systems
- Powertrain, chassis, body and infotainment applications
- Medium/Low power motor drive
- DC-DC systems
- LED lighting

4. Quick reference data

Table 1. Quick reference data

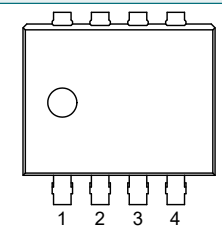
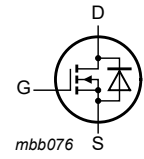
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|-----|-----|-----|------|
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | | - | - | 40 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2 | [1] | - | - | 50 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C};$ Fig. 1 | | - | - | 70 | W |
| Static characteristics | | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ °C};$ Fig. 11 | | 3.4 | 4.9 | 6 | mΩ |
| Dynamic characteristics | | | | | | | |
| Q_{GD} | gate-drain charge | $I_D = 20\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 10\text{ V};$ Fig. 13; Fig. 14 | | - | 3.9 | 7.8 | nC |
| Source-drain diode | | | | | | | |
| Q_r | recovered charge | $I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 20\text{ V}$ | | - | 19 | - | nC |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------------|---|-----|------|-----|------|
| S | softness factor | $I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ °C}$; Fig. 17 | - | 0.63 | - | |

[1] 50A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|--|---|
| 1 | S | source |  <p>LFPAK33 (SOT1210)</p> |  <p>mbb076 S</p> |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | Mounting base; connected to drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|---------|---|---------|
| | Name | Description | Version |
| BUK7M6R0-40H | LFPAK33 | Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch | SOT1210 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|--------------|--------------|
| BUK7M6R0-40H | 76H040 |

8. Limiting values

Table 5. Limiting values

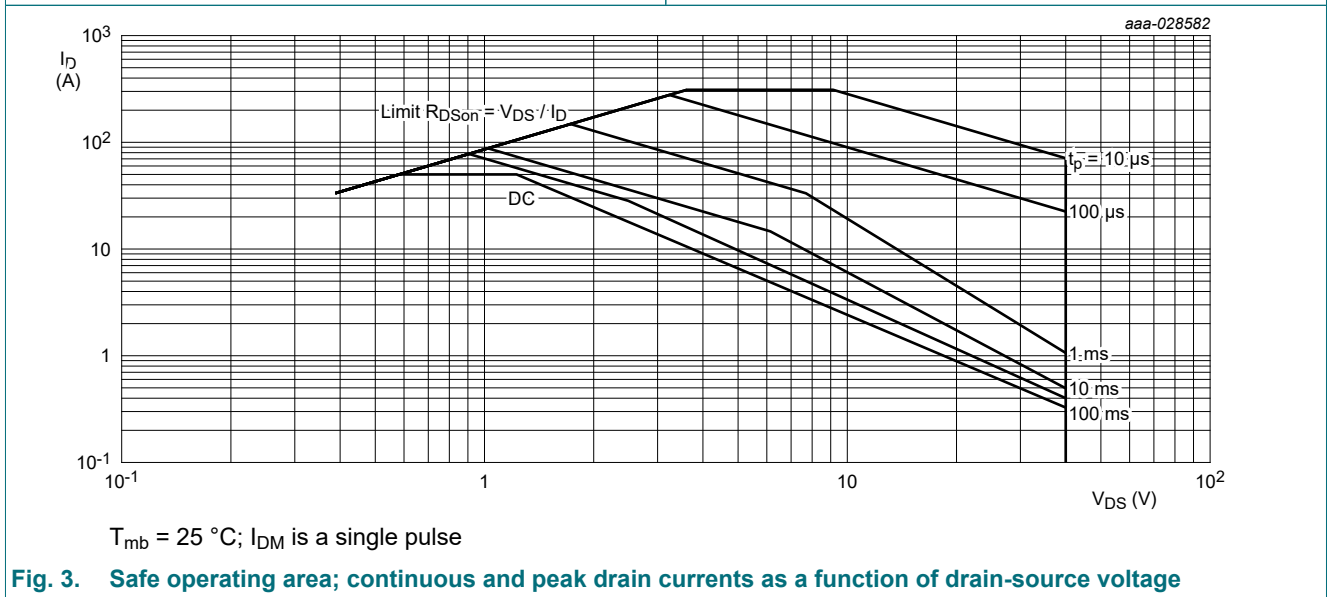
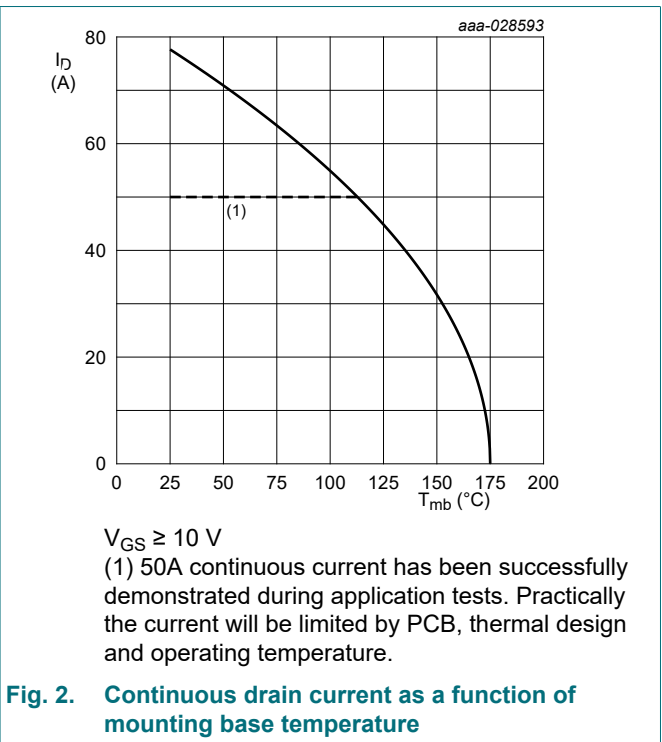
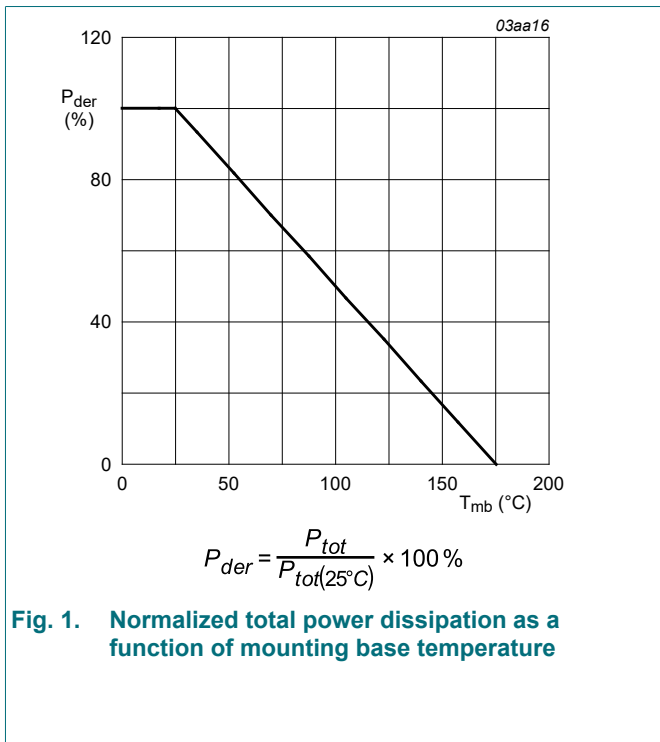
In accordance with the Absolute Maximum Rating System (IEC 60134).

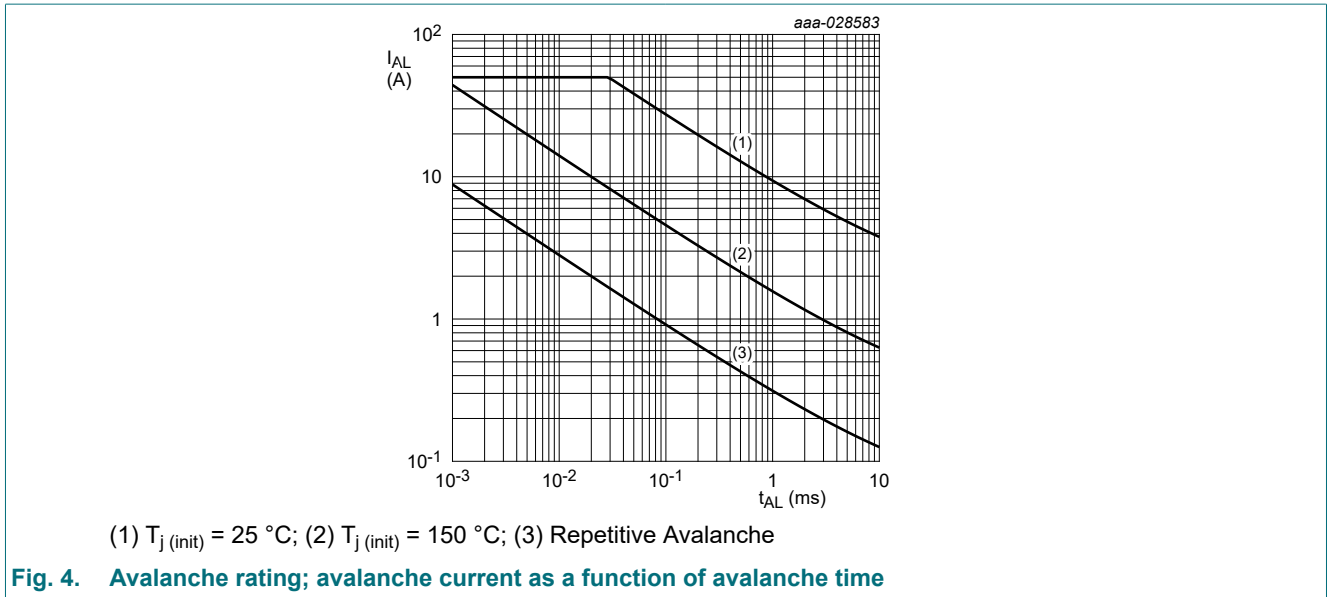
| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---|-----|-----|------|
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | - | 40 | V |
| V_{GS} | gate-source voltage | DC; $T_j \leq 175\text{ °C}$ | -10 | 20 | V |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | - | 70 | W |
| I_D | drain current | $V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2 | [1] | 50 | A |
| | | $V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2 | - | 50 | A |
| I_{DM} | peak drain current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3 | - | 311 | A |
| T_{stg} | storage temperature | | -55 | 175 | °C |
| T_j | junction temperature | | -55 | 175 | °C |

Source-drain diode

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|---|---------|-----|-------|
| I_S | source current | $T_{mb} = 25\text{ °C}$ | - | 50 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$ | - | 311 | A |
| Avalanche ruggedness | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 50\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; unclamped; Fig. 4 | [2] [3] | - | 37 mJ |

- [1] 50A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.

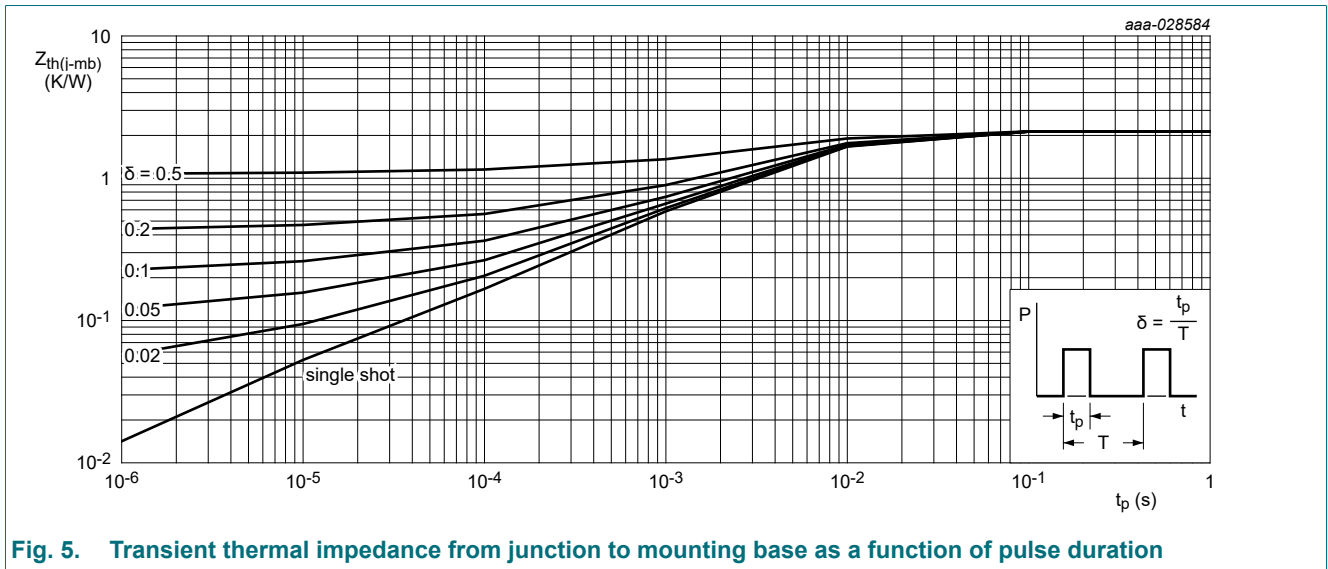




9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | - | 1.91 | 2.14 | K/W |



10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------|--|-----|------|-----|------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250\text{ }\mu\text{A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$ | 40 | 43 | - | V |
| | | $I_D = 250\text{ }\mu\text{A}; V_{GS} = 0\text{ V}; T_j = -40\text{ }^\circ\text{C}$ | - | 40.5 | - | V |

N-channel 40 V, 6.0 mΩ standard level MOSFET in LPAK33

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|--|-----|------|------|---------------|
| | | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$ | 36 | 40 | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 9 ; Fig. 10 | 2.4 | 3 | 3.6 | V |
| | | $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 9 | - | - | 4.3 | V |
| | | $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 9 | 1 | - | - | V |
| I_{DSS} | drain leakage current | $V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 0.04 | 1 | μA |
| | | $V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$ | - | 0.6 | 10 | μA |
| | | $V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$ | - | 40 | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 2 | 100 | nA |
| | | $V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 2 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 11 | 3.4 | 4.9 | 6 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 105 \text{ }^\circ\text{C};$ Fig. 12 | 4.6 | 6.9 | 9 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 125 \text{ }^\circ\text{C};$ Fig. 12 | 5.1 | 7.6 | 9.7 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 12 | 6.2 | 9.2 | 11.6 | mΩ |
| R_G | gate resistance | $f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$ | 0.3 | 0.8 | 2 | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 20 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 13 ; Fig. 14 | - | 20 | 28 | nC |
| Q_{GS} | gate-source charge | | - | 6.1 | 9.2 | nC |
| Q_{GD} | gate-drain charge | | - | 3.9 | 7.8 | nC |
| C_{iss} | input capacitance | $V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ Fig. 15 | - | 1339 | 1875 | pF |
| C_{oss} | output capacitance | | - | 446 | 624 | pF |
| C_{rss} | reverse transfer capacitance | | - | 68 | 150 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 30 \text{ V}; R_L = 1.5 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 5 \text{ } \Omega$ | - | 7.7 | - | ns |
| t_r | rise time | | - | 6.4 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 14 | - | ns |
| t_f | fall time | | - | 6.6 | - | ns |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 20 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 16 | - | 0.85 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 20 \text{ V};$ Fig. 17 | - | 25 | - | ns |
| Q_r | recovered charge | $I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 20 \text{ V}$ | - | 19 | - | nC |
| S | softness factor | $I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 17 | - | 0.63 | - | |
| | | $I_S = 20 \text{ A}; dI_S/dt = -500 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 17 | - | 0.43 | - | |

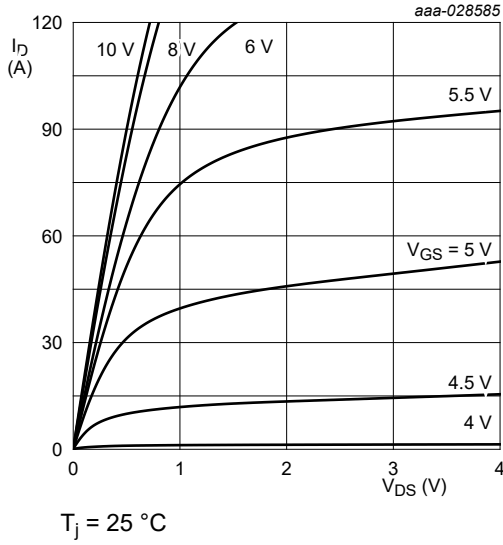


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

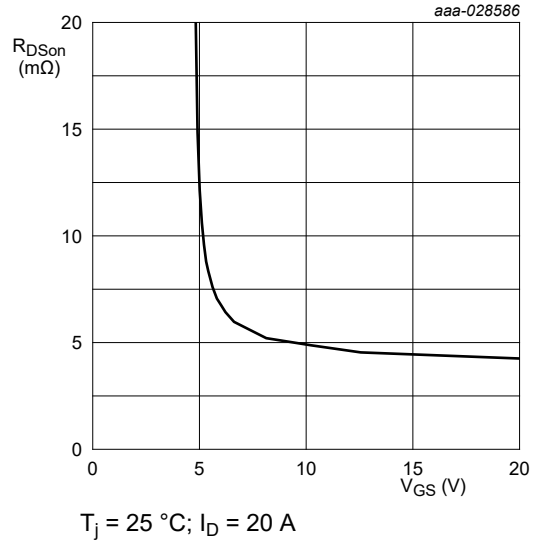


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

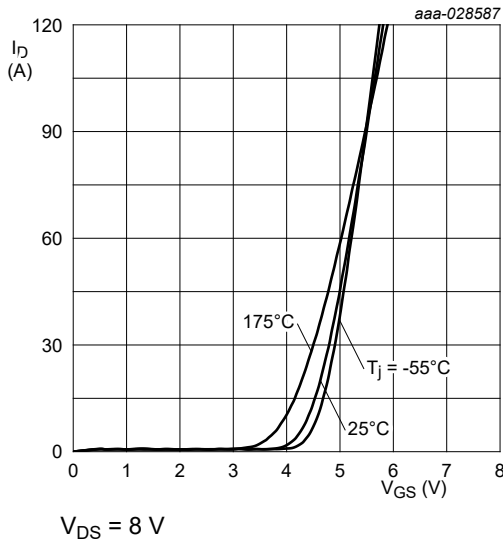


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

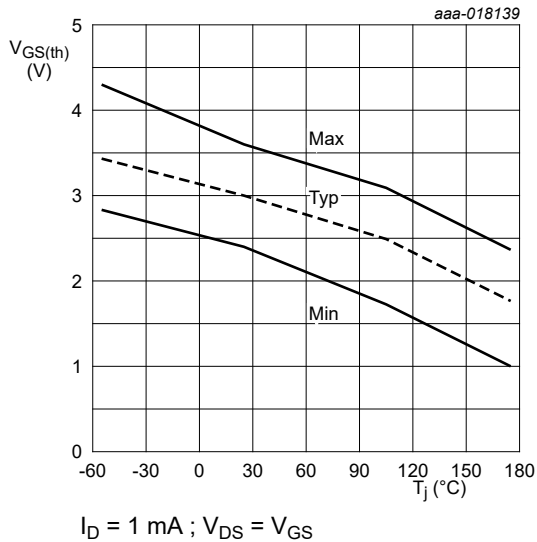


Fig. 9. Gate-source threshold voltage as a function of junction temperature

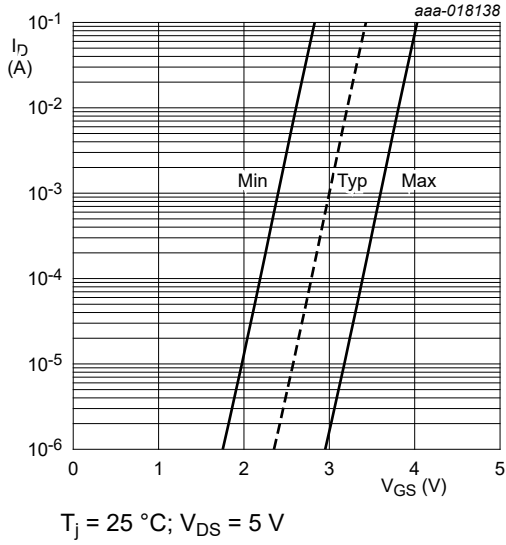


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

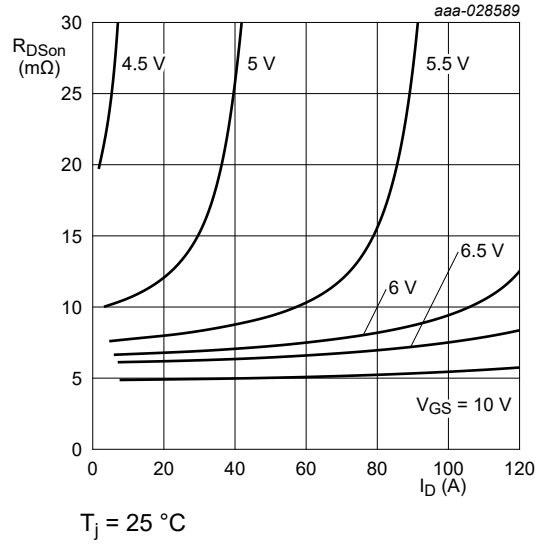


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

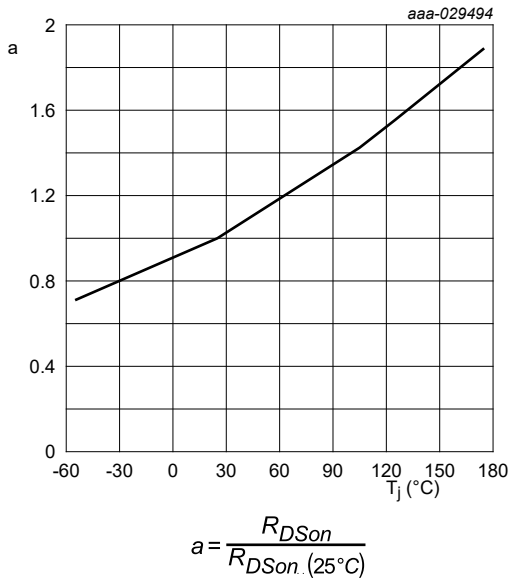


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

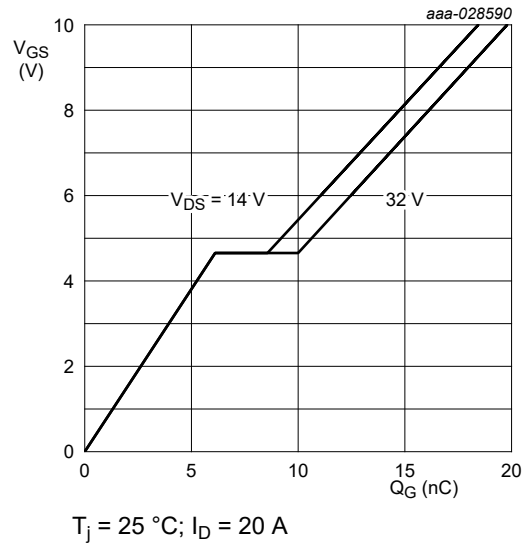


Fig. 13. Gate-source voltage as a function of gate charge; typical values

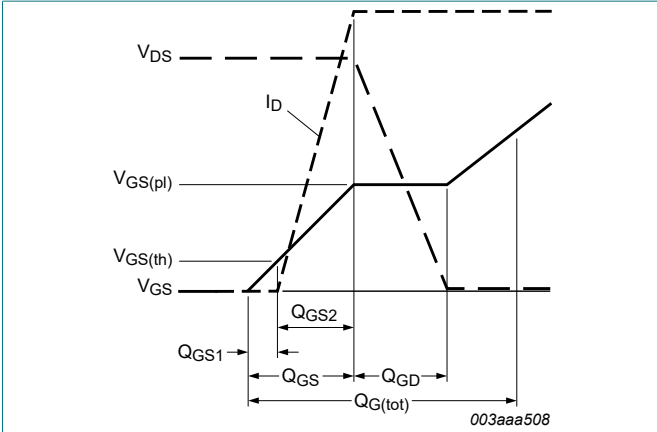
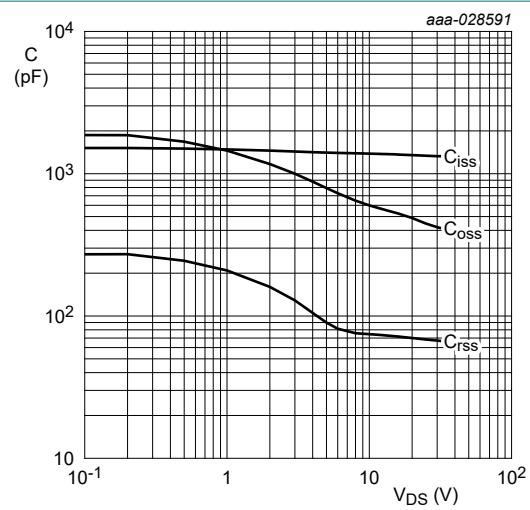
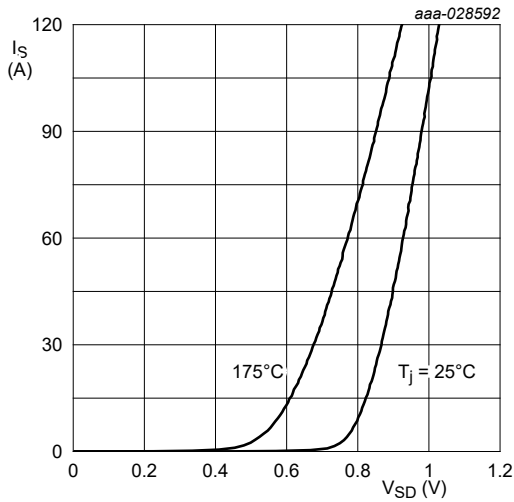


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0$ V; $f = 1$ MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0$ V

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

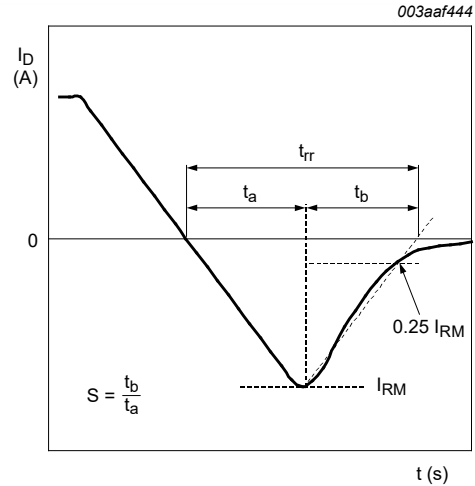


Fig. 17. Reverse recovery timing definition

11. Package outline

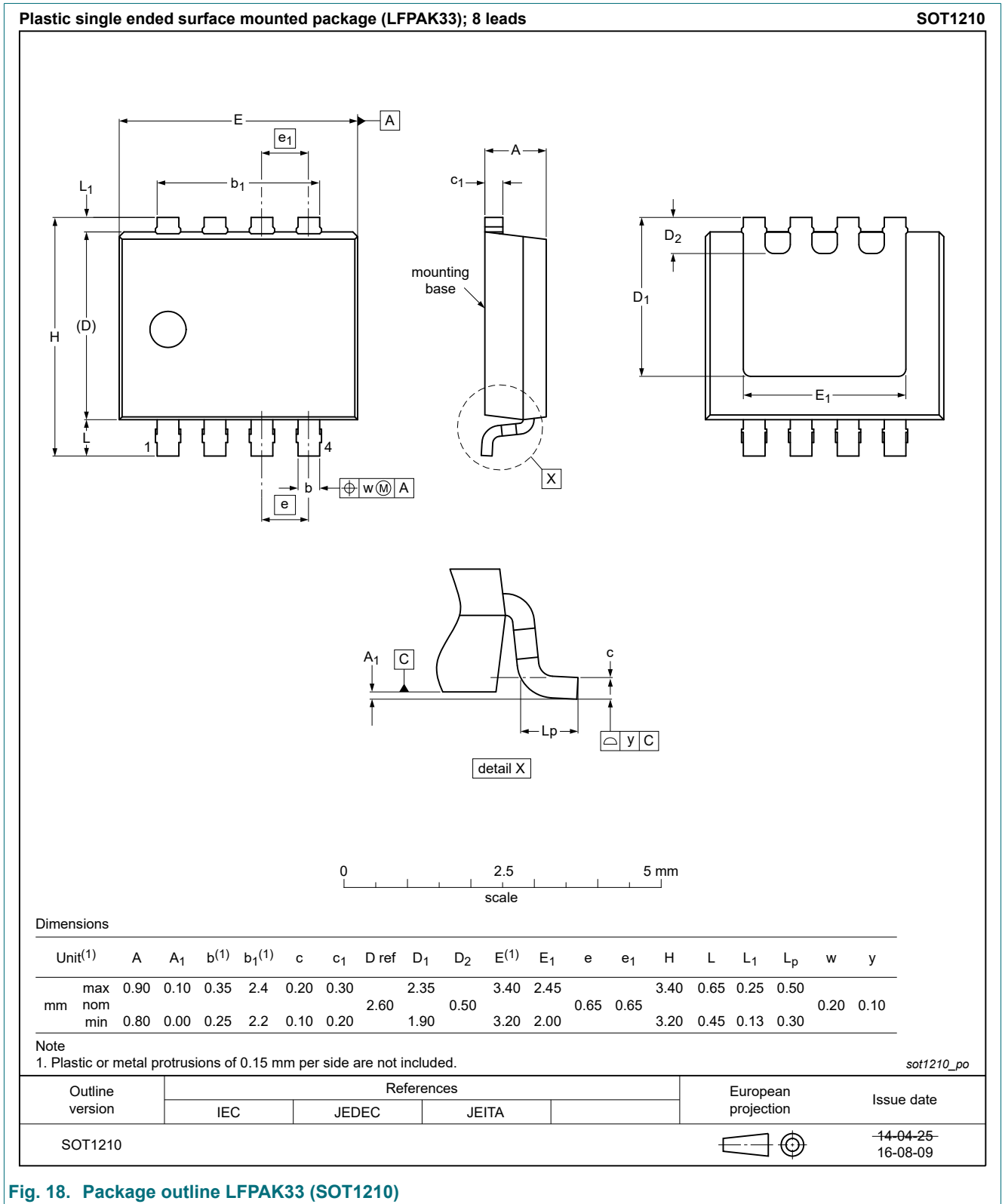


Fig. 18. Package outline LPAK33 (SOT1210)

12. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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